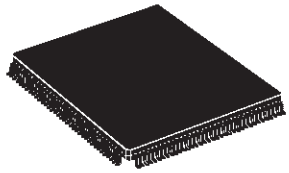
ST10F168

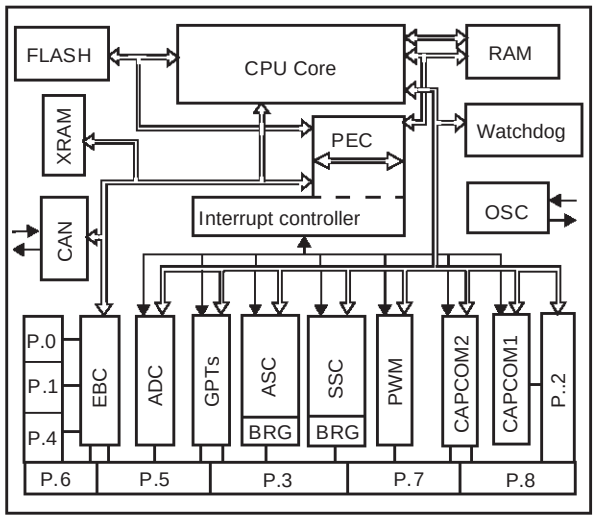
16-BIT MCU WITH 256K BYTE FLASH MEMORY AND 8K BYTE RAM

- HIGH PERFORMANCE CPU
  - 16-BIT CPU WITH 4-STAGE PIPELINE
  - 80ns INSTRUCTION CYCLE TIME AT 25MHz CPU CLOCK
  - 400ns 16 X 16-BIT MULTIPLICATION
  - 800ns 32 / 16-BIT DIVISION
  - ENHANCED BOOLEAN BIT MANIPULATION FACILITIES
  - ADDITIONAL INSTRUCTIONS TO SUPPORT HLL AND OPERATING SYSTEMS
  - SINGLE-CYCLE CONTEXT SWITCHING SUPPORT
- MEMORY ORGANIZATION
  - 256K BYTE ON-CHIP FLASH MEMORY
  - 10K ERASING / PROGRAMMING CYCLES
  - UP TO 16M BYTE LINEAR ADDRESS SPACE FOR CODE AND DATA (5M BYTE WITH CAN)
  - 2K BYTE ON-CHIP INTERNAL RAM (IRAM)
  - 6K BYTE ON-CHIP EXTENSION RAM (XRAM)
  - 20 YEAR DATA RETENTION TIME
- FAST AND FLEXIBLE BUS
  - PROGRAMMABLE EXTERNAL BUS CHARACTE- RISTICS FOR DIFFERENT ADDRESS RANGES
  - 8-BIT OR 16-BIT EXTERNAL DATA BUS
  - MULTIPLEXED OR DEMULTIPLEXED EXTERNAL ADDRESS / DATA BUSES
  - FIVE PROGRAMMABLE CHIP-SELECT SIGNALS
  - HOLD-ACKNOWLEDGE BUS ARBITRATION SUPPORT
- INTERRUPT
  - 8-CHANNEL PERIPHERAL EVENT CONTROLLER FOR SINGLE CYCLE, INTERRUPT DRIVEN DATA TRANSFER
  - 16-PRIORITY-LEVEL INTERRUPT SYSTEM WITH 56 SOURCES, SAMPLE-RATE DOWN TO 40ns
- TIMERS
  - TWO MULTI-FUNCTIONAL GENERAL PURPOSE TIMER UNITS WITH 5 TIMERS
  - TWO 16-CHANNEL CAPTURE / COMPARE UNITS.
- 4-CHANNEL PWM UNIT
- SERIAL CHANNELS
  - SYNCHRONOUS / ASYNCHRONOUS SERIAL CHANNEL
  - HIGH-SPEED SYNCHRONOUS CHANNEL



PQFP144 (28 x 28 mm)
(Plastic Quad Flat Pack)

- A/D CONVERTER
  - 16-CHANNEL 10-BIT
  - 7.76µS CONVERSION TIME
- FAIL-SAFE PROTECTION
  - PROGRAMMABLE WATCHDOG TIMER
  - OSCILLATOR WATCHDOG
- ON-CHIP CAN 2.0B INTERFACE
- ON-CHIP BOOTSTRAP LOADER
- CLOCK GENERATION
  - ON-CHIP PLL
  - DIRECT OR PRESCALED CLOCK INPUT.
- UP TO 111 GENERAL PURPOSE I/O LINES
  - INDIVIDUALLY PROGRAMMABLE AS INPUT, OUTPUT OR SPECIAL FUNCTION.
  - PROGRAMMABLE THRESHOLD (HYSTERESIS)
- IDLE AND POWER DOWN MODES
- SINGLE VOLTAGE SUPPLY: 5V ±10%
- 144-PIN PQFP PACKAGE



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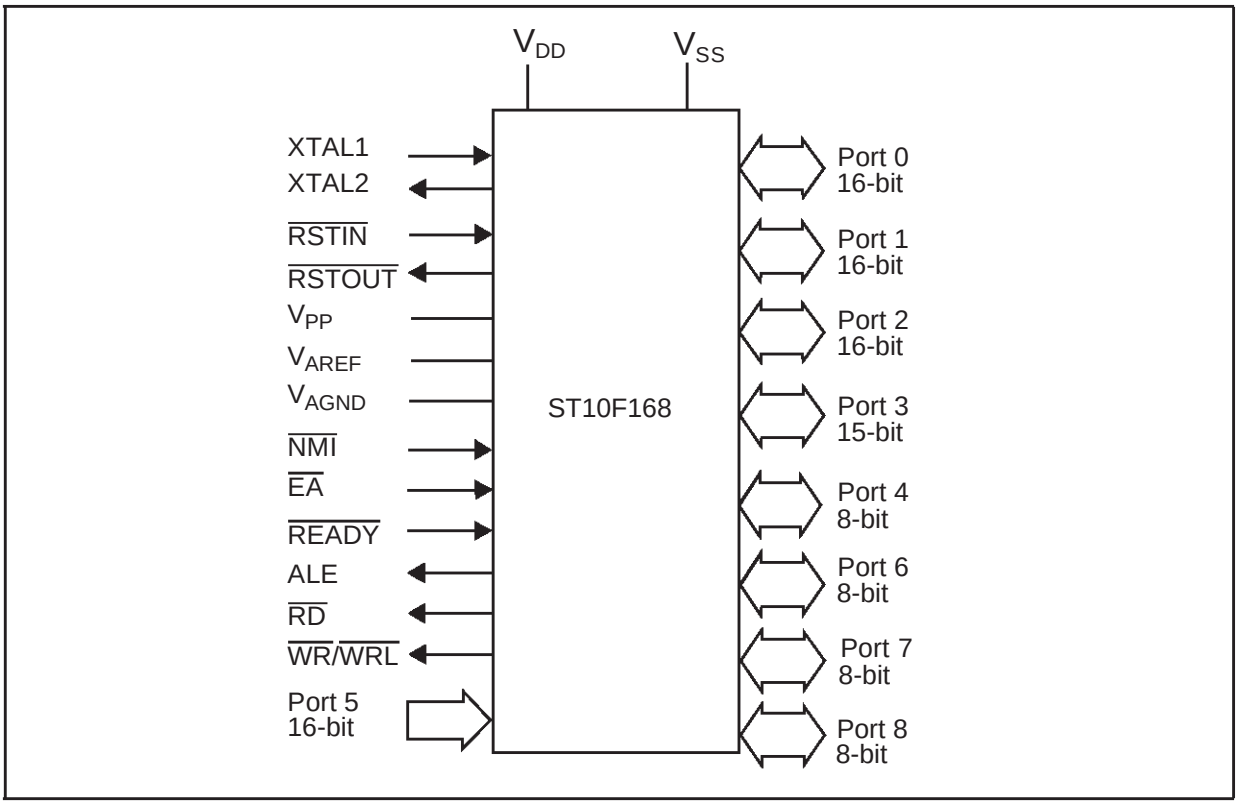
1 - INTRODUCTION

The ST10F168 is a derivative of the STMicroelectronics 16-bit single-chip CMOS microcontrollers. It combines high CPU performance (up to 12.5 million instructions per second) with high peripheral functionality and enhanced I/O capabilities. It also provides on-chip high-speed Flash memory, on-chip high-speed RAM, and clock generation via PLL.

Figure 1 : Logic Symbol



2 - PIN DATA

Figure 2 : Pin Configuration (top view)

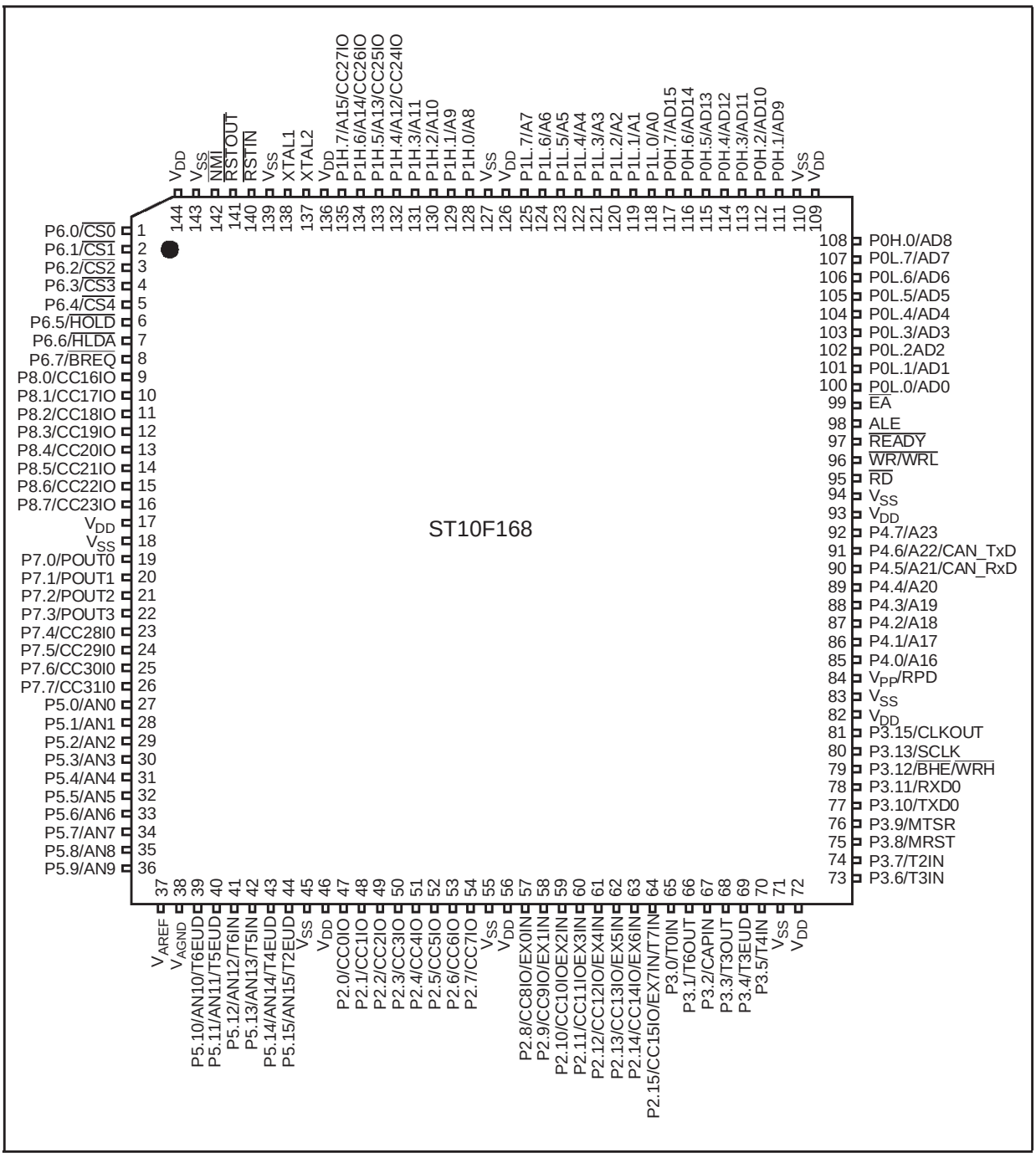


Table 1 : Pin Description

Symbol	Pin	Type	Function		
P6.0 - P6.7	1 - 8	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 6 outputs can be configured as push-pull or open drain drivers. The following Port 6 pins have alternate functions:		
	1	O	P6.0	$\overline{CS0}$	Chip Select 0 Output
	...	...	...	...	...
	5	O	P6.4	$\overline{CS4}$	Chip Select 4 Output
	6	I	P6.5	$\overline{HOLD}$	External Master Hold Request Input
	7	O	P6.6	$\overline{HLDA}$	Hold Acknowledge Output
	8	O	P6.7	$\overline{BREQ}$	Bus Request Output
P8.0 - P8.7	9-16	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 8 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 8 is selectable (TTL or special). The following Port 8 pins have alternate functions:		
	9	I/O	P8.0	CC16IO	CAPCOM2: CC16 Capture Input / Compare Output
	...	...	...	...	...
	16	I/O	P8.7	CC23IO	CAPCOM2: CC23 Capture Input / Compare Output
P7.0 - P7.7	19-26	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 7 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or special). The following Port 7 pins have alternate functions:		
	19	O	P7.0	POUT0	PWM Channel 0 Output
	...	...	...	...	...
	22	O	P7.3	POUT3	PWM Channel 3 Output
	23	I/O	P7.4	CC28IO	CAPCOM2: CC28 Capture Input / Compare Output
	...	...	...	...	...
	26	I/O	P7.7	CC31IO	CAPCOM2: CC31 Capture Input / Compare Output
P5.0 - P5.9 P5.10 - P5.15	27-36 39-44	I I	16-bit input-only port with Schmitt-Trigger characteristics. The pins of Port 5 can be the analog input channels (up to 16) for the A/D converter, where P5.x equals ANx (Analog input channel x), or they are timer inputs:		
	39	I	P5.10	T6EUD	GPT2 Timer T6 External Up / Down Control Input
	40	I	P5.11	T5EUD	GPT2 Timer T5 External Up / Down Control Input
	41	I	P5.12	T6IN	GPT2 Timer T6 Count Input
	42	I	P5.13	T5IN	GPT2 Timer T5 Count Input
	43	I	P5.14	T4EUD	GPT1 Timer T4 External Up / Down Control Input
	44	I	P5.15	T2EUD	GPT1 Timer T2 External Up / Down Control Input

Table 1 : Pin Description (continued)

Symbol	Pin	Type	Function		
P2.0 - P2.7 P2.8 - P2.15	47-54 57-64	I/O	16-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 2 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or special). The following Port 2 pins have alternate functions:		
	47	I/O	P2.0	CC0IO	CAPCOM: CC0 Capture Input / Compare Output
	...	...	...	...	...
	54	I/O	P2.7	CC7IO	CAPCOM: CC7 Capture Input / Compare Output
	57	I/O	P2.8	CC8IO	CAPCOM: CC8 Capture Input / Compare Output
		I		EX0IN	Fast External Interrupt 0 Input
	...	...	...	...	...
	64	I/O	P2.15	CC15IO	CAPCOM: CC15 Capture Input / Compare Output
		I		EX7IN	Fast External Interrupt 7 Input
		I		T7IN	CAPCOM2 Timer T7 Count Input
P3.0 - P3.5 P3.6 - P3.13, P3.15	65-70, 73-80, 81	I/O I/O I/O	15-bit (P3.14 is missing) bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 3 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or special). The following Port 3 pins have alternate functions:		
	65	I	P3.0	T0IN	CAPCOM Timer T0 Count Input
	66	O	P3.1	T6OUT	GPT2 Timer T6 Toggle Latch Output
	67	I	P3.2	CAPIN	GPT2 Register CAPREL Capture Input
	68	O	P3.3	T3OUT	GPT1 Timer T3 Toggle Latch Output
	69	I	P3.4	T3EUD	GPT1 Timer T3 External Up / Down Control Input
	70	I	P3.5	T4IN	GPT1 Timer T4 Input for Count / Gate / Reload / Capture
	73	I	P3.6	T3IN	GPT1 Timer T3 Count / Gate Input
	74	I	P3.7	T2IN	GPT1 Timer T2 Input for Count / Gate / Reload / Capture
	75	I/O	P3.8	MRST	SSC Master-Receiver / Slave-Transmitter I/O
	76	I/O	P3.9	MTSR	SSC Master-Transmitter / Slave-Receiver O/I
	77	O	P3.10	TxD0	ASC0 Clock / Data Output (Asynchronous / Synchronous)
	78	I/O	P3.11	RxD0	ASC0 Data Input (Asynchronous) or I/O (Synchronous)
	79	O	P3.12	$\overline{BHE}$	External Memory High Byte Enable Signal
				$\overline{WRH}$	External Memory High Byte Write Strobe
	80	I/O	P3.13	SCLK	SSC Master Clock Output / Slave Clock Input
	81	O	P3.15	CLKOUT	System Clock Output (=CPU Clock)

Table 1 : Pin Description (continued)

Symbol	Pin	Type	Function
P4.0 - P4.7	85-92	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. For external bus configuration, Port 4 can be used to output the segment address lines:
	85-89	O	P4.0-P4.4 A16-A20 Segment Address Line
	90	O	P4.5 A21 Segment Address Line
		I	CAN_RxD CAN Receiver Data Input
	91	O	P4.6 A22 Segment Address Line
		O	CAN_TxD CAN Transmitter Data Output
	92	O	P4.7 A23 Most Significant Segment Addrress Line
$\overline{RD}$	95	O	External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access.
$\overline{WR}$/$\overline{WRL}$	96	O	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$ mode this pin is activated for low Byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in the SYSCON register for mode selection.
READY/ $\overline{READY}$	97	I	Ready Input. The active level is programmable. When the Ready function is enabled, the selected inactive level at this pin, during an external memory access, will force the insertion of wait state cycles until the pin returns to the selected active level.
ALE	98	O	Address Latch Enable Output. In case of use of external addressing or of multiplexed mode, this signal is the latch command of the address lines.
$\overline{EA}$	99	I	External Access Enable pin. A low level at this pin during and after Reset forces the ST10F168 to start the program from the external memory space. A high level forces the ST10F168 to start in the internal memory space.
P0L.0 - P0L.7 P0H.0 P0H.1 - P0H.7	100 - 107, 108, 111 - 117	I/O	Two 8-bit bidirectional I/O ports P0L and P0H, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. In case of an external bus configuration, Port0 serves as the address (A) and as the address / data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: D0 – D7 D0 - D7 P0H.0 – P0H.7: I/O D8 - D15 **Multiplexed bus modes** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: AD0 – AD7 AD0 - AD7 P0H.0 – P0H.7: A8 – A15 AD8 – AD15

Table 1 : Pin Description (continued)

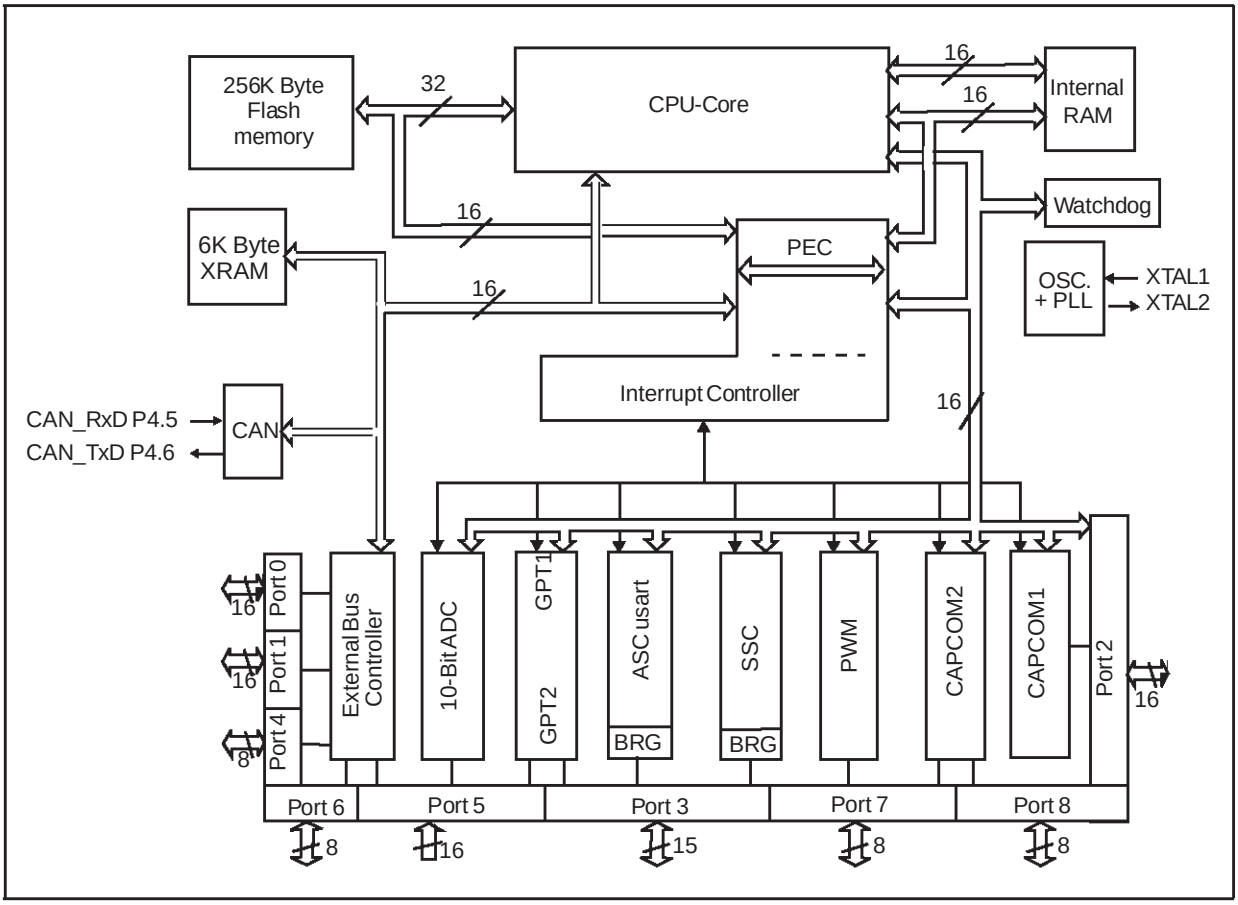
Symbol	Pin	Type	Function
P1L.0 - P1L.7 P1H.0 - P1H.7	118-125 128-135	I/O	Two 8-bit bidirectional I/O ports P1L and P1H, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode. The following Port1 pins have alternate functions:
	132	I	P1H.4 CC24IO CAPCOM2: CC24 Capture Input
	133	I	P1H.5 CC25IO CAPCOM2: CC25 Capture Input
	134	I	P1H.6 CC26IO CAPCOM2: CC26 Capture Input
	135	I	P1H.7 CC27IO CAPCOM2: CC27 Capture Input
XTAL1	138	I	XTAL1 Oscillator amplifier and internal clock generator input
XTAL2	137	O	XTAL2: Oscillator amplifier circuit output. To clock the device from an external source, drive XTAL1 while leaving XTAL2 unconnected. Minimum and maximum high / low and rise / fall times specified in the AC Characteristics must be observed.
$\overline{\text{RSTIN}}$	140	I	Reset Input with Schmitt-Trigger characteristics. A low level at this pin for a specified duration while the oscillator is running resets the ST10F168. An internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}. In bidirectional reset mode (enabled by setting bit BDRSTEN in SYSCON register), the RSTIN line is pulled low for the duration of the internal reset sequence.
$\overline{\text{RSTOUT}}$	141	O	Internal Reset Indication Output. This pin is set to a low level during hardware, software or watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.
$\overline{\text{NMI}}$	142	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. If bit PWDCFG = '0' in SYSCON register, when the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the ST10F168 to go into power down mode. If $\overline{\text{NMI}}$ is high and PWDCFG ='0', when PWRDN is executed, the part will continue to run in normal mode. If it is not used, pin $\overline{\text{NMI}}$ should be pulled high externally.
V_{AREF}	37	-	A/D converter reference voltage.
V_{AGND}	38	-	A/D converter reference ground.
V_{PP}/RPD	84	-	Flash programming voltage. Programming voltage of the on-chip Flash memory must be supplied to this pin. It is used also as the timing pin for the return from interruptible powerdown mode.
V_{DD}	17,46, 56,72, 82,93, 109, 126, 136, 144	-	Digital Supply Voltage: = + 5V during normal operation and idle mode. ≥ 2.5V during power down mode.
V_{SS}	18,45, 55,71, 83,94, 110, 127, 139, 143	-	Digital Ground.

3 - FUNCTIONAL DESCRIPTION

The architecture of the ST10F168 combines advantages of both RISC and CISC processors and an advanced peripheral subsystem.

The block diagram gives an overview of the different on-chip components and the high bandwidth internal bus structure of the ST10F168.

Figure 3 : Block Diagram



4 - MEMORY ORGANIZATION

The memory space of the ST10F168 is configured in a Von Neumann architecture. Code memory, data memory, registers and I/O ports are organized within the same linear address space of 16M Byte. The entire memory space can be accessed bytewise or wordwise. Particular portions of the on-chip memory have additionally been made directly bit addressable.

FLASH: 256K Byte of on-chip Flash memory. See *Flash Memory* on page 13

IRAM: 2K Byte of on-chip internal RAM (dual-port) is provided as a storage for data, system stack, general purpose register banks and code. A register bank is 16 wordwide (R0 to R15) and / or bytewide (RL0, RH0, …, RL7, RH7) general purpose registers.

XRAM: 6K Byte of on-chip extension RAM (single port XRAM) is provided as a storage for data, user stack and code. The XRAM is connected to the internal XBUS and is accessed like an external memory in 16-bit demultiplexed bus-mode without wait state or read / write delay (80ns access at 25MHz CPU clock). Byte and Word access are allowed.
The XRAM address range is 00'D000h - 00'E7FFh if the XRAM is enabled (XPEN bit 2 of SYSCON register). As the XRAM appears like external memory, it cannot be used for the ST10F168's system stack or register banks. The XRAM is not provided for single bit storage and therefore is not bit addressable. If bit XPEN is cleared, then any access in the address range 00'D000h - 00'E7FFh will be directed to external memory interface, using the BUSCONx register corresponding to address matching ADDRSELx register.

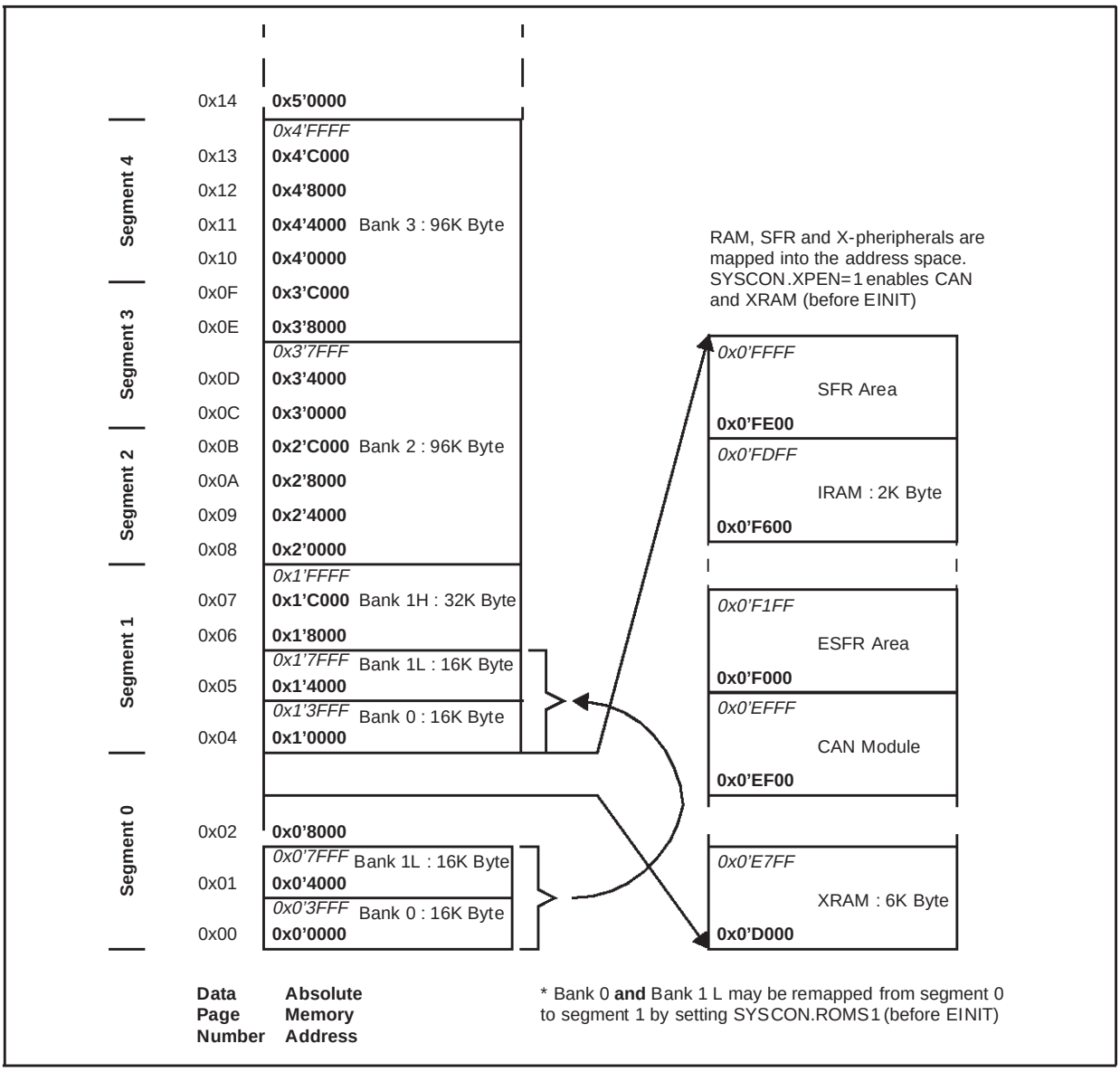
SFR/ESFR: 1024 Byte (2 x 512 Byte) of address space is reserved for the Special Function Register areas. SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units.

CAN: Address range 00'EF00h - 00'EFFFh is reserved for the CAN Module access. The CAN is enabled by setting XPEN bit 2 of the SYSCON register. Accesses to the CAN Module use demultiplexed addresses and a 16-bit data bus (Byte accesses are possible). Two wait states give an access time of 160ns at 25MHz CPU clock. No tristate wait state is used.

Note: If the CAN module is used, Port 4 can not be programmed to output all 8 segment address lines. Therefore, only 4 segment address lines can be used, reducing the external memory space to 5M Byte (1M Byte per $\overline{CS}$ line)

To meet the needs of designs where more memory is required than is provided on chip, up to 16M Byte of external RAM and / or ROM can be connected to the microcontroller.

Figure 4 : ST10F168 on-chip memory mapping



5 - FLASH MEMORY

The ST10F168 provides 256K Byte of an electrically erasable and reprogrammable Flash Memory on-chip.

The Flash Memory can be used both for code and data storage. It is organized into four 32-bit wide blocks allowing even double Word instructions to be fetched in one machine cycle. The four blocks of size16K, 48K, 96K and 96K Byte can be erased and reprogrammed individually (see Table 2 and Table 3).

The Flash Memory can be programmed in a programming board or in the target system which provides high system flexibility. The algorithms to program or erase the flash memory are embedded in the Flash Memory itself (ST Embedded Algorithm Kernel, or STEAK^{TM}).

To start a program / erase operation, the user's software has just to load GPRs with the address and data to be programmed, or sector to be erased. STEAK uses embedded routines, which check the validity of the programmed parameters, decode and then execute the programming or erase command. During operation, the STEAK routines carry out checks and retries to verify proper cell programming or erasing. When an error occurs, STEAK returns an error-code which identifies the cause of the error.

A Flash Memory protection option prevents the read-back of the Flash Memory contents from external memory, or from on-chip RAM. Code operation from within the Flash continues as normal.

The first bank (16K Byte) and part of the second bank (16K Byte out of 48K Byte) of the on-chip Flash Memory of the ST10F168 can be mapped to either segment 0 (addresses 00000h to 07FFFh) or to segment 1 (addresses 10000h to 17FFFh) during the initialization phase. External memory can be used for additional system flexibility.

V_{DD} = 5V ± 10%, V_{PP} = 12V ± 5%, V_{SS} = 0V, f_{CPU} = 25MHz, for Q6 version : T_A = -40°C, +85°C and for Q3 version T_A = -40°C, + 125°C.

Table 2 : Flash Memory Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{CPU}	CPU Frequency during erasing / programming operation		5	-	32	MHz
Cyc	Erasing / Programming Cycles	f_{CPU} = 25MHz	-	-	10K	
t_{SPRG}	Single Word Programming Time	f_{CPU} = 25MHz	-	40	1500	µs
t_{DPRG}	Double Word Programming Time	f_{CPU} = 25MHz	-	40	1500	µs
t_{EBNK}	Sector Erasing Time	f_{CPU} = 25MHz	-	3	15	s
t_{RET}	Data Retention Time	Defectivity below 1ppm / year	20	-	-	year

Table 3 : Flash Memory Bank Organisation

Bank	Addresses (segment 0)	Addresses (segment 1)	Size (Byte)
0	000000h to 003FFFh	010000h to 013FFFh	16K
1	004000h to 007FFFh + 018000h to 01FFFFh	014000h to 01FFFFh	48K
2	020000h to 037FFFh	020000h to 03FFFFh	96K
3	038000h to 04FFFFh	038000h to 04FFFFh	96K

5.1 - Programming / Erasing with ST Embedded Algorithm Kernel

There are three stages to run STEAK :

– To load the registers R0 to R4 with the STEAK command, the address and the data to be programed, or sector to be erased. Table 4 gives the STEAK parameters for each type of Flash programming / erasing operation. Table 5 defines the codes used in Table 4.

– To initiate the Unlock Sequence. The Unlock Sequence is composed of two consecutive writes to an even address in the Flash active address space - the first write has direct addressing mode (MOV mem, Rwn) - the second write has indirect addressing mode (MOV [Rwm], Rwn). Rwn can be any unused Word-GPR (R6 to R15) loaded with a value resulting in the same even address as “mem”.

– To read the return values in R0. When the embedded programming / erasing algorithm returns to trigger point, return values are given in R0. Table 6 gives the error-code definitions, Table 7 gives the return values in each register for each type of Flash programming / erasing command.

Note: The Flash Embedded STEAK Algorithms require at least 50 words on the Internal System Stack. STEAK verifies that there is enough free space on the System Stack, before performing a programming or erasing operation.The MDH, MDL and MDC register content are modified.

Code examples for programming and erasing the Flash Memory using STEAK are given in Section 5.2.

Note For more details refer to STEAK application note on www.st.com web site.

Table 4 : STEAK parameters

Command	R0	R1	R2	R3	R4
Single Word programming	55Ash	AddOff	W	nu	2TCL
Double Word programming	DD4sh	AddOff	DWL	DWH	2TCL
Multiple (block) programming	AA5sh	BegAddOff	EndAddOff	SourceAddr	2TCL
Sector Erasing	EEEEh	5555h	Bnk	Bnk	2TCL
Set Flash Protection UPROG bit	CCCCh	5555h	3333h	AAAAh	2TCL
Read Status	7777h	nu	nu	nu	2TCL

Table 5 : Programming / erasing code definition

s	Segment of the Target Flash Memory cell,
AddOff	Segment Offset of the Target Flash Memory cell. Must be even value (Word-aligned address).
W	Data (Word) to be written in Flash.
DWL,DWH	Data (double Word, DHL = low Word, DWH = high Word) to be written in Flash.
BegAddOff	Segment Offset of the FIRST Target Flash Memory Word to be written in a Multiple programming command. Must be even value (Word-aligned address).
EndAddOff	Segment Offset of the LAST Target Flash Memory Word to be written in a Multiple programming command. Must be even value (Word-aligned address). The value D = (EndAddOff - BegAddOff) must be: 0 <= D < 16384 (ie. up to one page (16K Byte) can be written in the flash with one multi-Word programming command).
SourceAdd	Start address for the block to be programmed. This address is using implicitly the data paging mechanism of the CPU. SourceAdd value must respect the following rules : - SourceAdd + (EndAddOff - BegAddOff) < 16384. - Page 0 and 1 can NOT be used for source data if bit ROMS1 = ‘1’ (in SYSCON register). Note that source data can be located in Flash (In pages 0, 1, 6 to 19 if bit ROMS1 = ‘0’, or in pages 4 to 19 if bit ROMS1 = ‘1’).
Bnk	Number of the Bank to be erased. For security, R2 and R3 must hold the same value.
2TCL	CPU clock period in nano-seconds (eg. R4 = 50 (32h) means CPU frequency is 20MHz).

Table 6 : Error Code Definition (R0 content after STEAK execution)

Error Code	Meaning
00h	Operation was successful
01h	Flash Protection is active
02h	Vpp voltage not present
03h	Programming operation failed
04h	Address value (R1) incorrect: not in Flash address area or odd
05h	CPU period out of range (must be between 30 ns to 500 ns)
06h	Not enough free space on system stack for proper operation
07h	Incorrect bank number (R2,R3) specified
08h	Erase operation failed (phase 1)
09h	Bad source address for Multiple Word programming command
0Ah	Bad number of words to be copied in Multiple Word programming command: one destination will be out of flash.
0Bh	PLL Unlocked or Oscillator watchdog overflow occured during programming or erasing the flash.
0Ch	Erase operation failed (phase 2)
FFh	Unknown or bad command

Table 7 : Return values for each programming / erase command

Programming Command	R0	R1	R2	R3	R4-R15
Single or double Word programming	Error code	Unchanged	Data in Flash for location Segment + Segment Offset (R0.[3:0] with R1)	Data in Flash for location Segment + Segment Offset + 2 (R0[3:0] with R1+2)	Unchanged
Block programming	Error code	The last segment offset address of the last written Word in Flash (failing Flash address if R0 is not equal to zero)	Undefined		Unchanged
Erasing	Error code	Undefined			Unchanged
After status read	Error code	Flash embedded rev MSByte = major release LSByte = minor revision	Circuit identifiers : R2 = #0787h R3 = #0101h for this device		Unchanged

Note: The Flash Embedded STEAK Algorithms require at least **50 words** on the Internal System Stack for proper operation. The program itself verifies that there is enough free space on the System Stack before performing a programming or erasing operation, by computing the Word number between Stack Pointer (SP) and Stack Overflow register (STKOV).
The MDH, MDL and MDC register content are modified.
Registers R0 to R4 are used as Input Data for STEAK, and are modified as explained above (Return Values).
Registers R5 to R15 are used internally by STEAK, but preserved on entry and restore on exit of STEAK.
IT IS VERY IMPORTANT TO TAKE INTO ACCOUNT THE FACT THAT STEAK USES UP TO 50 WORDS ON THE SYSTEM STACK. TO PREVENT ANY ABNORMAL SITUATION, IT IS VERY IMPORTANT TO INITIALIZE CORRECTLY THE STACK SIZE TO AT LEAST 64 WORDS, AND TO CORRECTLY INITIALIZE REGISTER STKOV.

5.2 - Programming Examples

Programming a double Word

```
; code shown below assumes that Flash is mapped in segment 1
; ie. bit ROMS1 = ‘1’ in SYSCON register
; Flash must be enabled, ie. bit ROMEN = ‘1’ in SYSCON.
MOV    R0, #0DD40h   ; DD4xh : Double Word programming command
OR     R0, #01h      ; Selects segment 1 in flash memory
MOV    R1, #00224h   ; Address to be programmed is 01’0224h
MOV    R2, #03456h   ; Data to be programmed at 01’0224h
MOV    R3, #04567h   ; Data to be programmed at 01’0226h
MOV    R4, #050d     ; 50ns is 20MHz CPU clock frequency
MOV    R7, #08000h   ; R7 used for Flash trigger sequence
#define FCR 08000h
; Flash Unlock Sequence consists in two consecutive writes, with the direct
addressing mode and then the indirect addressing mode. FCR must represent an
even address in the active address space of the Flash memory, and Rwn can be
any unused Word GPR (R6 to R15)loaded with a value resulting in the same even
address than FCR
EXTS   #1, #2        ; Flash can be mapped in segment 0 or 1
MOV    FCR, R7       ; first part
MOV    [R7], R7      ; second part
NOP                  ; WARNING: place 2 NOP operations after
NOP                  ; the Unlock sequence to avoid all possible
                     ; pipeline conflicts in STEAK programs
```

Note: For easier coding, the standard data paging addressing scheme is overriden for the two MOV instructions of the Flash Trigger Sequence (EXTS instruction). However this coding also locks both standard and PEC interrupts and class A hardware traps. This override can be replaced by an ATOMIC instruction if the standard DPP addressing scheme must be preserved.

Programming a block of data

The following code is provided as an example to program a block of data. Flash to be programmed is from address 01'9000h to 01'9FFEh (included). Source data (data to be copied into flash) is located in external RAM from address 05'1000h (to 05'1FFEh, implicitly) :

```
; code shown below assumes that flash is mapped in segment 1
; ie. bit ROMS1 = '1' in SYSCON register
; Flash must be enabled, ie. bit ROMEN = '1' in SYSCON.
MOV    R0, #0AA50h   ; AA5xh : Multi Word programming command
OR     R0, #01h      ; Selects segment 1 in Flash memory
MOV    R1, #09000h   ; First Flash Segment Offset Address
MOV    R2, #09FFEh   ; Last Flash Segment Offset Address
MOV    R3, #09000h   ; Source data address: use DPP2 as
                     ; data page pointer
SCXT   DPP2,#20d     ; Source is in page 20 (first page of
                     ; segment 5): save previous DPP2 value
                     ; and load it with source page number
MOV    R4, #050d     ; 50ns is 20MHz CPU clock frequency
MOV    R7, #08000h   ; R7 used for Flash trigger sequence
#define FCR 08000h
EXTS   #1, #2        ; Flash can be mapped in segment 0 or 1
MOV    FCR, R7       ; first part
MOV    [R7], R7      ; second part
NOP                  ; WARNING: place 2 NOP operations after
NOP                  ; the Unlock sequence to avoid all possible
                     ; pipeline conflicts in STEAK programs
POP    DPP2          ; restore DPP2
```

5.3 - Flash Memory Configuration

The default memory configuration of the ST10F168 Memory is determined by the state of the $\overline{EA}$ pin at reset. This value is stored in the Internal ROM Enable bit : ROMEN of the SYSCON Register.

When ROMEN = 0, the internal FLASH is disabled and external ROM is used for startup control. Flash memory can be enabled later by setting the ROMEN bit of SYSCON to 1. Ensure that the code which performs this setting is NOT running from external ROM in a segment that will be replaced by FLASH memory, otherwise unexpected behaviour may occur.

For example, if the external ROM code is located in the first 32K Byte of segment 0, the first 32K Byte of the FLASH must then be enabled in segment 1. This is done by setting the ROMS1 bit of SYSCON to 0, before or simultaneously with setting the ROMEN bit. This must be done in the externally supplied program, before the execution of the EINIT instruction. If program execution starts from external memory, but the Flash memory mapped in segment 0 is accessed later, then the code that sets the ROMEN bit must be executed either in segment 0 but above address 00'8000h, or from the internal RAM.

Bit ROMS1 only affects the mapping of the first 32K Byte of the Flash memory. All other parts of the Flash memory (addresses 01'8000h - 04'FFFFh) remain unaffected.

Note: The SGTDIS Segmentation Disable / Enable must also be set to 0 to enable the use of the full 256K Byte of on-chip memory in addition to the external boot memory. The correct procedure for changing the segmentation registers must be observed to prevent an unwanted trap condition :

– Instructions that configure the internal memory must only be executed from external memory or from the internal RAM.
– An Absolute Inter-Segment Jump (JMPS) instruction must be executed after Flash enabling, before the next instruction, even if the next instruction is located in the consecutive address.
– Whenever the internal memory is disabled, enabled or remapped, the DPPs must be explicitly (re)loaded to enable correct data accesses to the internal memory and / or external memory.

5.4 - Flash Protection

If Flash Protection is active, data operands in the on-chip Flash Memory area can only be read by a program executed from the Flash Memory itself. Program branches from or into the on-chip Flash memory are possible in the Flash protection mode. Erasing and programming of the Flash memory is not possible as long as protection is active.

Flash protection is controlled by the Protection UPROM Programming Bit (UPROG). UPROG is a 'hidden' one-time programmable bit only accessible in a special mode which can be entered via a Flash EPROM programming board for example. If UPROG is set to "1", Flash protection is active after reset. By default Flash Protection is disabled (UPROG=0).

When flash protection is active (the default after reset if UPROG bit is set), then any read access in the flash by a code executed from external or internal RAM (IRAM or XRAM) will return the value 0B88Bh. Any call of STEAK will return the error code '01' (Protected flash).

Normally Flash protection should never be deactivated, once activated. If this has to be done, for example because the Flash memory has to be reprogrammed with updated program / variables, a zero value has to be written at any even address in the active address space of the Flash memory. This write can be done only by an instruction executed from the internal Flash Memory itself.
For example:

```
MOV FLASH,ZEROS ; Deactivate Flash
Protection.

; Flash is any even address in Flash
memory space. This instruction MUST
be executed from Flash memory itself.
```

After this instruction, the flash is temporarily de-protected, thus any read access of the flash from code executed from external memory or internal RAMs will be correctly executed, and calls of STEAK can be correctly performed (programming, erasing or status reading).

Note: 1. That all STEAK commands re-activate the flash protection if bit UPROG is set when completed.

5.5 - Bootstrap Loader Mode

Pin P0L.4 (BSL) activates the on-chip bootstrap loader, when low during hardware reset. The bootstrap loader allows moving the start code into the internal RAM of the ST10F168 via the serial interface ASC0. The ST10F168 will remain in bootstrap loader mode until a hardware reset with P0L.4 high or a software reset occurs. The bootstraps loader acknowledge byte is D5h.

6 - CENTRAL PROCESSING UNIT (CPU)

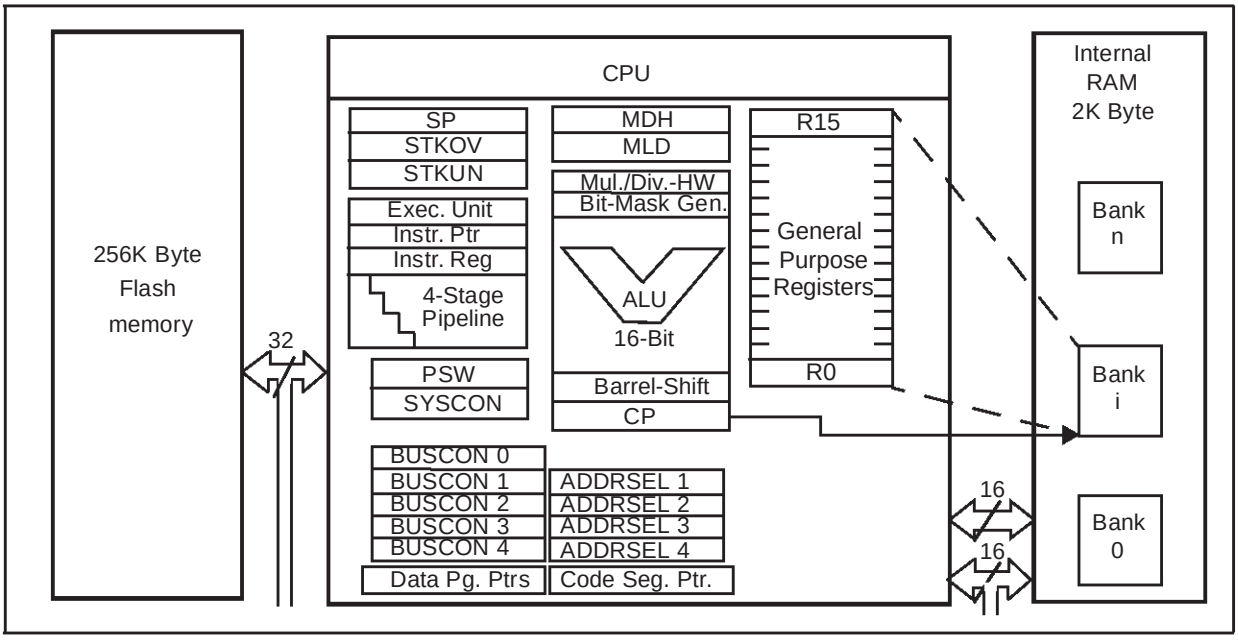
The CPU includes a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been added for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Most of the ST10F168's instructions can be executed in one instruction cycle which requires 62.5ns at 32MHz CPU clock. For example, shift and rotate instructions are processed in one instruction cycle independent of the number of bit to be shifted. Multiple-cycle instructions have been optimized: branches are carried out in 2 cycles, 16 x 16-bit multiplication in 5 cycles and a 32/16 bit division in 10 cycles.The jump cache reduces the execution time of repeatedly performed jumps in a loop, from 2 cycles to 1 cycle.

The CPU uses a bank of 16 word registers to run the current context. This bank of General Purpose Registers (GPR) is physically stored within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, one register bank may overlap others.

A system stack of up to 2048 Byte stores temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value on each stack access, for the detection of a stack overflow or underflow.

Figure 5 : CPU Block Diagram



6.1 - Instruction Set Summary

The Table 8 lists the instructions of the ST10F168. The various addressing modes, instruction operation, parameters for conditional execution of instructions, opcodes and a detailed description of each instruction can be found in the “ST10 Family Programming Manual”.

Table 8 : Instruction set summary

Mnemonic	Description	Bytes
ADD(B)	Add Word (Byte) operands	2 / 4
ADDC(B)	Add Word (Byte) operands with Carry	2 / 4
SUB(B)	Subtract Word (Byte) operands	2 / 4
SUBC(B)	Subtract Word (Byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16 x 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16 / 16-bit)	2
DIVL(U)	(Un)Signed long divide register MD by direct GPR (32 / 16-bit)	2
CPL(B)	Complement direct Word (Byte) GPR	2
NEG(B)	Negate direct Word (Byte) GPR	2
AND(B)	Bitwise AND, (Word / Byte operands)	2 / 4
OR(B)	Bitwise OR, (Word / Byte operands)	2 / 4
XOR(B)	Bitwise XOR, (Word / Byte operands)	2 / 4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND / OR / XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bitwise modify masked high / low Byte of bit-addressable direct Word memory with immediate data	4
CMP(B)	Compare Word (Byte) operands	2 / 4
CMPD1/2	Compare Word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare Word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct Word GPR and store result in direct Word GPR	2
SHL/SHR	Shift left / right direct Word GPR	2
ROL/ROR	Rotate left / right direct Word GPR	2
ASHR	Arithmetic (sign bit) shift right direct Word GPR	2
MOV(B)	Move Word (Byte) data	2 / 4
MOVBS	Move Byte operand to Word operand with sign extension	2 / 4
MOVBZ	Move Byte operand to Word operand. with zero extension	2 / 4
JMPA, JMPI, JMPR	Jump absolute / indirect / relative if condition is met	4
JMPS	Jump absolute to a code segment	4
J(N)B	Jump relative if direct bit is (not) set	4
JBC	Jump relative and clear bit if direct bit is set	4

Table 8 : Instruction set summary

Mnemonic	Description	Bytes
JNBS	Jump relative and set bit if direct bit is not set	4
CALLA, CALLI, CALLR	Call absolute / indirect / relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct Word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH, POP	Push / pop direct Word register onto / from system stack	2
SCXT	Push direct Word register onto system stack and update register with Word operand	4
RET	Return from intra-segment subroutine	2
RETS	Return from inter-segment subroutine	2
RETP	Return from intra-segment subroutine and pop direct Word register from system stack	2
RETI	Return from interrupt service subroutine	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes $\overline{\text{NMI}}$-pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT	Disable Watchdog Timer	4
EINIT	Signify End-of-Initialization on $\overline{\text{RSTOUT}}$-pin	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4
NOP	Null operation	2

7 - EXTERNAL BUS CONTROLLER

All external memory accesses are performed by the on-chip external bus controller. The EBC can be programmed to single chip mode when no external memory is required, or to one of four different external memory access modes :

– 16 / 18 / 20 / 24-bit addresses and 16-bit data, demultiplexed.
– 16 / 18 / 20 / 24-bit addresses and 16-bit data, multiplexed.
– 16 / 18 / 20 / 24-bit addresses and 8-bit data, multiplexed.
– 16 / 18 / 20 / 24-bit addresses and 8-bit data, demultiplexed.

In demultiplexed bus modes addresses are output on Port1 and data are input / output on Port0 or P0L, respectively. In the multiplexed bus modes both addresses and data use Port0 for input / output.

Timing characteristics of the external bus interface (memory cycle time, memory tri-state time, length of ALE and read / write delay) are programmable giving the choice of a wide range of memories and external peripherals. Up to 4 independent address windows may be defined (using register pairs ADDRSELx / BUSCONx) to access different resources and bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0. Up to 5 external $\overline{CS}$ signals (4 windows plus default) can be generated in order to save external glue logic. Access to very slow memories is supported by a 'Ready' function.

A $\overline{HOLD}$/$\overline{HLDA}$ protocol is available for bus arbitration which shares external resources with other bus masters. The bus arbitration is enabled by setting bit HLDEN in register SYSCON. After setting HLDEN once, pins P6.7...P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In master mode (default after reset) the $\overline{HLDA}$ pin is an output. By setting bit DP6.7 to'1' the slave mode is selected where pin $\overline{HLDA}$ is switched to input. This directly connects the slave controller to another master controller without glue logic.

For applications which require less external memory space, the address space can be restricted to 1M Byte, 256K Byte or to 64K Byte. Port4 outputs all 8 address lines if an address space of 16M Byte is used, otherwise four, two or no address lines.

Chip select timing can be programmed. By default (after reset), the CSx lines change half a CPU clock cycle after the rising edge of ALE. With the CSCFG bit set in the SYSCON register the CSx lines can change with the rising edge of ALE.

The active level of the READY pin can be set by bit RDYPOLx in the BUSCONx registers. When the READY function is enabled for a specific address window, each bus cycle within the window must be terminated with the active level defined by bit RDYPOLx in the associated BUSCONx register.

8 - INTERRUPT SYSTEM

The interrupt response time for internal program execution is from 157ns to 375ns at 32MHz CPU clock.

The ST10F168 architecture supports several mechanisms for fast and flexible response to service requests that can be generated from various sources (internal or external) to the microcontroller. Any of these interrupt requests can be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single Byte or Word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited to perform the transmission or the reception of blocks of data. The ST10F168 has 8 PEC channels, each of them offers such fast interrupt-driven data transfer capabilities.

A interrupt control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield is dedicated to each existing interrupt source. Thanks to its related register, each source can be programmed to one of sixteen interrupt priority levels. Once starting to be processed by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges). Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number. Table 9 shows all the available ST10F168 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers:

Table 9 : Interrupt sources

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Register 0	CC0IR	CC0IE	CC0INT	00'0040h	10h
CAPCOM Register 1	CC1IR	CC1IE	CC1INT	00'0044h	11h
CAPCOM Register 2	CC2IR	CC2IE	CC2INT	00'0048h	12h
CAPCOM Register 3	CC3IR	CC3IE	CC3INT	00'004Ch	13h
CAPCOM Register 4	CC4IR	CC4IE	CC4INT	00'0050h	14h
CAPCOM Register 5	CC5IR	CC5IE	CC5INT	00'0054h	15h
CAPCOM Register 6	CC6IR	CC6IE	CC6INT	00'0058h	16h
CAPCOM Register 7	CC7IR	CC7IE	CC7INT	00'005Ch	17h
CAPCOM Register 8	CC8IR	CC8IE	CC8INT	00'0060h	18h
CAPCOM Register 9	CC9IR	CC9IE	CC9INT	00'0064h	19h
CAPCOM Register 10	CC10IR	CC10IE	CC10INT	00'0068h	1Ah
CAPCOM Register 11	CC11IR	CC11IE	CC11INT	00'006Ch	1Bh
CAPCOM Register 12	CC12IR	CC12IE	CC12INT	00'0070h	1Ch
CAPCOM Register 13	CC13IR	CC13IE	CC13INT	00'0074h	1Dh
CAPCOM Register 14	CC14IR	CC14IE	CC14INT	00'0078h	1Eh
CAPCOM Register 15	CC15IR	CC15IE	CC15INT	00'007Ch	1Fh
CAPCOM Register 16	CC16IR	CC16IE	CC16INT	00'00C0h	30h
CAPCOM Register 17	CC17IR	CC17IE	CC17INT	00'00C4h	31h

Table 9 : Interrupt sources (continued)

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Register 18	CC18IR	CC18IE	CC18INT	00'00C8h	32h
CAPCOM Register 19	CC19IR	CC19IE	CC19INT	00'00CCh	33h
CAPCOM Register 20	CC20IR	CC20IE	CC20INT	00'00D0h	34h
CAPCOM Register 21	CC21IR	CC21IE	CC21INT	00'00D4h	35h
CAPCOM Register 22	CC22IR	CC22IE	CC22INT	00'00D8h	36h
CAPCOM Register 23	CC23IR	CC23IE	CC23INT	00'00DCh	37h
CAPCOM Register 24	CC24IR	CC24IE	CC24INT	00'00E0h	38h
CAPCOM Register 25	CC25IR	CC25IE	CC25INT	00'00E4h	39h
CAPCOM Register 26	CC26IR	CC26IE	CC26INT	00'00E8h	3Ah
CAPCOM Register 27	CC27IR	CC27IE	CC27INT	00'00ECh	3Bh
CAPCOM Register 28	CC28IR	CC28IE	CC28INT	00'00F0h	3Ch
CAPCOM Register 29	CC29IR	CC29IE	CC29INT	00'0110h	44h
CAPCOM Register 30	CC30IR	CC30IE	CC30INT	00'0114h	45h
CAPCOM Register 31	CC31IR	CC31IE	CC31INT	00'0118h	46h
CAPCOM Timer 0	T0IR	T0IE	T0INT	00'0080h	20h
CAPCOM Timer 1	T1IR	T1IE	T1INT	00'0084h	21h
CAPCOM Timer 7	T7IR	T7IE	T7INT	00'00F4h	3Dh
CAPCOM Timer 8	T8IR	T8IE	T8INT	00'00F8h	3Eh
GPT1 Timer 2	T2IR	T2IE	T2INT	00'0088h	22h
GPT1 Timer 3	T3IR	T3IE	T3INT	00'008Ch	23h
GPT1 Timer 4	T4IR	T4IE	T4INT	00'0090h	24h
GPT2 Timer 5	T5IR	T5IE	T5INT	00'0094h	25h
GPT2 Timer 6	T6IR	T6IE	T6INT	00'0098h	26h
GPT2 CAPREL Register	CRIR	CRIE	CRINT	00'009Ch	27h
A/D Conversion Complete	ADCIR	ADCIE	ADCINT	00'00A0h	28h
A/D Overrun Error	ADEIR	ADEIE	ADEINT	00'00A4h	29h
ASC0 Transmitter	S0TIR	S0TIE	S0TINT	00'00A8h	2Ah
ASC0 Transmitter Buffer	S0TBIR	S0TBIE	S0TBINT	00'011Ch	47h
ASC0 Receiver	S0RIR	S0RIE	S0RINT	00'00ACh	2Bh
ASC0 Error	S0EIR	S0EIE	S0EINT	00'00B0h	2Ch
SSC Transmitter	SCTIR	SCTIE	SCTINT	00'00B4h	2Dh
SSC Receiver	SCRIR	SCRIE	SCRINT	00'00B8h	2Eh
SSC Error	SCEIR	SCEIE	SCEINT	00'00BCh	2Fh
PWM Channel 0...3	PWMIR	PWMIE	PWMINT	00'00FCh	3Fh
CAN Interface	XP0IR	XP0IE	XP0INT	00'0100h	40h
X-Peripheral Node	XP1IR	XP1IE	XP1INT	00'0104h	41h
X-Peripheral Node	XP2IR	XP2IE	XP2INT	00'0108h	42h
PLL Unlock	XP3IR	XP3IE	XP3INT	00'010Ch	43h

Hardware traps are exceptions or error conditions that arise during run-time. They cause immediate non-maskable system reaction similar to a standard interrupt service (branching to a dedicated vector table location).

The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any other program execution.

Hardware trap services cannot not be interrupted by standard interrupt or by PEC interrupts.

Table 10 shows all of the possible exceptions or error conditions that can arise during run-time :

Table 10 : Exceptions or error conditions that can arise during run-time

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Priority
Reset Functions					
Hardware Reset		RESET	00'0000h	00h	III
Software Reset		RESET	00'0000h	00h	III
Watchdog Timer Overflow		RESET	00'0000h	00h	III
Class A Hardware Traps					
Non-Maskable Interrupt	NMI	NMITRAP	00'0008h	02h	II
Stack Overflow	STKOF	STOTRAP	00'0010h	04h	II
Stack Underflow	STKUF	STUTRAP	00'0018h	06h	II
Class B Hardware Traps					
Undefined Opcode	UNDOPC	BTRAP	00'0028h	0Ah	I
Protected Instruction Fault	PRTFLT	BTRAP	00'0028h	0Ah	I
Illegal Word Operand Access	ILLOPA	BTRAP	00'0028h	0Ah	I
Illegal Instruction Access	ILLINA	BTRAP	00'0028h	0Ah	I
Illegal External Bus Access	ILLBUS	BTRAP	00'0028h	0Ah	I
Reserved			[2Ch –3Ch]	[0Bh – 0Fh]	
Software Traps TRAP Instruction			Any [00'0000h– 00'01FCh] in steps of 4h	Any [00h – 7Fh]	Current CPU Priority

9 - CAPTURE / COMPARE (CAPCOM) UNIT

The ST10F168 has two 16 channel CAPCOM units which support generation and control of timing sequences on up to 32 channels with a maximum resolution of 320ns at 32MHz CPU clock.

The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Four 16-bit timers (T0/T1, T7/T8) with reload registers provide two independent time bases for the capture / compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow / underflow of timer T6 in module GPT2.

This provides a wide range of variation for the timer period and resolution and allows precise adjustments to application specific requirements. In addition, external count inputs for CAPCOM timers T0 and T7 allow event scheduling for the capture / compare registers relative to external events.

Each of the two capture / compare register arrays contain 16 dual purpose capture / compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1 (T7 or T8, respectively), and programmed for capture or compare functions. Each register has one associated port pin which serves as an input pin for triggering the capture function, or as an output pin (except for CC24...CC27) to indicate the occurrence of a compare event.

When a capture / compare register has been selected for capture mode, the current contents of the allocated timer will be latched (captured) into the dedicated capture / compare register in response to an external event at the corresponding port pin which is associated with this register. In addition, a specific interrupt request for this capture / compare register is generated.

Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all the registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture / compare register, specific actions will be taken based on the selected compare mode.

The input frequencies f_{Tx}, for the timer input selector Txl, are determined as a function of the CPU clock. The timer input frequencies, the resolution and the periods which result from the selected pre-scaler option in Txl when using a 25MHz CPU clock are listed in the Table 12.

The numbers of the timer periods are based on a reload value of 0000h. Note that some numbers are rounded to 3 significant figures.

Table 11 : Compare Modes

Compare Modes	Function
Mode 0	Interrupt-only compare mode ; several compare interrupts per timer period are possible.
Mode 1	Pin toggles on each compare match ; several compare events per timer period are possible.
Mode 2	Interrupt-only compare mode ; only one compare interrupt per timer period is generated.
Mode 3	Pin set ‘1’ on match; pin reset ‘0’ on compare time overflow ; only one compare event per timer period is generated.
Double Register Mode	Two registers operate on one pin; pin toggles on each compare match ; several compare events per timer period are possible.

Table 12 : CAPCOM timer input frequencies, resolution and periods

f_{CPU} = 25MHz	Timer Input Selection TxI							
	000b	**001b**	**010b**	**011b**	**100b**	**101b**	**110b**	**111b**
f_{CPU} pre-scaler	8	16	32	64	128	256	512	1024
Input Frequency	3.125MHz	1.56MHz	781KHz	391KHz	195KHz	97.7KHz	48.8KHz	24.4KHz
Resolution	320ns	640ns	1.28µs	2.56µs	5.12µs	10.24µs	20.48µs	40.96µs
Period	21.0ms	41.9ms	83.9ms	167ms	336ms	671ms	1.34s	2.68s

Table 13 : CAPCOM Channels Pin Assignement

CAPCOM Unit	**Channel**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
CAPCOM1	I/O	CC0	CC1	CC2	CC3	CC4	CC5	CC6	CC7	CC8[1]	CC9[1]	CC10[1]	CC11[1]	CC12	CC13	CC14	CC15
	Port	2.0	2.1	2.2	2.3	2.4	2.5	2.6	2.7	2.8	2.9	2.10	2.11	2.12	2.13	2.14	2.15
	Pin Number	47	48	49	50	51	52	53	54	57	58	59	60	61	62	63	64
CAPCOM2	I/O	CC16	CC17	CC18	CC19	CC20	CC21	CC22	CC23	CC24	CC25	CC26	CC27	CC28	CC29	CC30	CC31
	Port	8.0	8.1	8.2	8.3	8.4	8.5	8.6	8.7	1H.4	1H.5	1H.6	1H.7	7.4	7.5	7.6	7.7
	Pin Number	9	10	11	12	13	14	15	16	132	133	134	135	23	24	25	26

Note: 1. Input only.

10 - GENERAL PURPOSE TIMER UNIT

The GPT unit is a flexible multifunctional timer / counter structure which is used for time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication. The GPT unit contains five 16-bit timers organized into two separate modules GPT1 and GPT2. Each timer in each module may operate independently in several different modes, or may be concatenated with another timer of the same module.

10.1 - GPT1

Each of the three timers T2, T3, T4 of the GPT1 module can be configured individually for one of four basic modes of operation: **timer**, **gated timer**, **counter mode and incremental interface mode**. In timer mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler. In counter mode, the timer is clocked in reference to external events. Pulse width or duty cycle measurement is supported in gated timer mode where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input.

Table 14 lists the timer input frequencies, resolution and periods for each pre-scaler option at 25MHz CPU clock. This also applies to the Gated Timer Mode of T3 and to the auxiliary timers T2 and T4 in Timer and Gated Timer Mode.

The count direction (up / down) for each timer is programmable by software or may be altered dynamically by an external signal on a port pin (TxEUD).

In Incremental Interface Mode, the GPT1 timers (T2, T3, T4) can be connected directly to the incremental position sensor signals A and B by their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals so that the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has output toggle latches (TxOTL) which changes state on each timer over-flow / under-flow. The state of this latch may be output on port pins (TxOUT) e. g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for high resolution of long duration measurements.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

10.2 - GPT2

The GPT2 module provides precise event control and time measurement. It includes two timers (T5, T6) and a capture / reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The count direction (up / down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6 which changes its state on each timer overflow / underflow.

Table 14 : GPT1 timer input frequencies, resolution and periods

f_{CPU} = 25MHz	Timer Input Selection T2I / T3I / T4I							
	000b	**001b**	**010b**	**011b**	**100b**	**101b**	**110b**	**111b**
Pre-scaler Factor	8	16	32	64	128	256	512	1024
Input Frequency	3.125MHz	1.563MHz	781.3MHz	390KHz	195.3KHz	97.66KHz	48.83KHz	24.41KHz
Resolution	320ns	640ns	1.28µs	2.56µs	5.12µs	10.24µs	20.48µs	40.96µs
Period	21.0ms	41.9ms	83.9ms	167ms	336ms	671ms	1.34s	2.68s

The state of this latch may be used to clock timer T5, or it may be output on a port pin (T6OUT).

The overflows / underflows of timer T6 can also be used to clock the CAPCOM timers T0 or T1, and to cause a reload from the CAPREL register.

The CAPREL register can capture the contents of T5 from an external signal transition on the corresponding port pin (CAPIN), and T5 may be optionally cleared after the capture procedure. This allows absolute time differences to be measured or pulse multiplication to be performed without software overhead.

The capture trigger (timer T5 to CAPREL) may also be generated on transitions of GPT1 timer T3 inputs T3IN and / or T3EUD. This is useful when T3 operates in Incremental Interface Mode.

Table 15 GPT2 timer input frequencies, resolution and periods lists the timer input frequencies, resolution and periods for each pre-scaler option at 25MHz CPU clock. This also applies to the Gated Timer Mode of T6 and to the auxiliary timer T5 in Timer and Gated Timer Mode.

Table 15 : GPT2 timer input frequencies, resolution and periods

f_{CPU} = 25MHz	Timer Input Selection T5I / T6I							
	000b	**001b**	**010b**	**011b**	**100b**	**101b**	**110b**	**111b**
Pre-scaler Factor	4	8	16	32	64	128	256	512
Input Frequency	6.25MHz	3.125MHz	1.563MHz	781.3KHz	390KHz	195.3KHz	97.66KHz	48.83KHz
Resolution	160ns	320ns	640ns	1.28µs	2.56µs	5.12µs	10.24µs	20.48µs
Period	10.49ms	21.0ms	41.9ms	83.9ms	167ms	336ms	671ms	1.34s

Figure 6 : Block Diagram of GPT1

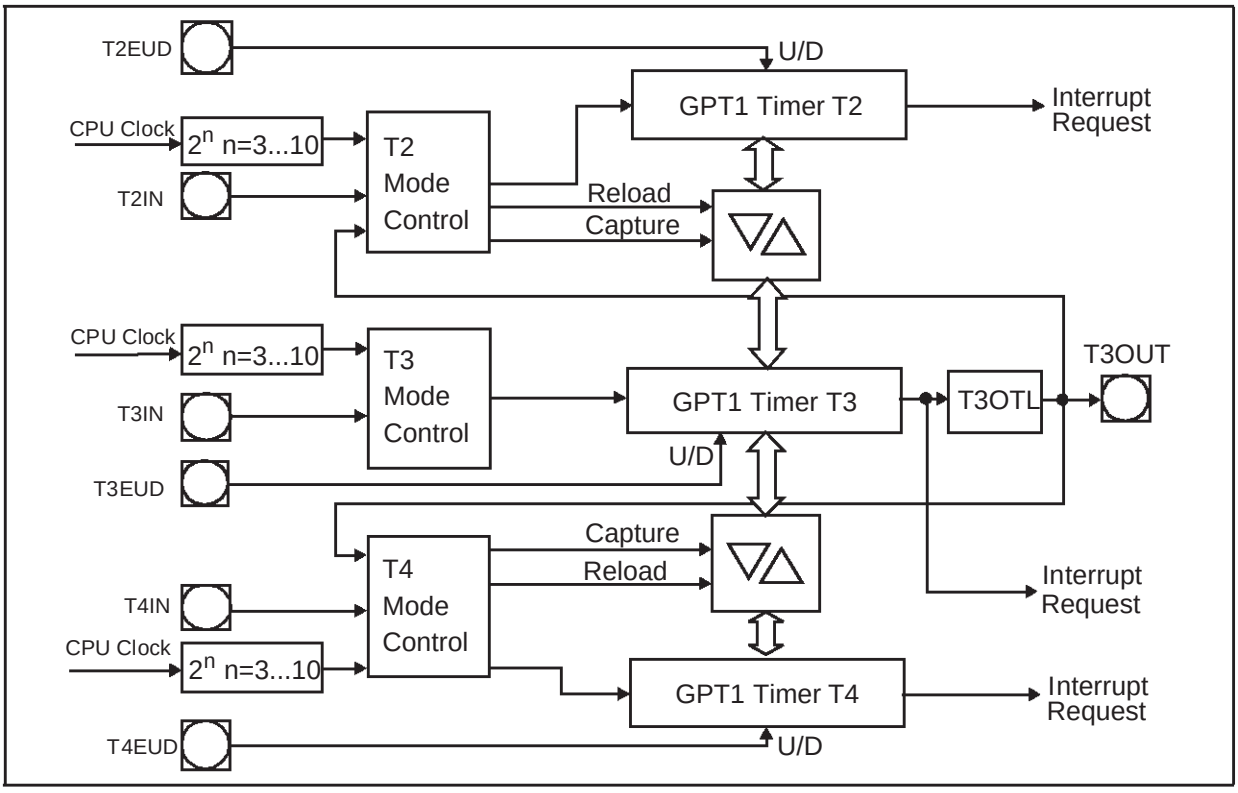
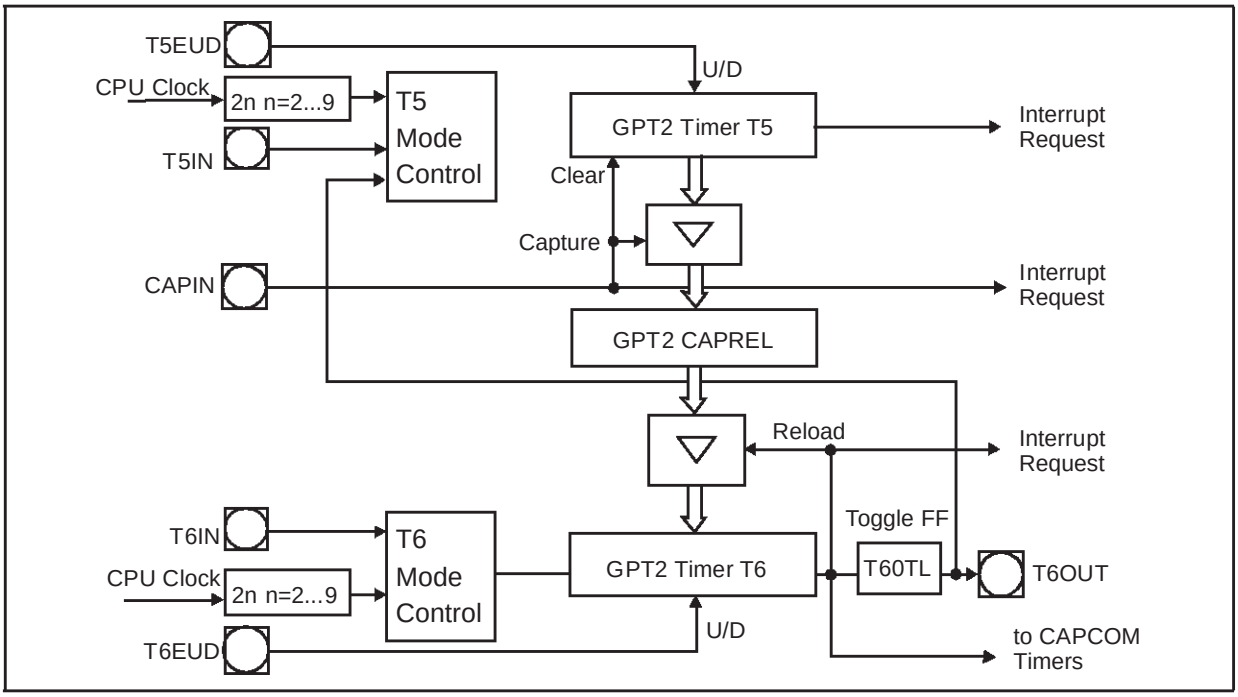


Figure 7 : Block Diagram of GPT2



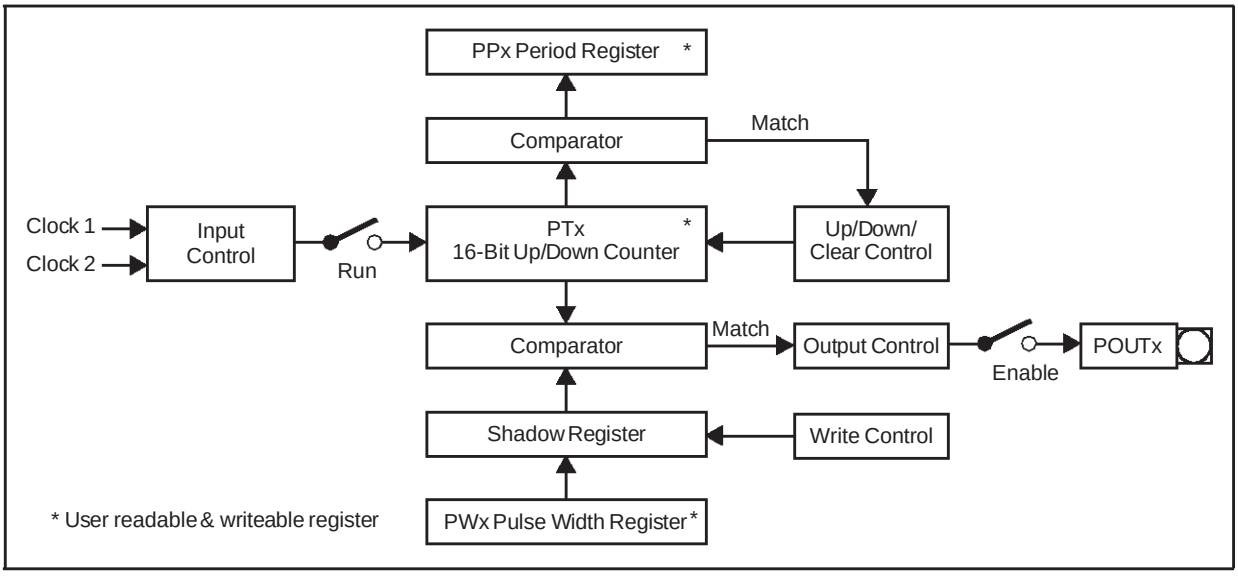
11 - PWM MODULE

The pulse width modulation module can generate up to four PWM output signals using edge-aligned or centre-aligned PWM. In addition, the PWM module can generate PWM burst signals and single shot outputs. The Table 16 shows the PWM frequencies for different resolutions. The level of the output signals is selectable and the PWM module can generate interrupt requests.

Table 16 : PWM unit frequencies and resolution at 25MHz CPU clock

Mode 0	**Resolution**	**8-bit**	**10-bit**	**12-bit**	**14-bit**	**16-bit**
CPU Clock / 1	40ns	97.66KHz	24.41KHz	6.104KHz	1.526KHz	0.381Hz
CPU Clock / 64	2.56µs	1.526KHz	381.5Hz	95.37Hz	23.84Hz	5.96Hz
Mode 1	**Resolution**	**8-bit**	**10-bit**	**12-bit**	**14-bit**	**16-bit**
CPU Clock / 1	40ns	48.82KHz	12.20KHz	3.05KHz	762.9Hz	190.7Hz
CPU Clock / 64	2.56µs	762.9Hz	190.7Hz	47.68Hz	11.92Hz	2.98Hz

Figure 8 : PWM Module Block Diagram



12 - PARALLEL PORTS

The ST10F168 provides up to 111 I/O lines organized into eight input / output ports and one input port. All port lines are bit-addressable, and all input / output lines are individually (bit-wise) programmable as input or output via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of five I/O ports can be configured (pin by pin) for push-pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

The input threshold of Port 2, Port 3, Port 7 and Port 8 is selectable (TTL or CMOS-like), where the special CMOS-like input threshold reduces noise sensitivity to the input hysteresis. The input thresholds are selected with bit of PICON register dedicated to blocks of 8 input pins (2-bit for Port2, 2-bit for Port3, 1-bit for Port7, 1-bit for Port8).

All pins of I/O ports also support an alternate programmable function:

– Port0 and Port1 may be used as address and data lines when accessing external memory.

– Port 2, Port 7 and Port 8 are associated with the capture inputs or with the compare outputs of the CAPCOM units and / or with the outputs of the PWM module.

– Port 3 includes the alternate functions of timers, serial interfaces, the optional bus control signal $\overline{BHE}$ and the system clock output (CLKOUT).

– Port 4 outputs the additional segment address bit A16 to A23 in systems where segmentation is enabled to access more than 64K Byte of memory.

– Port 5 is used as analog input channels of the A/D converter or as timer control signals.

– Port 6 provides optional bus arbitration signals ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) and chip select signals.

All port lines that are not used for alternate functions may be used as general purpose I/O lines.

13 - A/D CONVERTER

A10-bit A/D converter with 16 multiplexed input channels and a sample and hold circuit is integrated on-chip. The sample time (for loading the capacitors) and the conversion time is programmable and can be adjusted to the external circuitry.

Overrun error detection / protection is controlled by the ADDAT register. Either an interrupt request is generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended until the previous result has been read. For applications which require less than 16 analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the ST10F168 supports different conversion modes :

– **Single channel single conversion** : the analog level of the selected channel is sampled once and converted. The result of the conversion is stored in the ADDAT register.

– **Single channel continuous conversion** : the analog level of the selected channel is repeatedly sampled and converted. The result of the conversion is stored in the ADDAT register.

– **Auto scan single conversion** : the analog level of the selected channels are sampled once and converted. After each conversion the result is stored in the ADDAT register. The data can be transfered to the RAM by interrupt software management or using the powerfull Peripheral Event Controller data transfert.

– **Auto scan continuous conversion** : the analog level of the selected channels are repeatedly sampled and converted. The result of the conversion is stored in the ADDAT register. The data can be transfered to the RAM by interrupt software management or using the powerfull Peripheral Event Controller data transfert.

– **Wait for ADDAT read mode** : when using continuous modes, in order to avoid to overwrite the result of the current conversion by the next one, the ADWR bit of ADCON control register must be activated. Then, until the ADDAT register is read, the new result is stored in a temporary buffer and the conversion is on hold.

– **Channel injection mode** : when using continuous modes, a selected channel can be converted in between without changing the current operating mode. The 10 bit data of the conversion are stored in ADRES field of ADDAT2. The current continuous mode remains active after the single conversion is completed.

The Table 17 ADC sample clock and conversion clock shows conversion clock and sample clock of the ADC unit. A complete conversion will take $14t_{CC} + 2t_{SC} + 4TCL$. This time includes the conversion it self, the sampling time and the time required to transfer the digital value to the result register. For example at 25MHz of CPU clock, the minimum complete conversion time is 7.76µs.

The A/D converter provides automatic offset and linearity self calibration. The calibration operation is performed in two ways :

– A full calibration sequence is performed after a reset and lasts 1.25ms minimum (at 25MHz CPU clock). During this time, the ADBSY flag is set to indicate the operation. Normal conversion can be performed during this time. The duration of the calibration sequence is then extended by the time consumed by the conversions.
Note : After a power-on reset, the total unadjusted error (TUE) of the ADC might be worse than ±2LSB (max. ±4LSB). During the full calibration sequence, the TUE is constantly improved until at the end of the cycle, TUE is within the specified limits of ±2LSB.

– One calibration cycle is performed after each conversion : each calibration cycle takes 4 ADC clock cycles. These operation cycles ensure constant updating of the ADC accuracy, compensating changing operating conditions.

Table 17 : ADC sample clock and conversion clock

ADCTC	Conversion Clock t_{CC}		ADSTC	Sample Clock t_{SC}	
	TCL[1] = 1/2 x f_{XTAL}	At f_{CPU} = 25MHz		t_{SC} =	At f_{CPU} = 25MHz
00	TCL x 24	0.48µs	00	t_{CC}	0.48µs [2]
01	Reserved, do not use	Reserved	01	t_{CC} x 2	0.96µs [2]
10	TCL x 96	1.92µs	10	t_{CC} x 4	1.92µs [2]
11	TCL x 48	0.96µs	11	t_{CC} x 8	3.84µs [2]

Notes: 1. See Section 20.5.5 - Direct Drive on page 55.
2. t_{CC} = TCL x 24.

14 - SERIAL CHANNELS

Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by two serial interfaces: the asynchronous / synchronous serial channel (ASC0) and the high-speed synchronous serial channel (SSC).

Two dedicated Baud rate generators set up all standard Baud rates without the requirement of oscillator tuning. For transmission, reception and erroneous reception, 3 separate interrupt vectors are provided for each serial channel.

ASC0

ASC0 supports full-duplex asynchronous communication at up to 781.25K Baud and half-duplex synchronous communication up to 5M Baud at 25MHz system clock.

For asynchronous operation, the Baud rate generator provides a clock with 16 times the rate of the established Baud rate.

Table 18 lists various commonly used Baud rates together with the required reload values and the deviation errors compared to the intended Baud rate.

For synchronous operation, the Baud rate generator provides a clock with 4 times the rate of the established Baud rate.

Table 18 : Commonly used Baud rates by reload value and deviation errors

S0BRS = '0', f_{CPU} = 25MHz			S0BRS = '1', f_{CPU} = 25MHz		
Baud Rate (Baud)	**Deviation Error**	**Reload Value**	**Baud Rate (Baud)**	**Deviation Error**	**Reload Value**
781 250	±0.0%	0000h	520 833	±0.0%	0000h
56 000	+7.3% / -0.4%	000Ch / 000Dh	56 000	+3.3% / -7.0%	0008h / 0009h
38 400	+1.7% / -3.1%	0013h / 0014h	38 400	+4.3% / -3.1%	000Ch / 000Dh
19 200	+1.7% / -0.8%	0027h / 0028h	19 200	+0.5% / -3.1%	001Ah / 001Bh
9 600	+0.5% / -0.8%	0050h/ 0051h	9 600	+0.5% / -1.4%	0035h / 0036h
4 800	+0.5% / -0.1%	00A1h / 00A2h	4 800	+0.5% / -0.5%	006Bh / 006Ch
2 400	+0.2% / -0.1%	0144h / 0145h	2 400	+0.0% / -0.5%	00D8h / 00D9h
1 200	+0.0% / -0.1%	028Ah / 028Bh	1 200	+0.0% / -0.2%	01B1h / 01B2h
600	+0.0% / -0.1%	0515h / 0516h	600	+0.0% / -0.1%	0363h / 0364h
95	+0.4%	1FFFh / 1FFFh	75	+0.0% / -0.0%	1B1Fh / 1B20h
			63	+0.9%	1FFFh / 1FFFh

High Speed Synchronous Serial Channel (SSC)

The High-Speed Synchronous Serial Interface SSC provides flexible high-speed serial communication between the ST10F168 and other microcontrollers, microprocessors or external peripherals. The SSC supports full-duplex and half-duplex synchronous communication; The serial clock signal can be generated by the SSC itself (master mode) or be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable.

This allows communication with SPI-compatible devices. Transmission and reception of data is double-buffered. A 16-bit Baud rate generator provides the SSC with a separate serial clock signal. The serial channel SSC has its own dedicated 16-bit Baud rate generator with 16-bit reload capability, allowing Baud rate generation independent from the timers.

SSCBR is the dual-function Baud rate Generator / Reload register. Table 19 lists some possible Baud rates against the required reload values and the resulting bit times for a 25MHz CPU clock.

Note: The deviation errors given in the Table 18 are rounded. To avoid deviation errors use a Baud rate crystal (providing a multiple of the ASC0/SSC sampling frequency).

Table 19 : Synchronous Baud rate and reload values

Baud Rate	Bit Time	Reload Value
Reserved use a reload value > 0.	---	0000h
5M Baud	200ns	0001h
3.3M Baud	303ns	0002h
2.5M Baud	400ns	0004h
2M Baud	500ns	0005h
1M Baud	1µs	000Bh
100K Baud	10µs	007Ch
10K Baud	100µs	04E1h
1K Baud	1ms	30D3h
190.7 Baud	5.2ms	FFFFh

15 - CAN MODULE

The integrated CAN module completely handles the autonomous transmission and the reception of CAN frames according to the CAN specification V2.0 part B (active). The on-chip CAN module can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

The CAN Module Provides full CAN functionality on up to 15 message objects. Message object 15 can be configured for basic CAN functionality. Both modes provide separate masks for acceptance filtering, allowing a number of identifiers in full CAN mode to be accepted and disregarding a number of identifiers in basic CAN mode. All message objects can be updated independently from other objects and are equipped for the maximum message length of 8 Bytes.

The bit timing is derived from the XCLK and is programmable up to a data rate of 1M Baud. The CAN module uses two pins to interface to a bus transceiver.

16 - WATCHDOG TIMER

The Watchdog Timer is a fail-safe mechanism which prevents the microcontroller from malfunctioning for long periods of time.

The Watchdog Timer is always enabled after a reset of the chip and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed.

Therefore, the chip start-up procedure is always monitored. The software must be designed to service the watchdog timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the watchdog timer overflows and generates an internal hardware reset. It pulls the $\overline{\text{RSTOUT}}$ pin low in order to allow external hardware components to be reset.

The Watchdog Timer is 16-bit, clocked with the system clock divided by 2 or 128. The high Byte of the watchdog timer register can be set to a pre-specified reload value (stored in WDTREL). Each time it is serviced by the application software, the high Byte of the watchdog timer is reloaded. *For security, rewrite WDTCON each time before the watchdog timer is serviced.*

Table 20 shows the watchdog time range for 25MHz CPU clock.

Table 20 : Watchdog time range (25MHz clock)

Reload value in WDTREL	Prescaler for f_{CPU}	
	2 (WDTIN = '0')	128 (WDTIN = '1')
FFh	20.48µs	1.31ms
00h	5.24ms	336ms

17 - SYSTEM RESET

Table 21 : Reset event definition

Reset Source	Short-cut	Conditions
Power-on reset	PONR	Power-on
Long Hardware reset (synchronous & asynchronous)	LHWR	t_{RSTIN} > 1032 TCL
Short Hardware reset (synchronous reset)	SHWR	4 TCL < t_{RSTIN} ≤ 1032 TCL
Watchdog Timer reset	WDTR	WDT overflow
Software reset	SWR	SRST execution

System reset initializes the MCU in a predefined state. There are five ways to activate a reset state. The system start-up configuration is different for each case as shown in Table 21.

17.1 - Asynchronous Reset (Long Hardware Reset)

An asynchronous reset is triggered when $\overline{RSTIN}$ pin is pulled low while V_{PP} pin is at low level. Then the MCU is immediately forced in reset default state. It pulls low $\overline{RSTOUT}$ pin, it cancels pending internal hold states if any, it waits for any internal access cycles to finish, it aborts external bus cycle, it switches buses (data, address and control signals) and I/O pin drivers to high-impedance, it pulls high Port0 pins and the reset sequence starts.

Power-on Reset

The asynchronous reset must be used during the power-on of the MCU. Depending on crystal frequency, the on-chip oscillator needs about 10ms to 50ms to stabilize. The logic of the MCU does not need a stabilized clock signal to detect an asynchronous reset, so it is suitable for power-on conditions. To ensure a proper reset sequence, the $\overline{RSTIN}$ pin and the V_{PP} pin must be held at low level until the MCU clock signal is stabilized and the system configuration value on Port0 is settled.

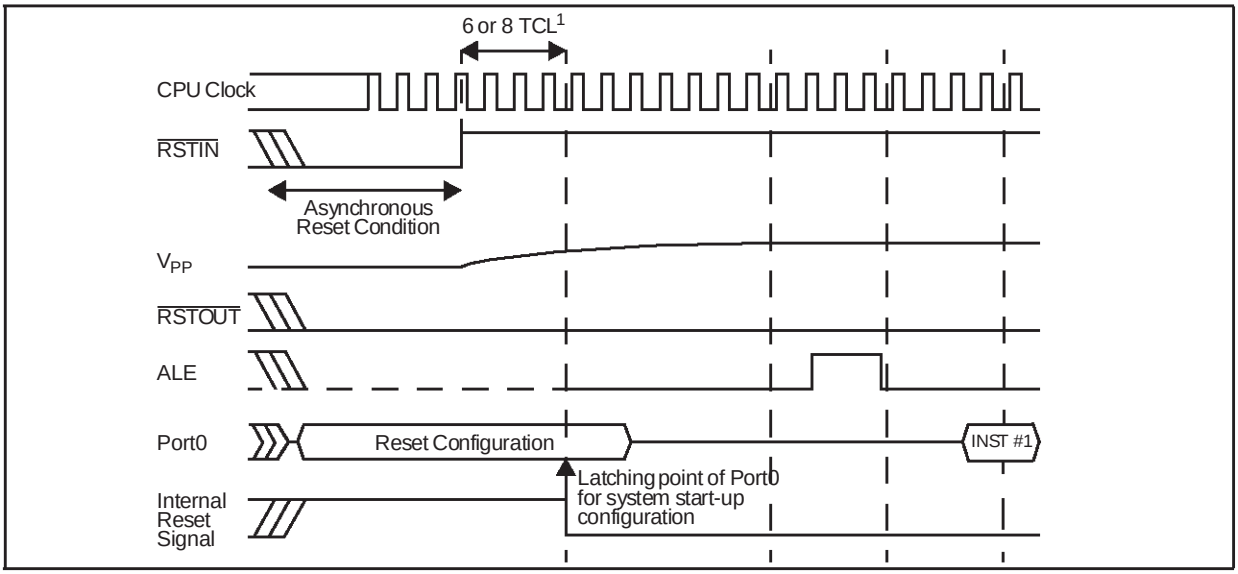
Hardware Reset

The asynchronous reset must be used to recover from catastrophic situations of the application. It may be triggerred by the hardware of the application. Internal hardware logic and application circuitry are described in Reset circuitry chapter and Figures 12, 13 and 14.

Exit of Asynchrounous Reset State

When the $\overline{RSTIN}$ pin is pulled high, the MCU restarts. The system configuration is latched from Port0 and ALE, $\overline{RD}$ and $\overline{R/W}$ pins are driven to their inactive level. The MCU starts program execution from memory location 00'0000h in code segment 0. This starting location will typically point to the general initialization routine. Timing of asynchronous reset sequence are summarized in Figure 9.

Figure 9 : Asynchronous Reset Timing



Note: 1. $\overline{RSTIN}$ rising edge to internal latch of Port0 is 3CPU clock cycles (6 TCL) if the PLL is bypassed and the prescaler is on ($f_{CPU} = f_{XTAL} / 2$), else it is 4 CPU clock cycles (8 TCL).

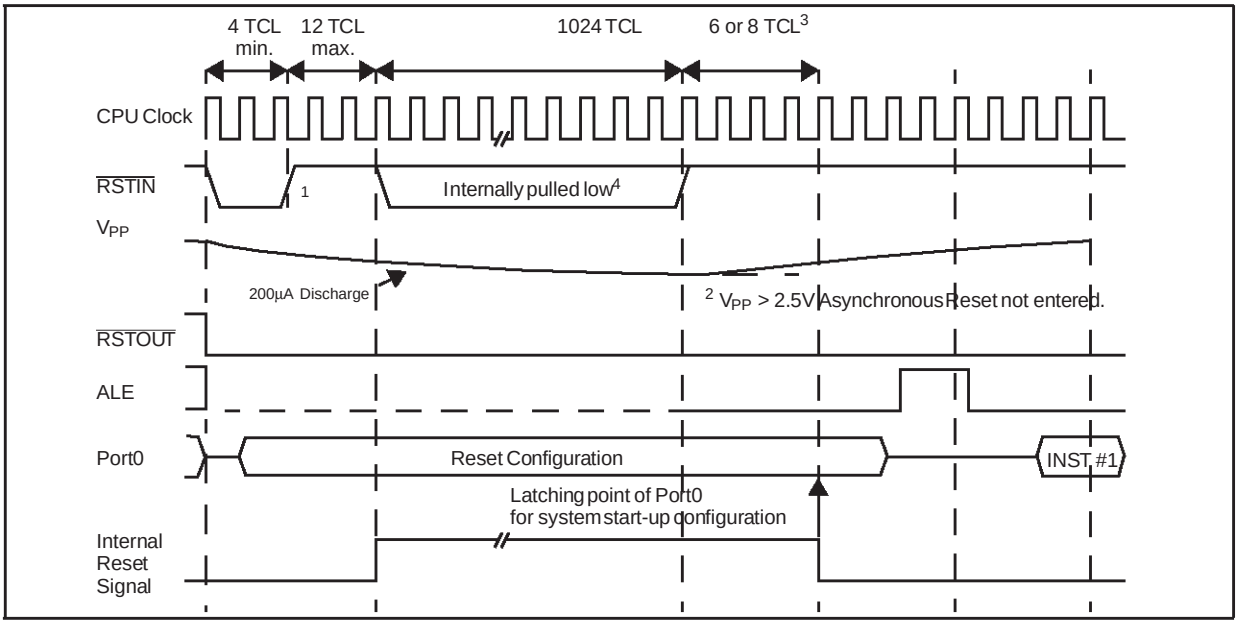
17.2 - Synchronous Reset (Warm Reset)

A synchronous reset is triggered when $\overline{RSTIN}$ pin is pulled low while V_{PP} pin is at high level. In order to properly activate the internal reset logic of the MCU, the $\overline{RSTIN}$ pin must be held low, at least, during 4 TCL (2 periods of CPU clock). The I/O pins are set to high impedance and $\overline{RSTOUT}$ pin is driven low. After $\overline{RSTIN}$ level is detected, a short duration of 12 TCL (approximately 6 periods of CPU clock) elapes, during which pending internal hold states are cancelled and the current internal access cycle if any is completed. External bus cycle is aborted. The internal pulldown of $\overline{RSTIN}$ pin is activated if bit BDRSTEN of SYSCON register was previously set by software. This bit is always cleared on power-on or after a reset sequence.

Exit of Synchrounous Reset State

The internal reset sequence starts for 1024 TCL (512 periods of CPU clock) and $\overline{RSTIN}$ pin level is sampled. The reset sequence is extended until $\overline{RSTIN}$ level becomes high. Then, the MCU restarts. The system configuration is latched from Port0 and ALE, $\overline{RD}$ and $\overline{R/W}$ pins are driven to their inactive level. The MCU starts program execution from memory location 00'0000h in code segment 0. This starting location will typically point to the general initialization routine. Timing of synchronous reset sequence are summarized in Figure 10 and 11.

Figure 10 : Synchronous Warm Reset: Short low pulse on $\overline{RSTIN}$



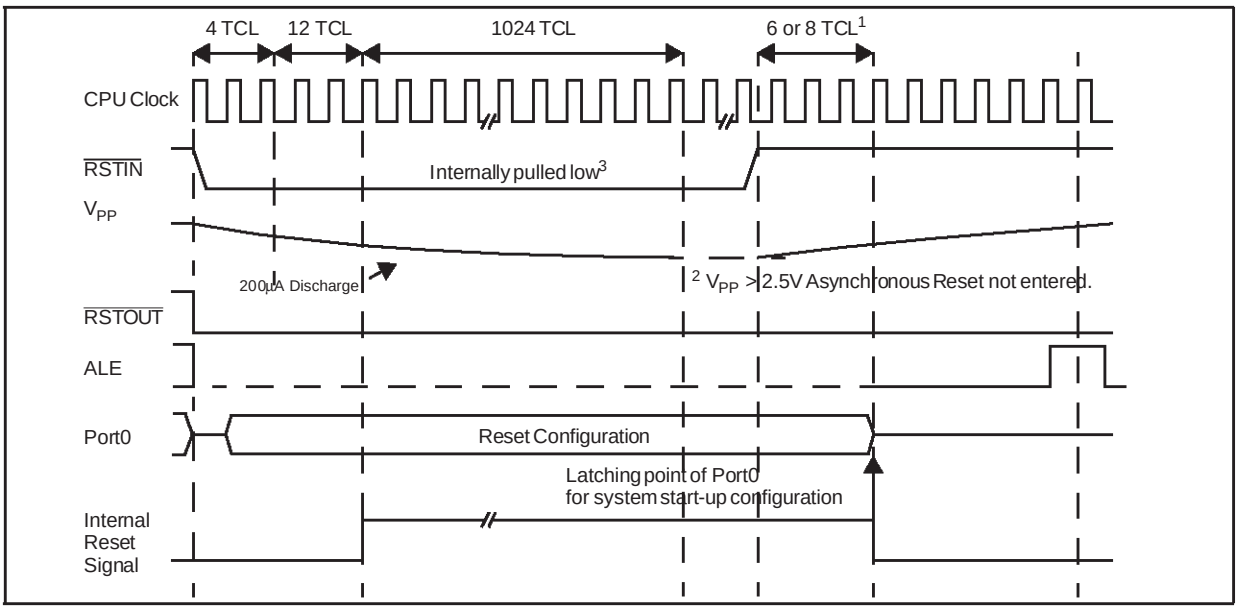
Notes: 1. $\overline{RSTIN}$ assertion can be released there.

2. If during the reset condition ($\overline{RSTIN}$ low), Vpp voltage drops below the threshold voltage (about 2.5V for 5V operation), the asynchronous reset is then immediately entered.

3. $\overline{RSTIN}$ rising edge to internal latch of Port0 is 3CPU clock cycles (6 TCL) if the PLL is bypassed and the prescaler is on ($f_{CPU} = f_{XTAL} / 2$), else it is 4 CPU clock cycles (8 TCL).

4) $\overline{RSTIN}$ pin is pulled low if bit BDRSTEN (bit 5 of SUSCON register) was previously set by software. Bit BDRSTEN is cleared after reset.

Figure 11 : Synchronous Warm Reset: Long low pulse on $\overline{\text{RSTIN}}$



Notes: 1. $\overline{\text{RSTIN}}$ rising edge to internal latch of Port0 is 3CPU clock cycles (6 TCL) if the PLL is bypassed and the prescaler is on ($f_{CPU} = f_{XTAL} / 2$), else it is 4 CPU clock cycles (8 TCL).

2. If during the reset condition ($\overline{\text{RSTIN}}$ low), Vpp voltage drops below the threshold voltage (about 2.5V for 5V operation), the asynchronous reset is then immediately entered.

3. $\overline{\text{RSTIN}}$ pin is pulled low if bit BDRSTEN (bit 5 of SYSCON register) was previously set by soft-ware. Bit BDRSTEN is cleared after reset.

17.3 - Software Reset

A software reset sequence can be triggered at any time by the protected SRST (software reset) instruction. This instruction can be deliberately executed within a program, e.g. to leave bootstrap loader mode, or on a hardware trap that reveals system failure.

On execution of the SRST instruction, the internal reset sequence is started. The microcontroller behaviour is the same as for a synchronous reset, except that only bit P0.12...P0.8 are latched at the end of the reset sequence, while previously latched, bit P0.7...P0.2 are cleared.

17.4 - Watchdog Timer Reset

When the watchdog timer is not disabled during the initialization, or serviced regularly during program execution, it will overflow and trigger the reset sequence.

Unlike hardware and software resets, the watchdog reset completes a running external bus cycle if this bus cycle either does not use $\overline{\text{READY}}$, or if $\overline{\text{READY}}$ is sampled active (low) after the programmed wait states. When $\overline{\text{READY}}$ is sampled inactive (high) after the programmed wait states the running external bus cycle is aborted. Then the internal reset sequence is started.

Bit P0.12...P0.8 are latched at the end of the reset sequence and bit P0.7...P0.2 are cleared.

17.5 - Reset Circuitry

Internal reset circuitry is described in Figure 13. The $\overline{\text{RSTIN}}$ pin provides an internal pullup resistor of 50KΩ to 250KΩ (The minimum reset time must be calculated using the lowest value). It also provides a programmable (BDRSTEN bit of SYSCON register) pulldown to output internal reset state signal (synchronous reset, watchdog timer reset or software reset).

This bidirectional reset function is useful in applications where external devices require a reset signal but cannot be connected to $\overline{\text{RSTOUT}}$ pin.

This is the case of an external memory running codes before EINIT (end of initialization) instruction is executed. $\overline{\text{RSTOUT}}$ pin is pulled high only when EINIT is executed.

The V_{PP} pin provides an internal weak pulldown resistor which discharges external capacitor at a typical rate of 200µA. If bit PWDCFG of SYSCON register is set, an internal pullup resistor is activated at the end of the reset sequence. This pullup will charge any capacitor connected on V_{PP} pin.

The simplest way to reset the ST10F168 is to insert a capacitor C1 between $\overline{RSTIN}$ pin and V_{SS}, and a capacitor between V_{PP} pin and V_{SS} (C0) with a pullup resistor R0 between V_{PP} pin and V_{CC}. The input $\overline{RSTIN}$ provides an internal pullup device equalling a resistor of 50kΩ to 150kΩ (the minimum reset time must be determined by the lowest value). Select C1 that produce a sufficient discharge time to permit the internal or external oscillator and / or internal PLL to stabilize.

To insure correct power-up reset with controlled supply current consumption, specially if clock signal requires a long period of time to stabilized, an asynchronous hardware reset is required during power-up. It is recommended to connect the external R0C0 circuit shown in Figure 12 to the V_{PP} pin. On power-up, the logical low level on V_{PP} pin forces an asynchronous harware reset when $\overline{RSTIN}$ is asserted.

The external pullup R0 will then charge the capacitor C0. Note that an internal pulldown device on V_{PP} pin is turned on when $\overline{RSTIN}$ pin is low, and causes the external capacitor (C0) to begin discharging at a typical rate of 100µA to 200µA. With this mechanism, after power-up reset, short low pulses applied on $\overline{RSTIN}$ produce synchronous hardware reset. If $\overline{RSTIN}$ is asserted longer than the time needed for C0 to be discharged by the internal pulldown device, then the device is forced in an asynchronous reset. This mechanism insures recovery from very catastrophic failure.

Figure 12 : Minimum External Reset Circuitry

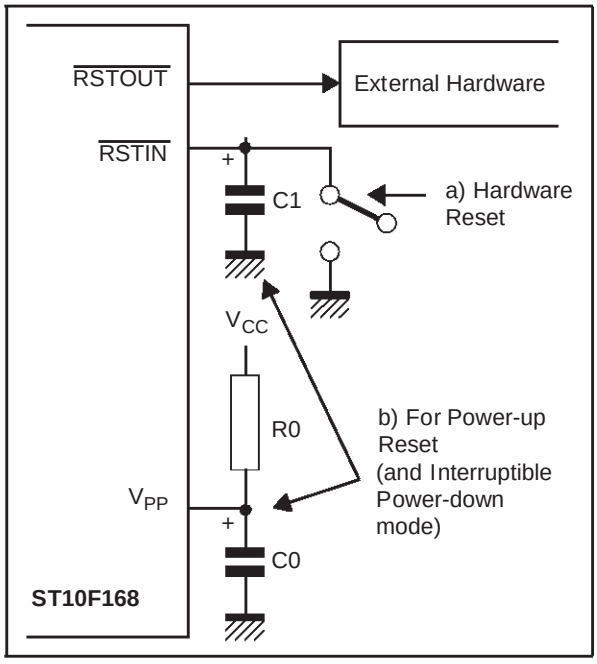
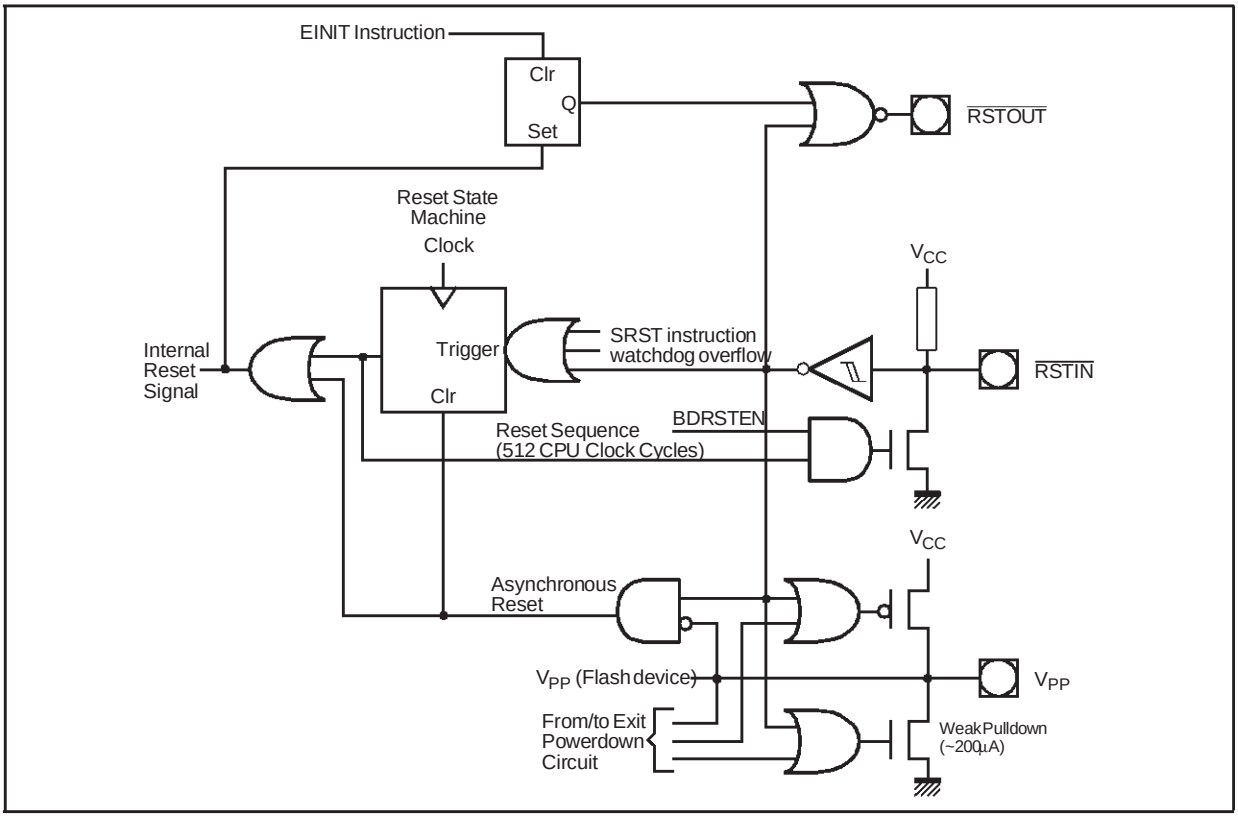


Figure 13 : Internal (simplified) Reset Circuitry

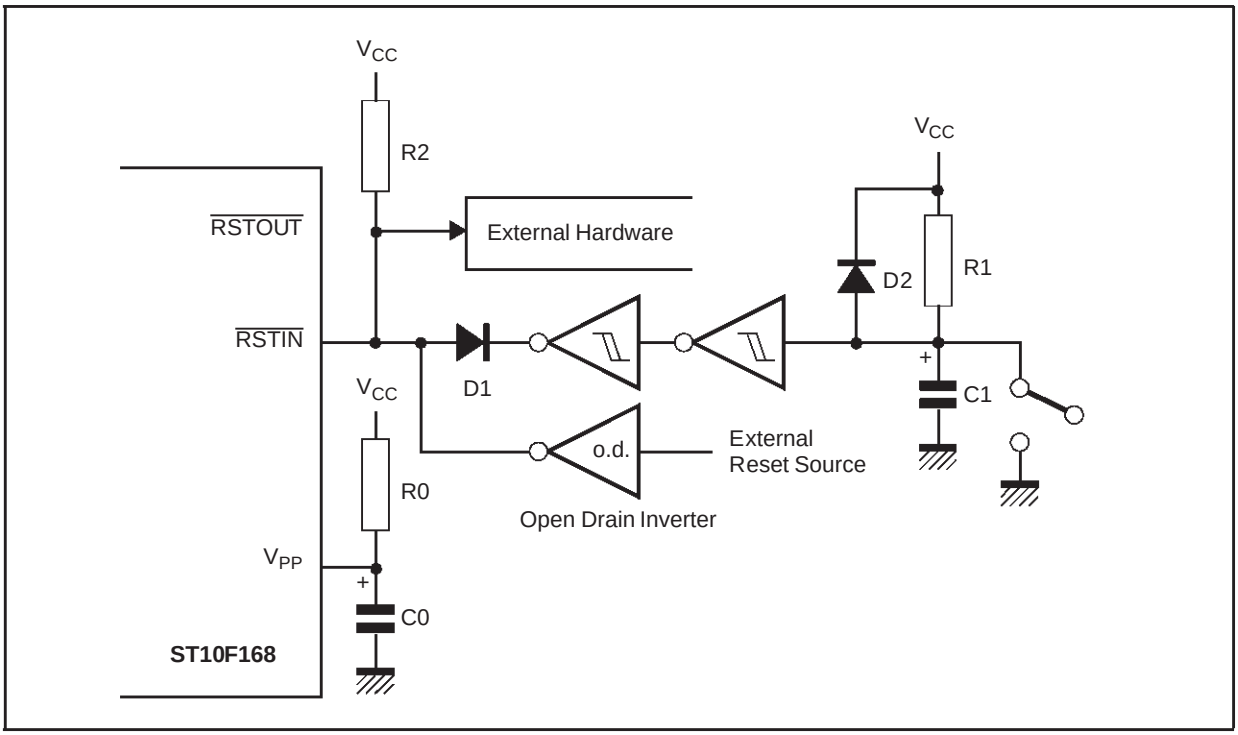


The minimum reset circuit of Figure 14 is not adequate when the $\overline{RSTIN}$ pin is driven from the ST10F168 itself during software or watchdog triggered resets, because of the capacitor C1 that will keep the voltage on $\overline{RSTIN}$ pin above V_{IL} after the end of the internal reset sequence, and thus will triggered an asynchronous reset sequence.

Figure 14 shows an example of a reset circuit. In this example, R1C1 external circuit is only used to generate power-up or manual reset, and R0C0 circuit on V_{PP} is used for power-up reset and to exit from powerdown mode. Diode D1 creates a wired-OR gate connection to the reset pin and may be replaced by open-collector schmitt trigger buffer. Diode D2 provides a faster cycle time for repetitive power-on resets.

R2 is an optional pullup for faster recovery and correct biasing of TTL Open Collector drivers.

Figure 14 : System Reset Circuit



18 - POWER REDUCTION MODES

Two different power reduction modes with different levels of power reduction can be entered under software control.

In **Idle mode** the CPU is stopped, while the peripherals continue their operation. Idle mode can be terminated by any reset or interrupt request.

In **Power Down mode** both the CPU and the peripherals are stopped. Power Down mode can be configured by software in order to be terminated only by a hardware reset or by an external interrupt source on fast external interrupt pins. There are two different operating Power Down modes:

– **Protected power down mode:** selected by setting bit PWDCFG in the SYSCON register to '0'. This mode can be used in conjunction with an external power failure signal which pulls the $\overline{\text{NMI}}$ pin low when a power failure is imminent. The microcontroller enters the $\overline{\text{NMI}}$ trap routine and saves the internal state into RAM. The trap routine then sets a flag or writes a bit pattern into specific RAM locations, and executes the PWRDN instruction. If the $\overline{\text{NMI}}$ pin is still low at this time, Power Down mode will be entered, if not program execution continues. During power down the voltage at the V_{CC} pins can be lowered to 2.5 V and the contents of the internal RAM will still be preserved.

– **Interruptible power down mode:** this mode is selected by setting bit PWDCFG in the SYSCON register. The CPU and peripheral clocks are frozen, and the oscillator and PLL are stopped. To exit power down mode with an external interrupt, an EXxIN (x = 7...0) pin has to be asserted for at least 40ns. This signal enables the internal oscillator and PLL circuitry, and turns on the weak pulldown. If the Interrupt was enabled before entering power down mode, the device executes the interrupt service routine, and then resumes execution after the PWRDN instruction. If the interrupt was disabled, the device executes the instruction following PWRDN instruction, and the Interrupt Request Flag remains set until it is cleared by software.

All external bus actions are completed before Idle or Power Down mode is entered. However, Idle or Power Down mode is **not** entered if READY is enabled, but has not been activated (driven low for negative polarity, or driven high for positive polarity) during the last bus access.

19 - SPECIAL FUNCTION REGISTER OVERVIEW

Table 22 lists all SFRs which are implemented in the ST10F168 in alphabetical order.
Bit-addressable SFRs are marked with the letter “b” in column “Name”. SFRs within the Extended SFR-Space (ESFRs) are marked with the letter “E” in column “Physical Address”.

An SFR can be specified by its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Table 22 : Special Function Registers listed by name

Name	Physical address	8-bit address	Description	Reset value
ADCIC b	FF98h	CCh	A/D Converter End Of Conversion Interrupt Control Register	0000h
ADCON b	FFA0h	D0h	A/D Converter Control Register	0000h
ADDAT	FEA0h	50h	A/D Converter Result Register	0000h
ADDAT2	F0A0h E	50h	A/D Converter 2 Result Register	0000h
ADDRSEL1	FE18h	0Ch	Address Select Register 1	0000h
ADDRSEL2	FE1Ah	0Dh	Address Select Register 2	0000h
ADDRSEL3	FE1Ch	0Eh	Address Select Register 3	0000h
ADDRSEL4	FE1Eh	0Fh	Address Select Register 4	0000h
ADEIC b	FF9Ah	CDh	A/D converter Overrun Error Interrupt Control Register	0000h
BUSCON0 b	FF0Ch	86h	Bus Configuration Register 0	0XX0h
BUSCON1 b	FF14h	8Ah	Bus Configuration Register 1	0000h
BUSCON2 b	FF16h	8Bh	Bus Configuration Register 2	0000h
BUSCON3 b	FF18h	8Ch	Bus Configuration Register 3	0000h
BUSCON4 b	FF1Ah	8Dh	Bus Configuration Register 4	0000h
CAPREL	FE4Ah	25h	GPT2 Capture / Reload Register	0000h
CC0	FE80h	40h	CAPCOM Register 0	0000h
CC0IC b	FF78h	BCh	CAPCOM Register 0 Interrupt Control Register	0000h
CC1	FE82h	41h	CAPCOM Register 1	0000h
CC1IC b	FF7Ah	BDh	CAPCOM Register 1 Interrupt Control Register	0000h
CC2	FE84h	42h	CAPCOM Register 2	0000h
CC2IC b	FF7Ch	BEh	CAPCOM Register 2 Interrupt Control Register	0000h
CC3	FE86h	43h	CAPCOM Register 3	0000h
CC3IC b	FF7Eh	BFh	CAPCOM Register 3 Interrupt Control Register	0000h
CC4	FE88h	44h	CAPCOM Register 4	0000h
CC4IC b	FF80h	C0h	CAPCOM Register 4 Interrupt Control Register	0000h
CC5	FE8Ah	45h	CAPCOM Register 5	0000h
CC5IC b	FF82h	C1h	CAPCOM Register 5 Interrupt Control Register	0000h
CC6	FE8Ch	46h	CAPCOM Register 6	0000h
CC6IC b	FF84h	C2h	CAPCOM Register 6 Interrupt Control Register	0000h
CC7	FE8Eh	47h	CAPCOM Register 7	0000h
CC7IC b	FF86h	C3h	CAPCOM Register 7 Interrupt Control Register	0000h
CC8	FE90h	48h	CAPCOM Register 8	0000h
CC8IC b	FF88h	C4h	CAPCOM Register 8 Interrupt Control Register	0000h
CC9	FE92h	49h	CAPCOM Register 9	0000h

Table 22 : Special Function Registers listed by name

Name	Physical address	8-bit address	Description	Reset value
CC9IC b	FF8Ah	C5h	CAPCOM Register 9 Interrupt Control Register	0000h
CC10	FE94h	4Ah	CAPCOM Register 10	0000h
CC10IC b	FF8Ch	C6h	CAPCOM Register 10 Interrupt Control Register	0000h
CC11	FE96h	4Bh	CAPCOM Register 11	0000h
CC11IC b	FF8Eh	C7h	CAPCOM Register 11 Interrupt Control Register	0000h
CC12	FE98h	4Ch	CAPCOM Register 12	0000h
CC12IC b	FF90h	C8h	CAPCOM Register 12 Interrupt Control Register	0000h
CC13	FE9Ah	4Dh	CAPCOM Register 13	0000h
CC13IC b	FF92h	C9h	CAPCOM Register 13 Interrupt Control Register	0000h
CC14	FE9Ch	4Eh	CAPCOM Register 14	0000h
CC14IC b	FF94h	CAh	CAPCOM Register 14 Interrupt Control Register	0000h
CC15	FE9Eh	4Fh	CAPCOM Register 15	0000h
CC15IC b	FF96h	CBh	CAPCOM Register 15 Interrupt Control Register	0000h
CC16	FE60h	30h	CAPCOM Register 16	0000h
CC16IC b	F160h E	B0h	CAPCOM Register 16 Interrupt Control Register	0000h
CC17	FE62h	31h	CAPCOM Register 17	0000h
CC17IC b	F162h E	B1h	CAPCOM Register 17 Interrupt Control Register	0000h
CC18	FE64h	32h	CAPCOM Register 18	0000h
CC18IC b	F164h E	B2h	CAPCOM Register 18 Interrupt Control Register	0000h
CC19	FE66h	33h	CAPCOM Register 19	0000h
CC19IC b	F166h E	B3h	CAPCOM Register 19 Interrupt Control Register	0000h
CC20	FE68h	34h	CAPCOM Register 20	0000h
CC20IC b	F168h E	B4h	CAPCOM Register 20 Interrupt Control Register	0000h
CC21	FE6Ah	35h	CAPCOM Register 21	0000h
CC21IC b	F16Ah E	B5h	CAPCOM Register 21 Interrupt Control Register	0000h
CC22	FE6Ch	36h	CAPCOM Register 22	0000h
CC22IC b	F16Ch E	B6h	CAPCOM Register 22 Interrupt Control Register	0000h
CC23	FE6Eh	37h	CAPCOM Register 23	0000h
CC23IC b	F16Eh E	B7h	CAPCOM Register 23 Interrupt Control Register	0000h
CC24	FE70h	38h	CAPCOM Register 24	0000h
CC24IC b	F170h E	B8h	CAPCOM Register 24 Interrupt Control Register	0000h
CC25	FE72h	39h	CAPCOM Register 25	0000h
CC25IC b	F172h E	B9h	CAPCOM Register 25 Interrupt Control Register	0000h
CC26	FE74h	3Ah	CAPCOM Register 26	0000h
CC26IC b	F174h E	BAh	CAPCOM Register 26 Interrupt Control Register	0000h
CC27	FE76h	3Bh	CAPCOM Register 27	0000h
CC27IC b	F176h E	BBh	CAPCOM Register 27 Interrupt Control Register	0000h
CC28	FE78h	3Ch	CAPCOM Register 28	0000h
CC28IC b	F178h E	BCh	CAPCOM Register 28 Interrupt Control Register	0000h
CC29	FE7Ah	3Dh	CAPCOM Register 29	0000h

Table 22 : Special Function Registers listed by name

Name	Physical address	8-bit address	Description	Reset value
CC29IC b	F184h E	C2h	CAPCOM Register 29 Interrupt Control Register	0000h
CC30	FE7Ch	3Eh	CAPCOM Register 30	0000h
CC30IC b	F18Ch E	C6h	CAPCOM Register 30 Interrupt Control Register	0000h
CC31	FE7Eh	3Fh	CAPCOM Register 31	0000h
CC31IC b	F194h E	CAh	CAPCOM Register 31 Interrupt Control Register	0000h
CCM0 b	FF52h	A9h	CAPCOM Mode Control Register 0	0000h
CCM1 b	FF54h	AAh	CAPCOM Mode Control Register 1	0000h
CCM2 b	FF56h	ABh	CAPCOM Mode Control Register 2	0000h
CCM3 b	FF58h	ACh	CAPCOM Mode Control Register 3	0000h
CCM4 b	FF22h	91h	CAPCOM Mode Control Register 4	0000h
CCM5 b	FF24h	92h	CAPCOM Mode Control Register 5	0000h
CCM6 b	FF26h	93h	CAPCOM Mode Control Register 6	0000h
CCM7 b	FF28h	94h	CAPCOM Mode Control Register 7	0000h
CP	FE10h	08h	CPU Context Pointer Register	FC00h
CRIC b	FF6Ah	B5h	GPT2 CAPREL Interrupt Control Register	0000h
CSP	FE08h	04h	CPU Code Segment Pointer Register (read only)	0000h
DP0L b	F100h E	80h	P0L Direction Control Register	00h
DP0H b	F102h E	81h	P0h Direction Control Register	00h
DP1L b	F104h E	82h	P1L Direction Control Register	00h
DP1H b	F106h E	83h	P1h Direction Control Register	00h
DP2 b	FFC2h	E1h	Port 2 Direction Control Register	0000h
DP3 b	FFC6h	E3h	Port 3 Direction Control Register	0000h
DP4 b	FFCAh	E5h	Port 4 Direction Control Register	00h
DP6 b	FFCEh	E7h	Port 6 Direction Control Register	00h
DP7 b	FFD2h	E9h	Port 7 Direction Control Register	00h
DP8 b	FFD6h	EBh	Port 8 Direction Control Register	00h
DPP0	FE00h	00h	CPU Data Page Pointer 0 Register (10-bit)	0000h
DPP1	FE02h	01h	CPU Data Page Pointer 1 Register (10-bit)	0001h
DPP2	FE04h	02h	CPU Data Page Pointer 2 Register (10-bit)	0002h
DPP3	FE06h	03h	CPU Data Page Pointer 3 Register (10-bit)	0003h
EXICON b	F1C0h E	E0h	External Interrupt Control Register	0000h
IDCHIP	F07Ch E	3Eh	Device Identifier Register	0A8Xh[1]
IDMANUF	F07Eh E	3Fh	Manufacturer Identifier Register	0400h
IDMEM	F07Ah E	3Dh	On-chip Memory Identifier Register	3040h
IDPROG	F078h E	3Ch	Programming Voltage Identifier Register	9A40h
MDC b	FF0Eh	87h	CPU Multiply Divide Control Register	0000h
MDH	FE0Ch	06h	CPU Multiply Divide Register – High Word	0000h
MDL	FE0Eh	07h	CPU Multiply Divide Register – Low Word	0000h
ODP2 b	F1C2h E	E1h	Port 2 Open Drain Control Register	0000h
ODP3 b	F1C6h E	E3h	Port 3 Open Drain Control Register	0000h

Table 22 : Special Function Registers listed by name

Name	Physical address	8-bit address	Description	Reset value
ODP6 b	F1CEh E	E7h	Port 6 Open Drain Control Register	00h
ODP7 b	F1D2h E	E9h	Port 7 Open Drain Control Register	00h
ODP8 b	F1D6h E	EBh	Port 8 Open Drain Control Register	00h
ONES b	FF1Eh	8Fh	Constant Value 1's Register (read only)	FFFFh
P0L b	FF00h	80h	Port 0 Low Register (Lower half of Port0)	00h
P0H b	FF02h	81h	Port 0 High Register (Upper half of Port0)	00h
P1L b	FF04h	82h	Port 1 Low Register (Lower half of Port1)	00h
P1H b	FF06h	83h	Port 1 High Register (Upper half of Port1)	00h
P2 b	FFC0h	E0h	Port 2 Register	0000h
P3 b	FFC4h	E2h	Port 3 Register	0000h
P4 b	FFC8h	E4h	Port 4 Register (8-bit)	00h
P5 b	FFA2h	D1h	Port 5 Register (read only)	XXXXh
P6 b	FFCCh	E6h	Port 6 Register (8-bit)	00h
P7 b	FFD0h	E8h	Port 7 Register (8-bit)	00h
P8 b	FFD4h	EAh	Port 8 Register (8-bit)	00h
PECC0	FEC0h	60h	PEC Channel 0 Control Register	0000h
PECC1	FEC2h	61h	PEC Channel 1 Control Register	0000h
PECC2	FEC4h	62h	PEC Channel 2 Control Register	0000h
PECC3	FEC6h	63h	PEC Channel 3 Control Register	0000h
PECC4	FEC8h	64h	PEC Channel 4 Control Register	0000h
PECC5	FECAh	65h	PEC Channel 5 Control Register	0000h
PECC6	FECCh	66h	PEC Channel 6 Control Register	0000h
PECC7	FECEh	67h	PEC Channel 7 Control Register	0000h
PICON	F1C4h E	E2h	Port Input Threshold Control Register	0000h
PP0	F038h E	1Ch	PWM Module Period Register 0	0000h
PP1	F03Ah E	1Dh	PWM Module Period Register 1	0000h
PP2	F03Ch E	1Eh	PWM Module Period Register 2	0000h
PP3	F03Eh E	1Fh	PWM Module Period Register 3	0000h
PSW b	FF10h	88h	CPU Program Status Word	0000h
PT0	F030h E	18h	PWM Module Up / Down Counter 0	0000h
PT1	F032h E	19h	PWM Module Up / Down Counter 1	0000h
PT2	F034h E	1Ah	PWM Module Up / Down Counter 2	0000h
PT3	F036h E	1Bh	PWM Module Up / Down Counter 3	0000h
PW0	FE30h	18h	PWM Module Pulse Width Register 0	0000h
PW1	FE32h	19h	PWM Module Pulse Width Register 1	0000h
PW2	FE34h	1Ah	PWM Module Pulse Width Register 2	0000h
PW3	FE36h	1Bh	PWM Module Pulse Width Register 3	0000h
PWMCON0 b	FF30h	98h	PWM Module Control Register 0	0000h
PWMCON1 b	FF32h	99h	PWM Module Control Register 1	0000h

Table 22 : Special Function Registers listed by name

Name	Physical address	8-bit address	Description	Reset value
PWMIC b	F17Eh E	BFh	PWM Module Interrupt Control Register	0000h
RP0H b	F108h E	84h	System Start-up Configuration Register (read only)	XXh
S0BG	FEB4h	5Ah	Serial Channel 0 Baud Rate Generator Reload Register	0000h
S0CON b	FFB0h	D8h	Serial Channel 0 Control Register	0000h
S0EIC b	FF70h	B8h	Serial Channel 0 Error Interrupt Control Register	0000h
S0RBUF	FEB2h	59h	Serial Channel 0 Receive Buffer Register (read only)	XXh
S0RIC b	FF6Eh	B7h	Serial Channel 0 Receive Interrupt Control Register	0000h
S0TBIC b	F19Ch E	CEh	Serial Channel 0 Transmit Buffer Interrupt Control Register	0000h
S0TBUF	FEB0h	58h	Serial Channel 0 Transmit Buffer Register (write only)	00h
S0TIC b	FF6Ch	B6h	Serial Channel 0 Transmit Interrupt Control Register	0000h
SP	FE12h	09h	CPU System Stack Pointer Register	FC00h
SSCBR	F0B4h E	5Ah	SSC Baud Rate Register	0000h
SSCCON b	FFB2h	D9h	SSC Control Register	0000h
SSCEIC b	FF76h	BBh	SSC Error Interrupt Control Register	0000h
SSCRB	F0B2h E	59h	SSC Receive Buffer (read only)	XXXXh
SSCRIC b	FF74h	BAh	SSC Receive Interrupt Control Register	0000h
SSCTB	F0B0h E	58h	SSC Transmit Buffer (write only)	0000h
SSCTIC b	FF72h	B9h	SSC Transmit Interrupt Control Register	0000h
STKOV	FE14h	0Ah	CPU Stack Overflow Pointer Register	FA00h
STKUN	FE16h	0Bh	CPU Stack Underflow Pointer Register	FC00h
SYSCON b	FF12h	89h	CPU System Configuration Register	0xx0h[2]
T0	FE50h	28h	CAPCOM Timer 0 Register	0000h
T01CON b	FF50h	A8h	CAPCOM Timer 0 and Timer 1 Control Register	0000h
T0IC b	FF9Ch	CEh	CAPCOM Timer 0 Interrupt Control Register	0000h
T0REL	FE54h	2Ah	CAPCOM Timer 0 Reload Register	0000h
T1	FE52h	29h	CAPCOM Timer 1 Register	0000h
T1IC b	FF9Eh	CFh	CAPCOM Timer 1 Interrupt Control Register	0000h
T1REL	FE56h	2Bh	CAPCOM Timer 1 Reload Register	0000h
T2	FE40h	20h	GPT1 Timer 2 Register	0000h
T2CON b	FF40h	A0h	GPT1 Timer 2 Control Register	0000h
T2IC b	FF60h	B0h	GPT1 Timer 2 Interrupt Control Register	0000h
T3	FE42h	21h	GPT1 Timer 3 Register	0000h
T3CON b	FF42h	A1h	GPT1 Timer 3 Control Register	0000h
T3IC b	FF62h	B1h	GPT1 Timer 3 Interrupt Control Register	0000h
T4	FE44h	22h	GPT1 Timer 4 Register	0000h
T4CON b	FF44h	A2h	GPT1 Timer 4 Control Register	0000h
T4IC b	FF64h	B2h	GPT1 Timer 4 Interrupt Control Register	0000h
T5	FE46h	23h	GPT2 Timer 5 Register	0000h
T5CON b	FF46h	A3h	GPT2 Timer 5 Control Register	0000h
T5IC b	FF66h	B3h	GPT2 Timer 5 Interrupt Control Register	0000h

Table 22 : Special Function Registers listed by name

Name		Physical address		8-bit address	Description	Reset value
T6		FE48h		24h	GPT2 Timer 6 Register	0000h
T6CON	b	FF48h		A4h	GPT2 Timer 6 Control Register	0000h
T6IC	b	FF68h		B4h	GPT2 Timer 6 Interrupt Control Register	0000h
T7		F050h	E	28h	CAPCOM Timer 7 Register	0000h
T78CON	b	FF20h		90h	CAPCOM Timer 7 and 8 Control Register	0000h
T7IC	b	F17Ah	E	BEh	CAPCOM Timer 7 Interrupt Control Register	0000h
T7REL		F054h	E	2Ah	CAPCOM Timer 7 Reload Register	0000h
T8		F052h	E	29h	CAPCOM Timer 8 Register	0000h
T8IC	b	F17Ch	E	BFh	CAPCOM Timer 8 Interrupt Control Register	0000h
T8REL		F056h	E	2Bh	CAPCOM Timer 8 Reload Register	0000h
TFR	b	FFACh		D6h	Trap Flag Register	0000h
WDT		FEAEh		57h	Watchdog Timer Register (read only)	0000h
WDTCON	b	FFAEh		D7h	Watchdog Timer Control Register	000xh[3]
XP0IC	b	F186h	E	C3h	CAN Module Interrupt Control Register	0000h[4]
XP1IC	b	F18Eh	E	C7h	X-Peripheral 1 Interrupt Control Register	0000h[4]
XP2IC	b	F196h	E	CBh	X-Peripheral 2 Interrupt Control Register	0000h[4]
XP3IC	b	F19Eh	E	CFh	PLL unlock Interrupt Control Register	0000h[4]
ZEROS	b	FF1Ch		8Eh	Constant Value 0's Register (read only)	0000h

Notes: 1. The value depends on the silicon revision and is described in the chapter 19.1.

2. The system configuration is selected during reset.

3. Bit WDTR indicates a watchdog timer triggered reset.

4. The XPnIC Interrupt Control Registers control the interrupt requests from integrated X-Bus peripherals. Nodes where no X-Peripherals are connected may be used to generate software controlled interrupt requests by setting the respective XPnIR bit.

19.1 - Identification Registers

The ST10F168 has four Identification registers, mapped in ESFR space. These register contain:

– A manufacturer identifier,
– A chip identifier, with its revision,
– A internal memory and size identifier,
– Programming voltage description.

IDMANUF (F07Eh / 3Fh) ESFR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MANUF											-	-	-	-	-
R															

Description

MANUF : Manufacturer Identifier - 020h: STmicroelectronics Manufacturer (JTAG worldwide normalisation).

IDCHIP (F07Ch / 3Eh) ESFR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHIPID												REVID			
R												R			

Description

REVID : Device Revision Identifier - 1h for the first step, 2h for the second step,...

CHIPID: Device Identifier - 0A8h is the identifier of ST10F168.

IDMEM (F07Ah / 3Dh) ESFR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEMTYP				MEMSIZE											
R				R											

Description

MEMSIZE : Internal Memory Size - 040h for ST10F168 (256K Bytes).
Internal Memory size is 4 * <MEMSIZE> (in K Byte).

MEMTYP : Internal Memory Type - 3h for ST10F168 (Flash memory).

IDPROG (F078h / 3Ch) ESFR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROGVPP								PROGVDD							
R								R							

Description

PROGVDD : Programming V_{DD} Voltage
V_{DD} voltage when programming EPROM or Flash devices is calculated using the following formula: V_{DD} = 20 * <PROGVDD> / 256 [V] - 40h for ST10F168 (5V).

PROGVPP : Programming V_{PP} Voltage
V_{PP} voltage when programming EPROM or Flash devices is calculated using the following formula: V_{PP} = 20 * <PROGVDD> / 256 [V] - 9Ah for ST10F168 (12V).

20 - ELECTRICAL CHARACTERISTICS

20.1 - Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	Voltage on V_{DD} pins with respect to ground[1]	-0.5, +6.5	V
V_{IO}	Voltage on any pin with respect to ground[1]	-0.5, (V_{DD} +0.5)	V
I_{OV}	Input Current on any pin during overload condition[1]	-10, +10	mA
I_{TOV}	Absolute Sum of all input currents during overload condition[1]	|100 mA|	mA
P_{tot}	Power Dissipation[1]	1.5	W
T_A	Ambient Temperature under bias for - Q6[1] Ambient Temperature under bias for - Q3[1]	-40, +85 -40, +125	°C °C
T_{stg}	Storage Temperature[1]	-65, +150	°C

Note: 1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions (V_{IN}>V_{DD} or V_{IN}<V_{SS}) the voltage on pins with respect to ground (V_{SS}) must not exceed the values defined by the Absolute Maximum Ratings.

20.2 - Parameter Interpretation

The parameters listed in the following tables represent the characteristics of the ST10F168 and its demands on the system.

Where the ST10F168 logic provides signals with their respective timing characteristics, the symbol "**CC**" for Controller Characteristics is included in the "Symbol" column.

Where the external system must provide signals with their respective timing characteristics to the ST10F168, the symbol "**SR**" for System Requirement is included in the "Symbol" column.

20.3 - DC Characteristics

V_{DD} = 5V ± 10%, V_{SS} = 0V, Reset active, for Q6 version : T_A = -40, +85°C and for Q3 version T_A = -40, +125°C, unless otherwise specified.

Symbol		Parameter	Test Conditions	Min.	Max.	Unit
V_{IL}	SR	Input low voltage	–	– 0.5	0.2 V_{DD} – 0.1	V
V_{ILS}	SR	Input low voltage (special threshold)	–	– 0.5	2.0	V
V_{IH}	SR	Input high voltage (all except $\overline{RSTIN}$ and XTAL1)	–	0.2 V_{DD} + 0.9	V_{DD} + 0.5	V
V_{IH1}	SR	Input high voltage $\overline{RSTIN}$	–	0.6 V_{DD}	V_{DD} + 0.5	V
V_{IH2}	SR	Input high voltage XTAL1	–	0.7 V_{DD}	V_{DD} + 0.5	V
V_{IHS}	SR	Input high voltage (special threshold)	–	0.8 V_{DD} - 0.2	V_{DD} + 0.5	V
HYS		Input Hysteresis (special threshold)	–	300	-	mV
V_{OL}	CC	Output low voltage [1] (Port0, Port1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	I_{OL} = 2.4mA	–	0.45	V
V_{OL1}	CC	Output low voltage[1] (all other outputs)	I_{OL1} = 1.6mA	–	0.45	V
V_{OH}	CC	Output high voltage[1] (Port0, Port1, Port4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	I_{OH} = – 500µA I_{OH} = –2.4mA	0.9 V_{DD} 2.4	– –	V
V_{OH1}	CC	Output high voltage [1 2] (all other outputs)	I_{OH} = – 250µA I_{OH} = – 1.6mA	0.9 V_{DD} 2.4	– –	V V
I_{OZ1}	CC	Input leakage current (Port 5)	0V < V_{IN} < V_{DD}	–	±0.5	µA

Symbol		Parameter	Test Conditions	Min.	Max.	Unit
I_{OZ2}	CC	Input leakage current (all other)	$0V < V_{IN} < V_{DD}$	–	±1	µA
I_{OV}	SR	Overload current	[3] [4]	–	±5	mA
R_{RST}	CC	$\overline{RSTIN}$ pull-up resistor [3]	$0V < V_{IN} < V_{ILmax}$	50	250	kΩ
I_{RWH} [5]		Read / Write inactive current [6]	$V_{OUT} = 2.4V$	–	-40	µA
I_{RWL} [7]		Read / Write active current [6]	$V_{OUT} = V_{OLmax}$	-500	–	µA
I_{ALEL} [6]		ALE inactive current [6]	$V_{OUT} = V_{OLmax}$	40	–	µA
I_{ALEH} [6]		ALE active current [6]	$V_{OUT} = 2.4V$	–	600	µA
I_{P6H} [6]		Port 6 inactive current [6]	$V_{OUT} = 2.4V$	–	-40	µA
I_{P6L} [7]		Port 6 active current [6]	$V_{OUT} = V_{OL1max}$	-500	–	µA
I_{P0H} [6]		Port 0 configuration current [6]	$V_{IN} = V_{IHmin}$	–	-10	µA
I_{P0L} [7]			$V_{IN} = V_{ILmax}$	-100	–	µA
I_{IL}	CC	XTAL1 input current	$0V < V_{IN} < V_{DD}$	–	±20	µA
C_{IO}	CC	Pin capacitance [6] (digital inputs / outputs)	f = 1MHz, $T_A = 25°C$	–	10	pF
I_{CC}		Power supply current	RSTIN = V_{IH1} [8] f_{CPU} in [MHz]	–	20 + 6 x f_{CPU}	mA
I_{ID}		Idle mode supply current	RSTIN = V_{IH1} [9] f_{CPU} in [MHz]	–	20 + 3 x f_{CPU}	mA
I_{PD}		Power-down mode supply current	$V_{DD} = 5.5V$ [10]	–	100	µA
I_{PPR}		V_{PP} Read Current	$V_{PP} < V_{DD}$	–	200	µA
I_{PPW}		V_{PP} Programming / Erasing Current [3]	$V_{PP} = 12V$, $f_{CPU} = 25MHz$	–	20	mA
V_{PP} [11]		V_{PP} during Programming / Erasing Operations		11,4	12,6	V

Notes: 1. ST10F168 pins are equipped with low-noise output drivers which significantly improve the device's EMI performance. These low-noise drivers deliver their maximum current only until the respective target output level is reached. After this, the output current is reduced. This results in increased impedance of the driver, which attenuates electrical noise from the connected PCB tracks. The current specified in column "Test Conditions" is delivered in all cases.

2. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

3. Partially tested, guaranteed by design characterization.

4. Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD}$+0.5V or $V_{OV} < -0.5V$). The absolute sum of input overload currents on all port pins may not exceed 50mA. The supply voltage must remain within the specified limits.

5. The maximum current may be drawn while the respective signal line remains inactive.

6. This specification is only valid during Reset, or during Hold-mode or Adapt-mode. Port 6 pins are only affected if they are used for $\overline{CS}$ output and the open drain function is not enabled.

7. The minimum current must be drawn in order to drive the respective signal line active.

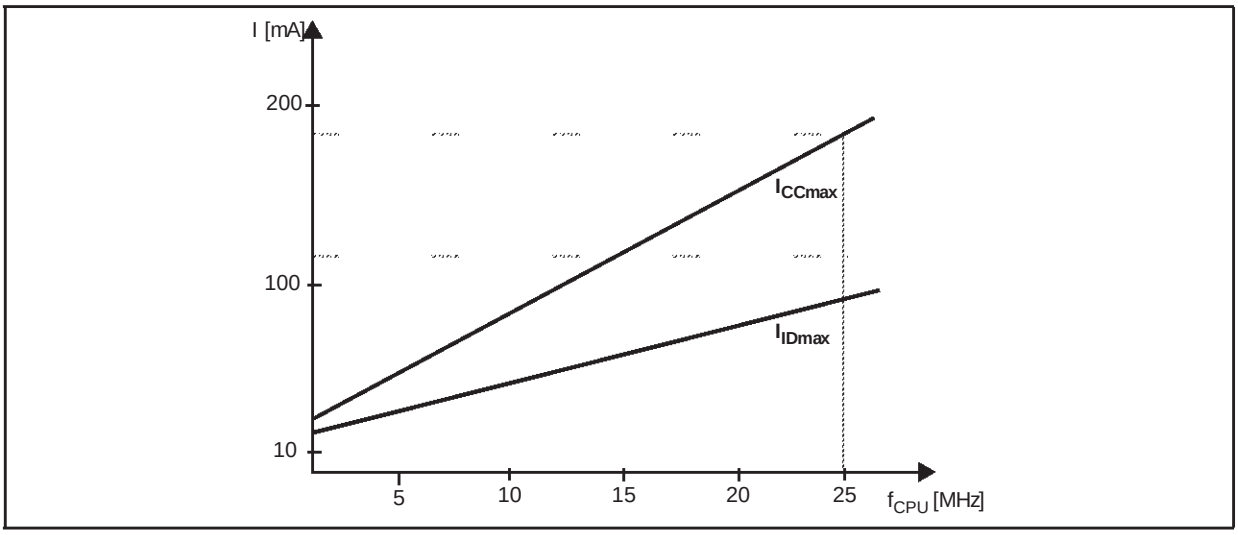
8. The power supply current is a function of the operating frequency. This dependency is illustrated in the Figure 15. These parameters are tested at V_{DD}max and 25MHz CPU clock with all outputs disconnected and all inputs at VIL or VIH. The chip is configured with a demultiplexed 16-bit bus, direct clock drive, 5 chip select lines and 2 segment address lines, EA pin is low during reset. After reset, Port 0 is driven with the value '00CCh' that produces infinite execution of NOP instruction with 15 wait-state, R/W delay, memory tristate wait state, normal ALE. Peripherals are not activated.

9. Idle mode supply current is a function of the operating frequency. This dependency is illustrated in the Figure 15. These parameters are tested at V_{DD}max and 25MHz CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

10. This parameter value includes leakage currents. With all inputs (including pins configured as inputs) at 0 V to 0.1V or at V_{DD} – 0.1V to V_{DD}, V_{REF} = 0V, all outputs (including pins configured as outputs) disconnected.

11. Apply 12V on V_{PP} 10ms after V_{DD} is stable at power up. V_{PP} pin must be switched to 0V before to switch off V_{DD} (5V).

Figure 15 : Supply / idle current as a function of operation frequency



20.4 - A/D Converter Characteristics

V_{DD} = 5V ±10%, V_{SS} = 0V, 4.0V ≤ V_{AREF} ≤ V_{DD} + 0.1V, V_{SS} - 0.1V ≤ V_{AGND} ≤ V_{SS} + 0.2V, Q6 version : T_A = -40, +85°C and for Q3 version T_A = -40°C, +125°C, unless otherwise specified

Symbol		Parameter	Test Conditions	Min.	Max.	Unit
V_{AIN}	SR	Analog input voltage range	1 - 8	V_{AGND}	V_{AREF}	V
t_S	CC	Sample time	2 - 4	48 TCL	1 536 TCL	
t_C	CC	Conversion time	3 - 4	388 TCL	2 884 TCL	
TUE	CC	Total unadjusted error	5	–	± 2	LSB
R_{AREF}	SR	Internal resistance of reference voltage source	t_{CC} in [ns] 6 - 7	–	(t_{CC} / 165) - 0.25	kΩ
R_{ASRC}	SR	Internal resistance of analog source	t_S in [ns] 2 - 7	–	(t_S / 330) - 0.25	kΩ
C_{AIN}	CC	ADC input capacitance	7	–	33	pF

Notes: 1. V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be X000h or X3FFh, respectively.

2. During the t_S sample time the input capacitance C_{ain} can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within the t_S sample time. After the end of the t_S sample time, changes of the analog input voltage have no effect on the conversion result. Values for the t_{SC} sample clock depend on the programming. Referring to the t_C conversion time formula of chapter 13, to the table 17 of page 33 and to the table below:

t_S min = 2 t_{SC} min = 2 t_{CC} min = 2 x 24 x TCL = 48 TCL

t_S max = 2 t_{SC} max = 2 x 8 t_{CC} max = 2 x 8 x 96 TCL = 1536 TCL

TCL is defined in section 20.5.5 at page 55.

3. The conversion time formula is:

t_C = 14 t_{CC} + t_S + 4 TCL (= 14 t_{CC} + 2 t_{SC} + 4 TCL)

The t_C parameter includes the t_S sample time, the time for determining the digital result and the time to load the result register with the result of the conversion. Values for the t_{CC} conversion clock depend on the programming. Referring to the table 17 of page 33 and to the table below:

t_C min = 14 t_{CC} min + t_S min + 4 TCL = 14 x 24 x TCL + 48 TCL + 4 TCL = 388 TCL

t_C max = 14 t_{CC} max + t_S max + 4 TCL = 14 x 96 TCL + 1536 TCL + 4 TCL = 2884 TCL

4. This parameter is fixed by ADC control logic.

5. TUE is tested at V_{AREF} = 5.0V, V_{AGND} = 0V, V_{CC} = 4.9V. It is guaranteed by design characterization for all other voltages within the defined voltage range. The specified TUE is guaranteed only if an overload condition (see Iov specification) occurs on maximum of 2 not selected analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10mA. During the reset calibration sequence the maximum TUE may be ±4 LSB.

6. During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference voltage source must allow the capacitance to reach its respective voltage level within t_{CC}. The maximum internal resistance results from the programmed conversion timing.

7. Partially tested, guaranteed by design characterization.

8. To remove noise and undesirable high frequency components from the analog input signal, a low-pass filter must be connected at the ADC input. The cut-off frequency of this filter must be twice the highest conversion frequency used in the application as described in the formula:
$f_{cut\text{-}off} = 2 / t_{c\ app}$
where $t_{c\ app}$ is the shorter conversion time used in the application, calculated with the following formula:
$t_{c\ app} = 14\ t_{CC} + t_S + 4$ TCL (= 14 t_{CC} + 2 t_{SC} + 4 TCL).

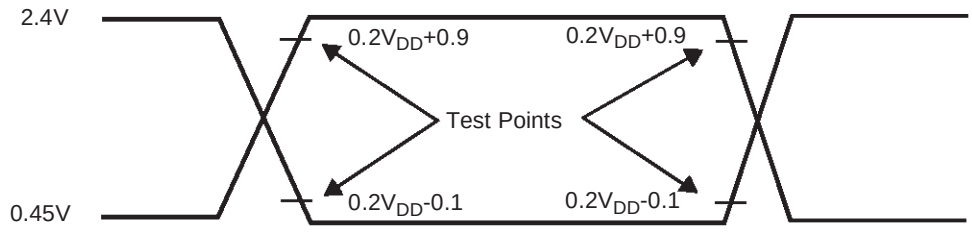
ADC Sample time and conversion time are programmable. The table below should be used to calculate the above timings.

Conversion Time		Sample Time	
ADCON.15|14 (ADCTC)	**Conversion clock t_{CC}**	**ADCON.13|12 (ADSTC)**	**Sample clock t_{SC}**
00	TCL x 24	00	t_{CC}
01	Reserved, do not use	01	t_{CC} x 2
10	TCL x 96	10	t_{CC} x 4
11	TCL x 48	11	t_{CC} x 8

20.5 - AC Characteristics

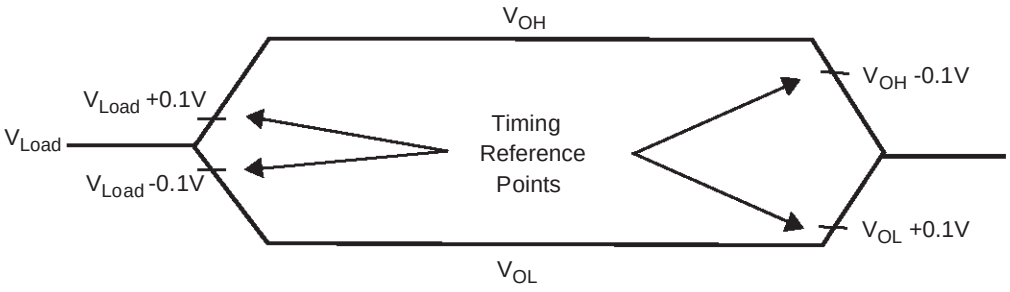
20.5.1 - Test Waveforms

Figure 16 : Input / output waveforms



AC inputs during testing are driven at 2.4V for a logic '1' and 0.4V for a logic '0'.
Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} max for a logic '0'.

Figure 17 : Float waveforms



For timing purposes a port pin is no longer floating when V_{LOAD} changes of ±100mV.
It begins to float when a 100mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20mA).

20.5.2 - Definition of Internal Timing

The internal operation of the ST10F168 is controlled by the internal CPU clock f_{CPU}. Both edges of the CPU clock can trigger internal (e.g. pipeline) or external (e.g. bus cycles) operations.

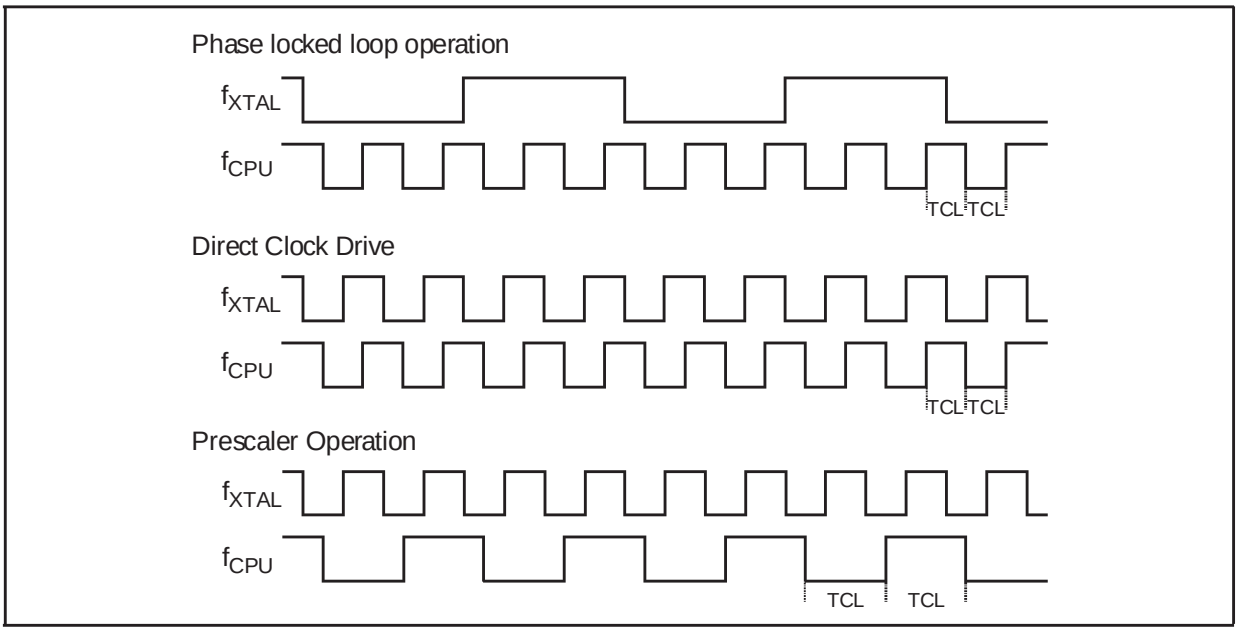
The specification of the external timing (AC Characteristics) therefore depends on the time between two consecutive edges of the CPU clock, called "TCL" (see Figure 18).

The CPU clock signal can be generated by different mechanisms. The duration of TCL and its variation (and also the derived external timing) depends on the mechanism used to generate f_{CPU}. This influence must be regarded when calculating the timings for the ST10F168.

The example for PLL operation shown in the Figure 18 refers to a PLL factor of 4.

The mechanism used to generate the CPU clock is selected during reset by the logic levels on pins P0.15-13 (P0H.7-5).

Figure 18 : Generation Mechanisms for the CPU Clock



20.5.3 - Clock Generation Modes

The Table 23 associates the combinations of these three bit with the respective clock generation mode.

Table 23 : CPU Frequency Generation

P0H.7	P0H.6	P0H.5	CPU Frequency $f_{CPU} = f_{XTAL} \times F$	External Clock Input Range[1]	Notes
1	1	1	$f_{XTAL} \times 4$	2.5 to 6.25MHz	Default configuration
1	1	0	$f_{XTAL} \times 3$	3.33 to 8.33MHz	
1	0	1	$f_{XTAL} \times 2$	5 to 12.5MHz	
1	0	0	$f_{XTAL} \times 5$	2 to 5MHz	
0	1	1	$f_{XTAL} \times 1$	1 to 25MHz	Direct drive [2]
0	1	0	$f_{XTAL} \times 1.5$	6.66 to 16.6MHz	
0	0	1	$f_{XTAL} / 2$	2 to 50MHz	CPU clock via prescaler [3]
0	0	0	$f_{XTAL} \times 2.5$	4 to 10MHz	

Notes: 1. The external clock input range refers to a CPU clock range of 1...25MHz.
2. The maximum depends on the duty cycle of the external clock signal.
3. The maximum input frequency is 25MHz when using an external crystal with the internal oscillator; providing that internal serial resistance of the crystal is less than 40Ω. However, higher frequencies can be applied with an external clock source on pin XTAL1, but in this case, the input clock signal must reach the defined levels V_{IL} and V_{IH2}.

20.5.4 - Prescaler Operation

When pins P0.15-13 (P0H.7-5) equal '001' during reset, the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.
The frequency of f_{CPU} is half the frequency of f_{XTAL} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{XTAL}.

The timings listed in the AC Characteristics that refer to TCL therefore can be calculated using the period of f_{XTAL} for any TCL.

Note that if the bit OWDDIS in SYSCON register is cleared, the PLL runs on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

20.5.5 - Direct Drive

When pins P0.15-13 (P0H.7-5) equal '011' during reset the on-chip phase locked loop is disabled and the CPU clock is directly driven from the internal oscillator with the input clock signal.
The frequency of f_{CPU} directly follows the frequency of f_{XTAL} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{XTAL}.

Therefore, the timings given in this chapter refer to the minimum TCL. This minimum value can be calculated by the following formula:

$$TCL_{min} = 1/f_{XTAL} \times DC_{min}$$

$$DC = \text{duty cycle}$$

For two consecutive TCLs, the deviation caused by the duty cycle of f_{XTAL} is compensated, so the duration of 2TCL is always $1/f_{XTAL}$. The minimum value TCL_{min} has to be used only once for timings that require an odd number of TCLs (1,3,...). Timings that require an even number of TCLs (2,4,...) may use the formula:

$$2TCL = 1/f_{XTAL}$$

Note: The address float timings in Multiplexed bus mode (t_{11} and t_{45}) use the maximum duration of TCL (TCL_{max} = $1/f_{XTAL}$ x DC_{max}) instead of TCL_{min}.

If bit OWDDIS in the SYSCON register is cleared, the PLL runs on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

20.5.6 - Oscillator Watchdog (OWD)

When the clock option selected is direct drive or direct drive with prescaler, in order to provide a fail safe mechanism in case of a loss of the external clock, an oscillator watchdog is implemented as an additional functionality of the PLL circuitry. This oscillator watchdog operates as follows :
After a reset, the Oscillator Watchdog is enabled by default. To disable the OWD, the bit OWDDIS (bit 4 of SYSCON register) must be set.

When the OWD is enabled, the PLL runs on its free-running frequency, and increments the Oscillator Watchdog counter. On each transition of XTAL1 pin, the Oscillator Watchdog is cleared. If an external clock failure occurs, then the Oscillator Watchdog counter overflows (after 16 PLL clock cycles). The CPU clock signal will be switched to the PLL free-running clock signal, and the Oscillator Watchdog Interrupt Request (XP3INT) is flagged. The CPU clock will not switch back to the external clock even if a valid external clock exits on XTAL1 pin. Only a hardware reset can switch the CPU clock source back to direct clock input.

When the OWD is disabled, the CPU clock is always fed from the oscillator input and the PLL is switched off to decrease power supply current.

20.5.7 - Phase Locked Loop

For all other combinations of pins P0.15-13 (P0H.7-5) during reset the on-chip phase locked loop is enabled and provides the CPU clock (see Table 23).

The PLL multiplies the input frequency by the factor F which is selected via the combination of pins P0.15-13 (i.e. f_{CPU} = f_{XTAL} x F). With every F'th transition of f_{XTAL} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothly, i.e. the CPU clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{XTAL}. The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCL.

The timings listed in the AC Characteristics that refer to TCL therefore must be calculated using the minimum TCL that is possible under the respective circumstances.

The real minimum value for TCL depends on the jitter of the PLL. The PLL tunes f_{CPU} to keep it locked on f_{XTAL}. The relative deviation of TCL is the maximum when it is refered to one TCL period. It decreases according to the formula and to the Figure 19 given below. For *N* periods of TCL the minimum value is computed using the corresponding deviation D_N:

$$TCL_{MIN} = TCL_{NOM} \times \left(1 - \frac{\left[D_N\right]}{100}\right)$$

$$D_N = \pm(4 - N/15)[\%]$$

where N = number of consecutive TCL periods and $1 \le N \le 40$. So for a period of 3 TCL periods (N = 3):

D_3 = 4 - 3/15 = 3.8%

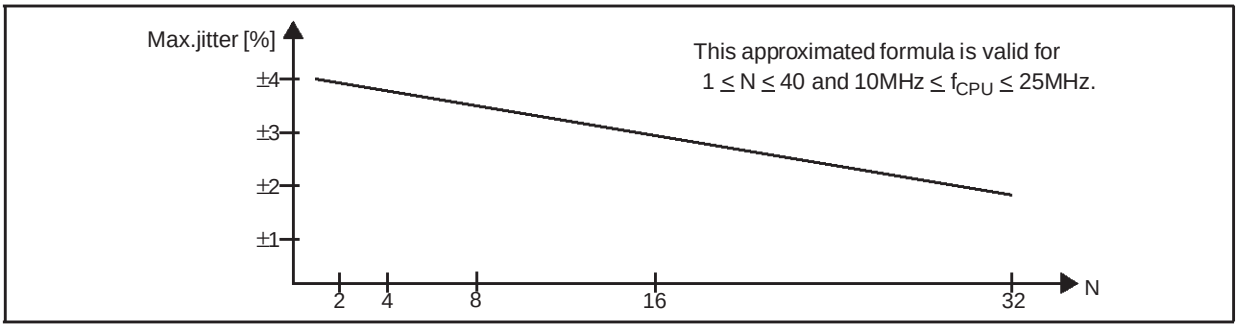
$3TCL_{min} = 3TCL_{NOM}$ x (1 - 3.8/100)

$= 3TCL_{NOM}$ x 0.962

$3TCL_{min}$ = (57.72ns at f_{CPU} = 25MHz)

This is especially important for bus cycles using wait states and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower Baud rates, etc.) the deviation caused by the PLL jitter is negligible (see Figure 19).

Figure 19 : Approximated maximum PLL jitter



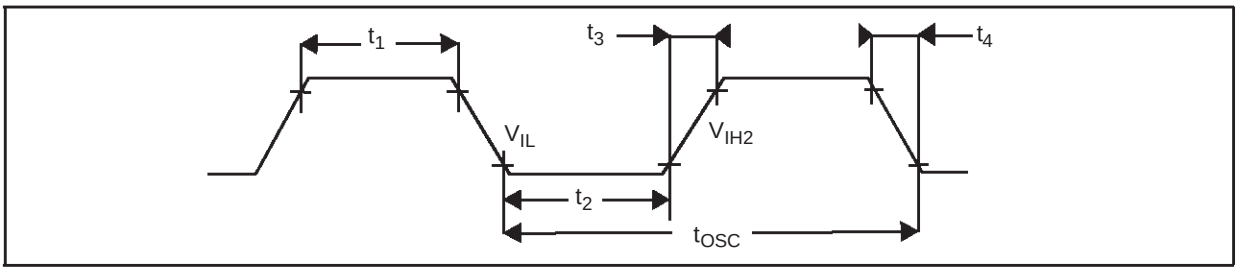
20.5.8 - External Clock Drive XTAL1

V_{DD} = 5V ± 10%, V_{SS} = 0V, for Q6 version : T_A = -40, +85°C and for Q3 version T_A = -40, + 125°C, unless otherwise specified.

Symbol		Parameter	$f_{CPU} = f_{XTAL}$		$f_{CPU} = f_{XTAL} / 2$		$f_{CPU} = f_{XTAL}$ x N N = 1.5 / 2 / 2.5 / 3 / 4 / 5		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{OSC}	SR	Oscillator period	40 [1]	1000	20	500	40 x N	100 x N	ns
t_1	SR	High time	18 [2]	–	6 [2]	–	10 [2]	–	ns
t_2	SR	Low time	18 [2]	–	6 [2]	–	10 [2]	–	ns
t_3	SR	Rise time	–	10 [2]	–	6 [3]	–	10 [2]	ns
t_4	SR	Fall time	–	10 [2]	–	6 [2]	–	10 [2]	ns

Notes: 1. Theoretical minimum. The real minimum value depends on the duty cycle of the input clock signal.
2. The input clock signal must reach the defined levels V_{IL} and V_{IH2}.

Figure 20 : External clock drive XTAL1



20.5.9 - Memory Cycle Variables

The tables below use three variables which are derived from the BUSCONx registers and which represent the special characteristics of the programmed memory cycle. The following table describes how these variables are computed.

Symbol	Description	Values
t_A	ALE Extension	TCL x <ALECTL>
t_C	Memory Cycle Time wait states	2TCL x (15 - <MCTC>)
t_F	Memory Tristate Time	2TCL x (1 - <MTTC>)

20.5.10 - Multiplexed Bus

V_{DD} = 5V ±10%, V_{SS} = 0V, for Q6 version : T_A = -40, +85°C and for Q3 version T_A = -40, + 125°C, C_L = 100pF, ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (120ns at 25MHz CPU clock without wait states), unless otherwise specified.

Table 24 : Multiplexed bus characteristics

Symbol		Parameter	Maximum CPU Clock 25MHz		Variable CPU Clock 1/2 TCL = 1 to 25MHz		Unit
			Minimum	Maximum	Minimum	Maximum	
t_5	CC	ALE high time	10 + t_A	–	TCL - 10 + t_A	–	ns
t_6	CC	Address setup to ALE	4 + t_A	–	TCL - 16+ t_A	–	ns
t_7	CC	Address hold after ALE	10 + t_A	–	TCL - 10 + t_A	–	ns
t_8	CC	ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	10 + t_A	–	TCL - 10 + t_A	–	ns
t_9	CC	ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	-10 + t_A	–	-10 + t_A	–	ns
t_{10}	CC	Address float after $\overline{RD}$, $\overline{WR}$ [1] (with RW-delay)	–	6	–	6	ns
t_{11}	CC	Address float after $\overline{RD}$, $\overline{WR}$ [1] (no RW-delay)	–	26	–	TCL + 6	ns
t_{12}	CC	$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	30 + t_C	–	2TCL - 10 + t_C	–	ns
t_{13}	CC	$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	50 + t_C	–	3TCL - 10 + t_C	–	ns
t_{14}	SR	$\overline{RD}$ to valid data in (with RW-delay)	–	20 + t_C	–	2TCL - 20+ t_C	ns
t_{15}	SR	$\overline{RD}$ to valid data in (no RW-delay)	–	40 + t_C	–	3TCL - 20+ t_C	ns
t_{16}	SR	ALE low to valid data in	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
t_{17}	SR	Address / Unlatched $\overline{CS}$ to valid data in	–	50 + $2t_A$ + t_C	–	4TCL - 30 + $2t_A$ + t_C	ns
t_{18}	SR	Data hold after $\overline{RD}$ rising edge	0	–	0	–	ns
t_{19}	SR	Data float after $\overline{RD}$ [1]	–	26 + t_F	–	2TCL - 14 + t_F	ns
t_{22}	CC	Data valid to $\overline{WR}$	20 + t_C	–	2TCL - 20 + t_C	–	ns

Table 24 : Multiplexed bus characteristics (continued)

Symbol		Parameter	Maximum CPU Clock 25MHz		Variable CPU Clock 1/2 TCL = 1 to 25MHz		Unit
			Minimum	Maximum	Minimum	Maximum	
t_{23}	CC	Data hold after $\overline{WR}$	26 + t_F	–	2TCL - 14 + t_F	–	ns
t_{25}	CC	ALE rising edge after $\overline{RD}$, $\overline{WR}$	26 + t_F	–	2TCL - 14 + t_F	–	ns
t_{27}	CC	Address / Unlatched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	26 + t_F	–	2TCL - 14 + t_F	–	ns
t_{38}	CC	ALE falling edge to Latched $\overline{CS}$	-4 - t_A	10 - t_A	-4 - t_A	10 - t_A	ns
t_{39}	SR	Latched $\overline{CS}$ low to Valid Data In	–	40 + t_C + 2t_A	–	3TCL - 20 + t_C + 2t_A	ns
t_{40}	CC	Latched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	46 + t_F	–	3TCL - 14 + t_F	–	ns
t_{42}	CC	ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	16 + t_A	–	TCL - 4 + t_A	–	ns
t_{43}	CC	ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	-4 + t_A	–	-4 + t_A	–	ns
t_{44}	CC	Address float after $\overline{RdCS}$, $\overline{WrCS}$ [1] (with RW delay)	–	0	–	0	ns
t_{45}	CC	Address float after $\overline{RdCS}$, $\overline{WrCS}$ [1] (no RW delay)	–	20	–	TCL	ns
t_{46}	SR	$\overline{RdCS}$ to Valid Data In (with RW delay)	–	16 + t_C	–	2TCL - 24 + t_C	ns
t_{47}	SR	$\overline{RdCS}$ to Valid Data In (no RW delay)	–	36 + t_C	–	3TCL - 24 + t_C	ns
t_{48}	CC	$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW delay)	30 + t_C	–	2TCL - 10 + t_C	–	ns
t_{49}	CC	$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW delay)	50 + t_C	–	3TCL - 10 + t_C	–	ns
t_{50}	CC	Data valid to $\overline{WrCS}$	26 + t_C	–	2TCL - 14+ t_C	–	ns
t_{51}	SR	Data hold after $\overline{RdCS}$	0	–	0	–	ns
t_{52}	SR	Data float after $\overline{RdCS}$ [1]	–	20 + t_F	–	2TCL - 20 + t_F	ns
t_{54}	CC	Address hold after $\overline{RdCS}$, $\overline{WrCS}$	20 + t_F	–	2TCL - 20 + t_F	–	ns
t_{56}	CC	Data hold after $\overline{WrCS}$	20 + t_F	–	2TCL - 20 + t_F	–	ns

Note: 1. Partially tested, guaranteed by design characterization.

Figure 21 : External Memory Cycle : multiplexed bus, with / without read/write delay, normal ALE

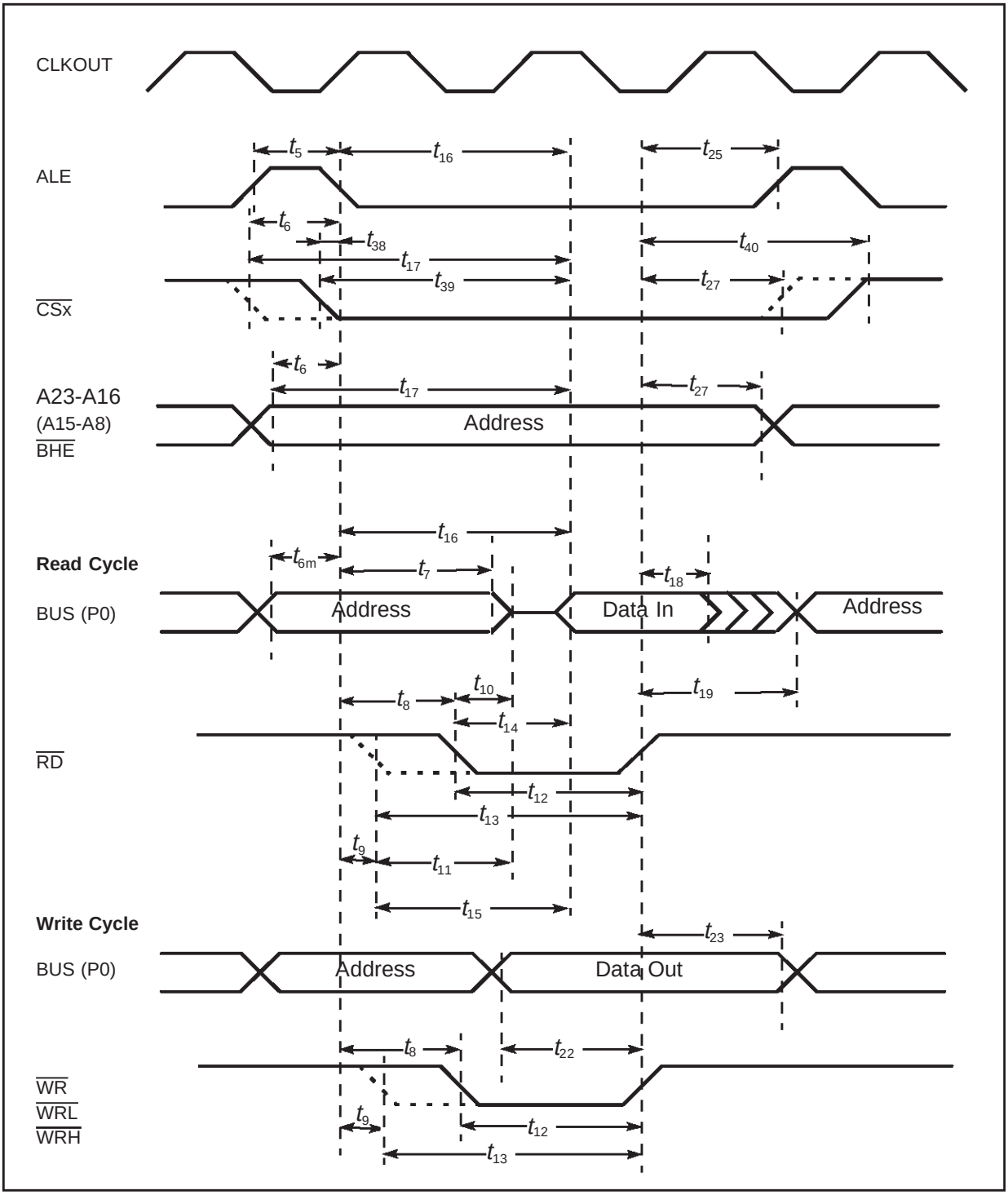


Figure 22 : External Memory Cycle: multiplexed bus, with / without read/write delay, extended ALE

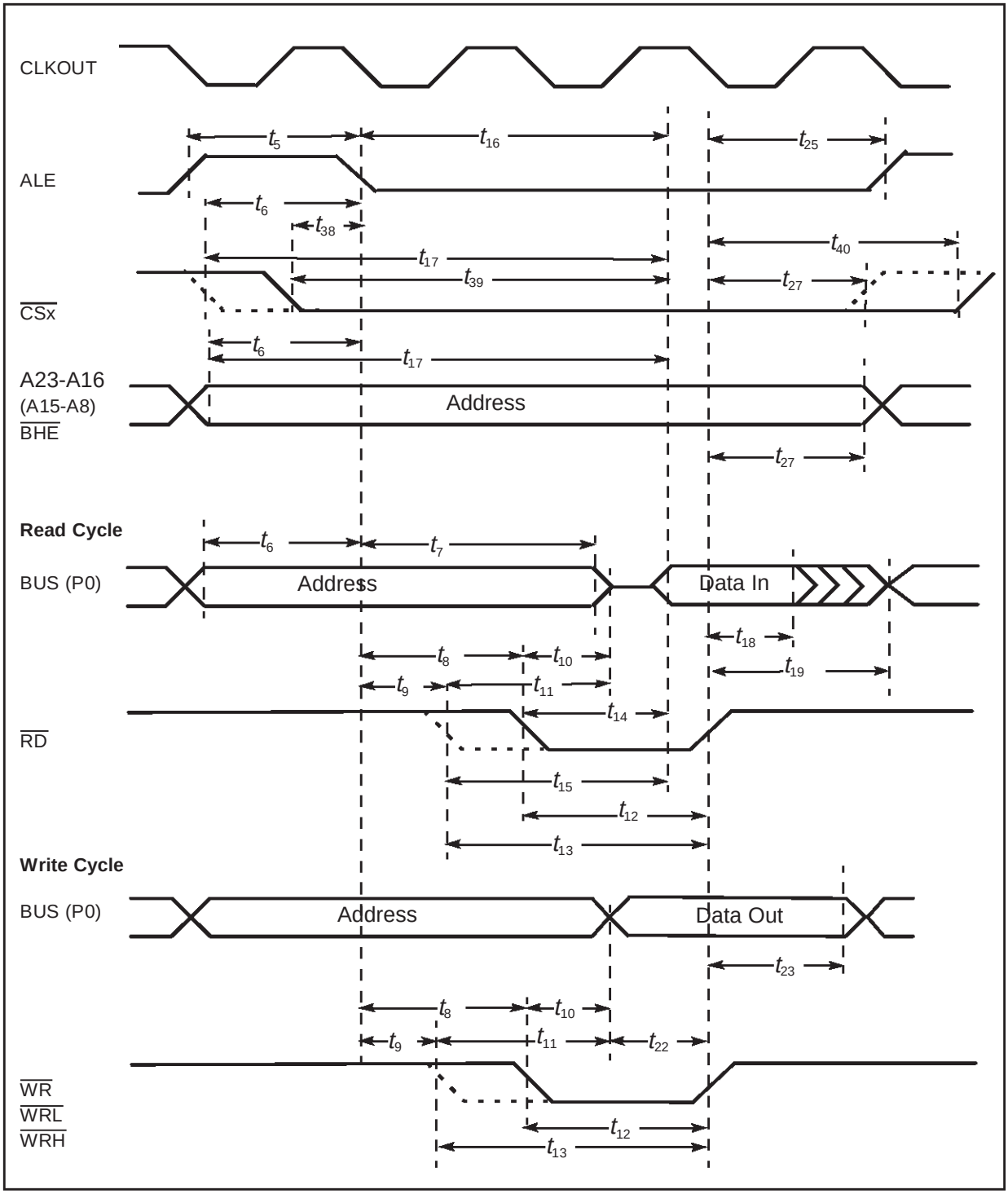


Figure 23 : External Memory Cycle: multiplexed bus, with / without read/write delay, normal ALE, read/write chip select

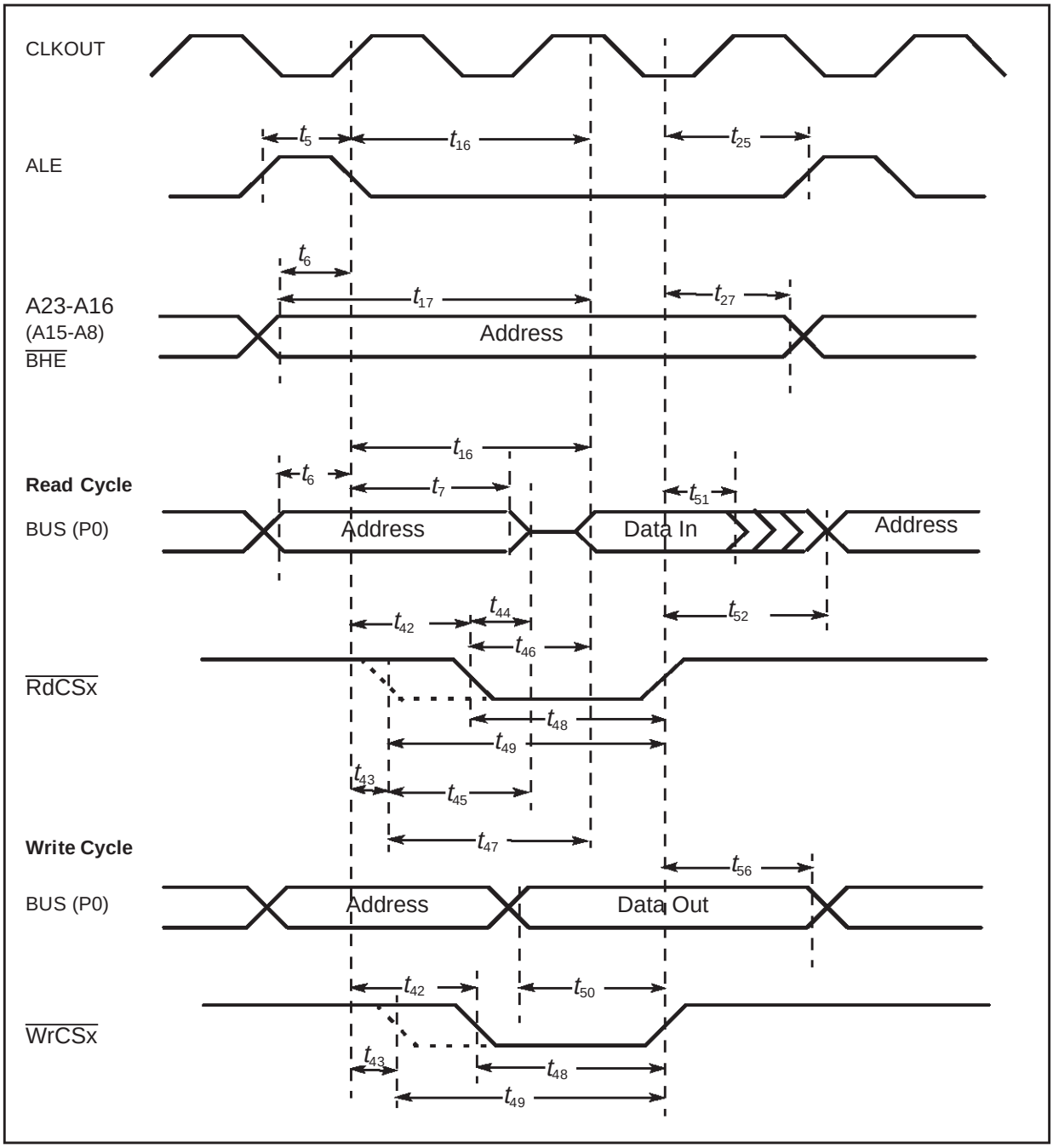
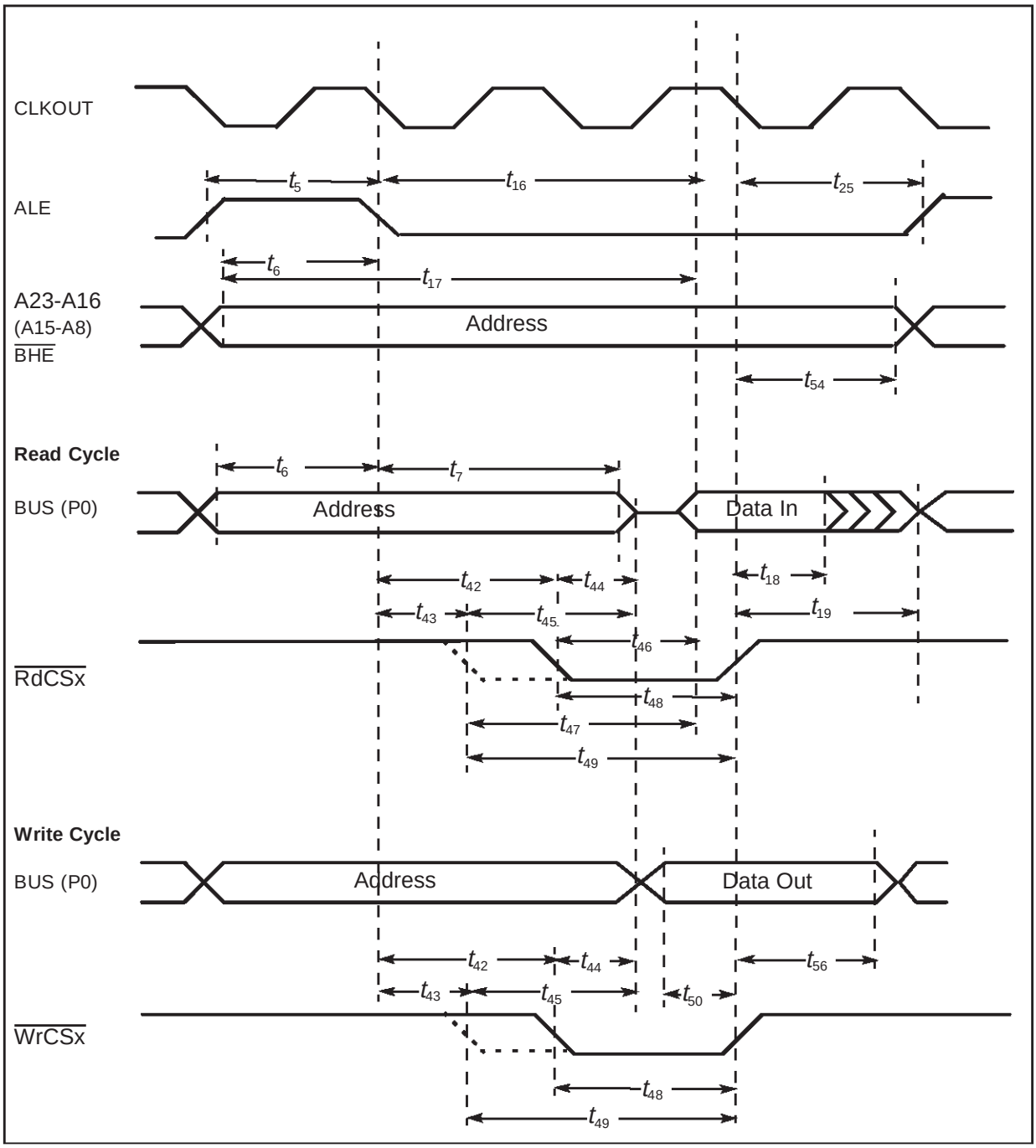


Figure 24 : External Memory Cycle: multiplexed bus, with / without read/write delay, extended ALE, read/write chip select



20.5.11 - Demultiplexed Bus

V_{DD} = 5V ±10%, V_{SS} = 0V, for Q6 version : T_A = -40, +85°C and for Q3 version T_A = -40, +125°C, C_L = 100pF, ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (80ns at 25MHz CPU clock without wait states), unless otherwise specified.

Table 25 : Demultiplexed bus characteristics

Symbol		Parameter	Maximum CPU Clock = 25MHz		Variable CPU Clock 1/2 TCL = 1 to 25MHz		Unit
			Minimum	Maximum	Minimum	Maximum	
t_5	CC	ALE high time	10 + t_A	–	TCL - 10+ t_A	–	ns
t_6	CC	Address setup to ALE	4 + t_A	–	TCL - 16+ t_A	–	ns
t_{80}	CC	Address / Unlatched $\overline{CS}$ setup to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	30 + $2t_A$	–	2TCL - 10 + $2t_A$	–	ns
t_{81}	CC	Address / Unlatched $\overline{CS}$ setup to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	10 + $2t_A$	–	TCL -10 + $2t_A$	–	ns
t_{12}	CC	$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	30 + t_C	–	2TCL - 10 + t_C	–	ns
t_{13}	CC	$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	50 + t_C	–	3TCL - 10 + t_C	–	ns
t_{14}	SR	$\overline{RD}$ to valid data in (with RW-delay)	–	20 + t_C	–	2TCL - 20 + t_C	ns
t_{15}	SR	$\overline{RD}$ to valid data in (no RW-delay)	–	40 + t_C	–	3TCL - 20 + t_C	ns
t_{16}	SR	ALE low to valid data in	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
t_{17}	SR	Address / Unlatched $\overline{CS}$ to valid data in	–	50 + $2t_A$ + t_C	–	4TCL - 30 + $2t_A$ + t_C	ns
t_{18}	SR	Data hold after $\overline{RD}$ rising edge	0	–	0	–	ns
t_{20}	SR	Data float after $\overline{RD}$ rising edge (with RW-delay)[1 2]	–	26 + t_F	–	2TCL - 14 + t_F + $2t_A$[1]	ns
t_{21}	SR	Data float after $\overline{RD}$ rising edge (no RW-delay)[1 2]	–	10 + t_F	–	TCL - 10 + t_F + $2t_A$[1]	ns
t_{22}	CC	Data valid to $\overline{WR}$	20 + t_C	–	2TCL- 20 + t_C	–	ns
t_{24}	CC	Data hold after $\overline{WR}$	10 + t_F	–	TCL - 10+ t_F	–	ns
t_{26}	CC	ALE rising edge after $\overline{RD}$, $\overline{WR}$	-10 + t_F	–	-10 + t_F	–	ns
t_{28}	CC	Address / Unlatched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$ [3]	0 (no t_F) -5 + t_F (t_F > 0)	–	0 (no t_F) -5 + t_F (t_F > 0)	–	ns
t_{28h}	CC	Address / Unlatched $\overline{CS}$ hold after $\overline{WRH}$	-5 + t_F	–	-5 + t_F	–	ns
t_{38}	CC	ALE falling edge to Latched $\overline{CS}$	-4 - t_A	10 - t_A	-4 - t_A	10 - t_A	ns

Table 25 : Demultiplexed bus characteristics (continued)

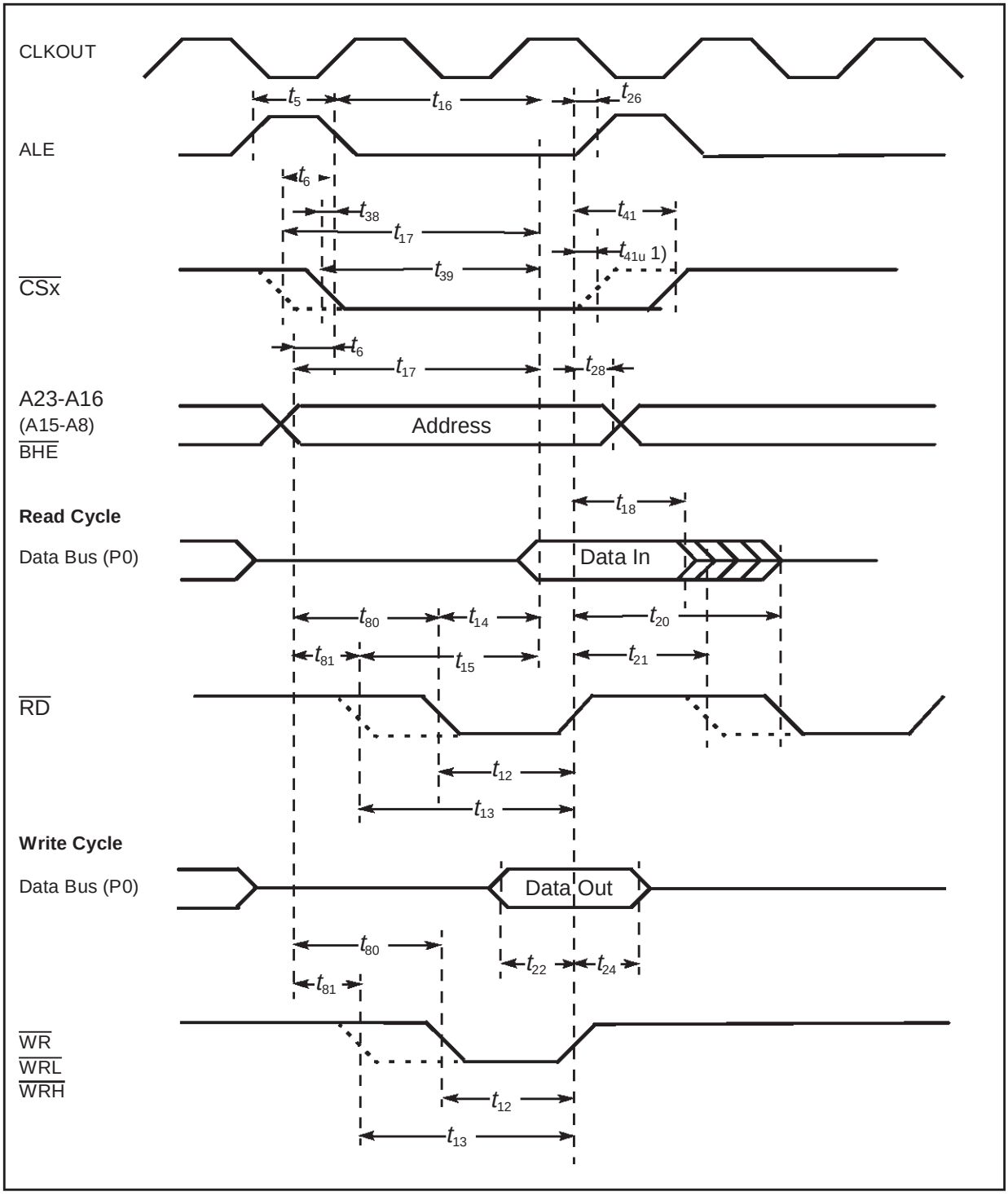
Symbol		Parameter	Maximum CPU Clock = 25MHz		Variable CPU Clock 1/2 TCL = 1 to 25MHz		Unit
			Minimum	Maximum	Minimum	Maximum	
t_{39}	SR	Latched $\overline{CS}$ low to Valid Data In	–	40 + t_C + 2t_A	–	3TCL - 20 + t_C + 2t_A	ns
t_{41}	CC	Latched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	6 + t_F	–	TCL - 14 + t_F	–	ns
t_{82}	CC	Address setup to $\overline{RdCS}$, $\overline{WrCS}$ (with RW-delay)	26 + 2t_A	–	2TCL - 14 + 2t_A	–	ns
t_{83}	CC	Address setup to $\overline{RdCS}$, $\overline{WrCS}$ (no RW-delay)	6 + 2t_A	–	TCL -14 + 2t_A	–	ns
t_{46}	SR	$\overline{RdCS}$ to Valid Data In (with RW-delay)	–	16 + t_C	–	2TCL - 24 + t_C	ns
t_{47}	SR	$\overline{RdCS}$ to Valid Data In (no RW-delay)	–	36 + t_C	–	3TCL - 24 + t_C	ns
t_{48}	CC	$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW-delay)	30 + t_C	–	2TCL - 10 + t_C	–	ns
t_{49}	CC	$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW-delay)	50 + t_C	–	3TCL - 10 + t_C	–	ns
t_{50}	CC	Data valid to $\overline{WrCS}$	26 + t_C	–	2TCL - 14 + t_C	–	ns
t_{51}	SR	Data hold after $\overline{RdCS}$	0	–	0	–	ns
t_{53}	SR	Data float after $\overline{RdCS}$ (with RW-delay) [2]	–	20 + t_F	–	2TCL - 20 + t_F	ns
t_{68}	SR	Data float after $\overline{RdCS}$ (no RW-delay) [2]	–	0 + t_F	–	TCL - 20 + t_F	ns
t_{55}	CC	Address hold after $\overline{RdCS}$, $\overline{WrCS}$	-10 + t_F	–	-10 + t_F	–	ns
t_{57}	CC	Data hold after $\overline{WrCS}$	6 + t_F	–	TCL - 14 + t_F	–	ns

Notes: 1. RW-delay and t_A refer to the following bus cycle.

2. Partially tested, guaranteed by design characterization.

3. Read data is latched with the same clock edge that triggers the address change and the rising $\overline{RD}$ edge. Therefore address changes before the end of $\overline{RD}$ have no impact on read cycles.

Figure 25 : External Memory Cycle: demultiplexed bus, with / without read/write delay, normal ALE



Note: 1. Un-latched CSx = t_{41u} = t_{41} - TCL = -14 + t_F

Figure 26 : External Memory Cycle: demultiplexed bus, with / without read/write delay, extended ALE

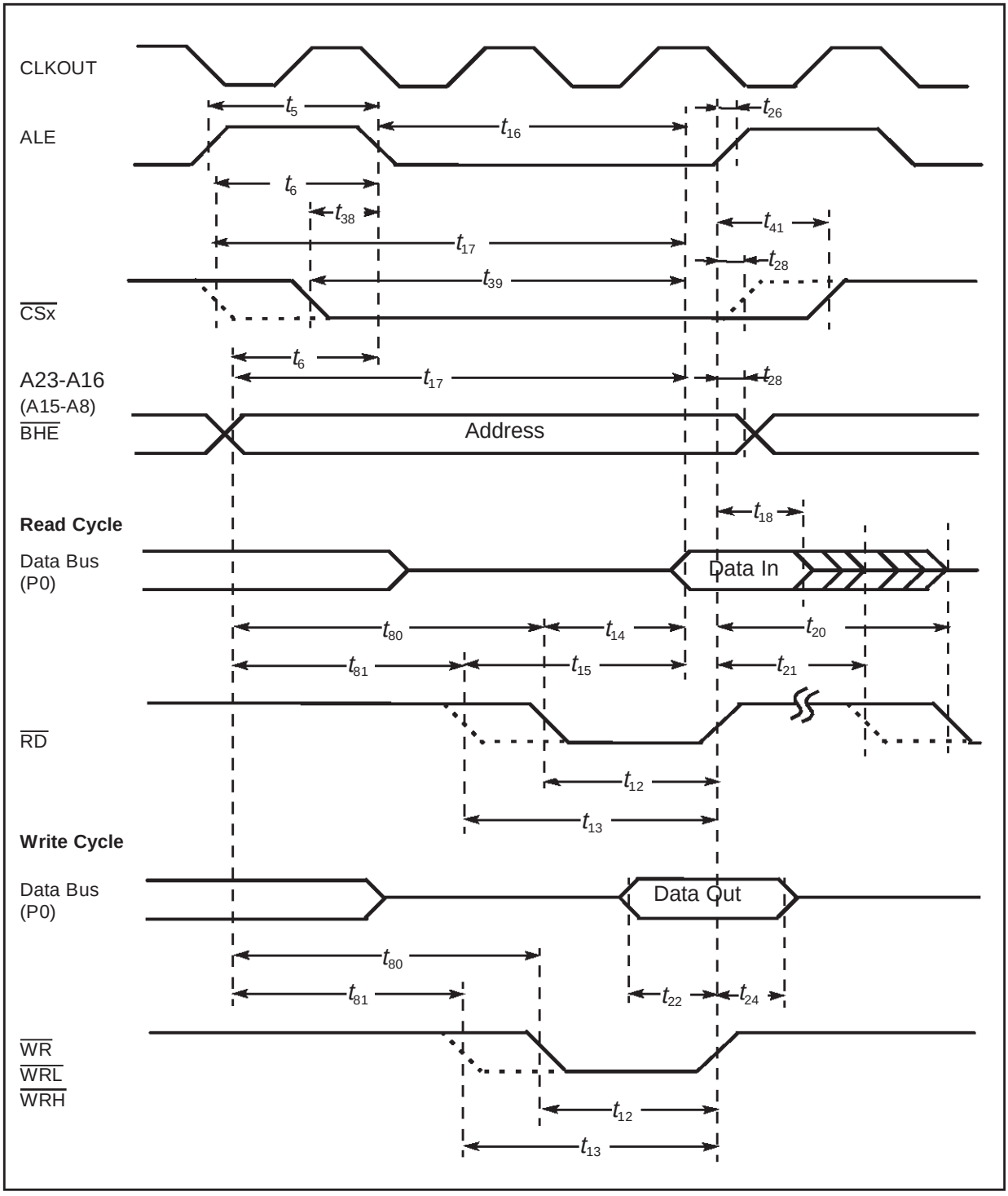


Figure 27 : External Memory Cycle: demultiplexed bus, with / without read/write delay, normal ALE, read/write chip select

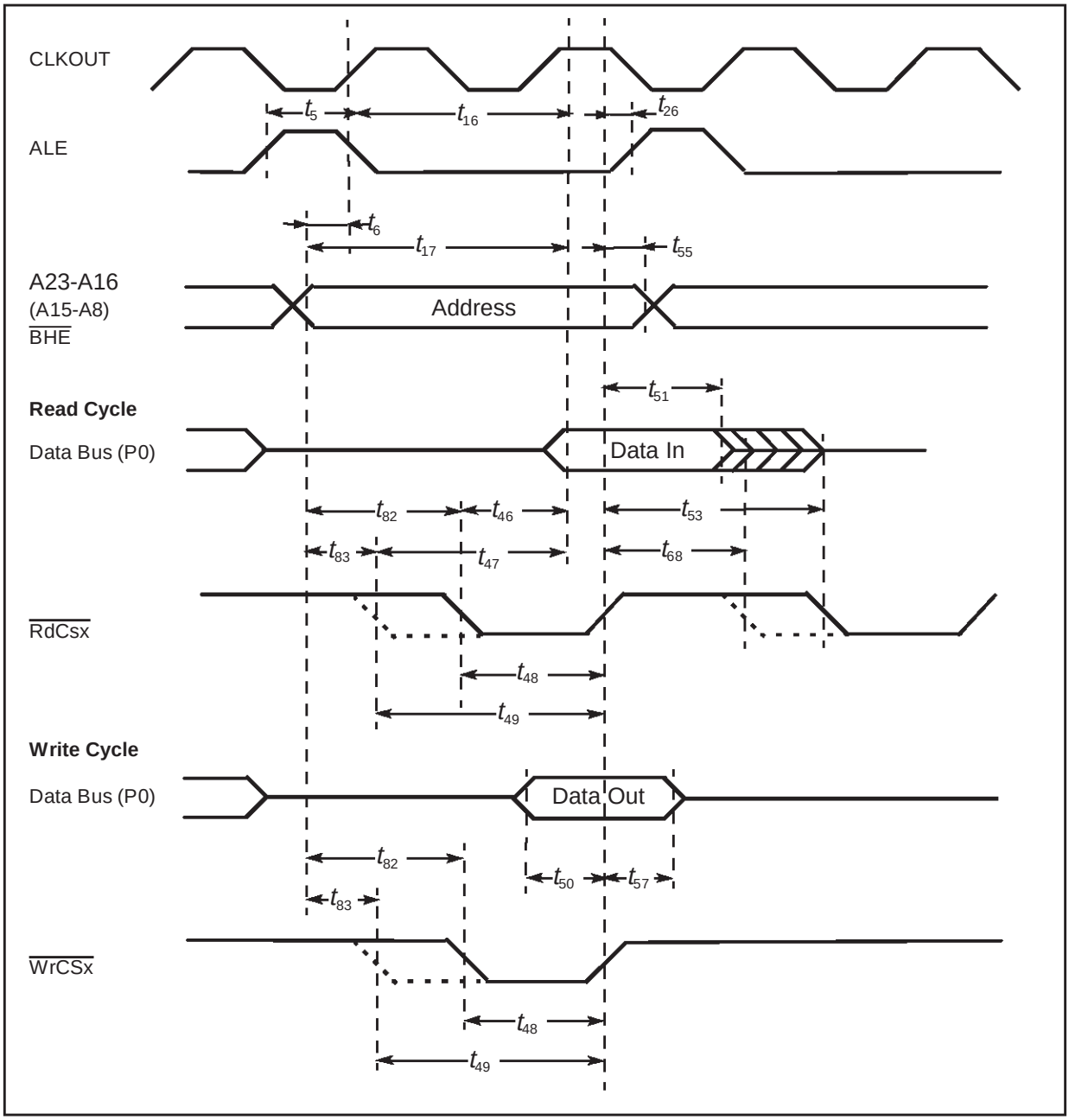
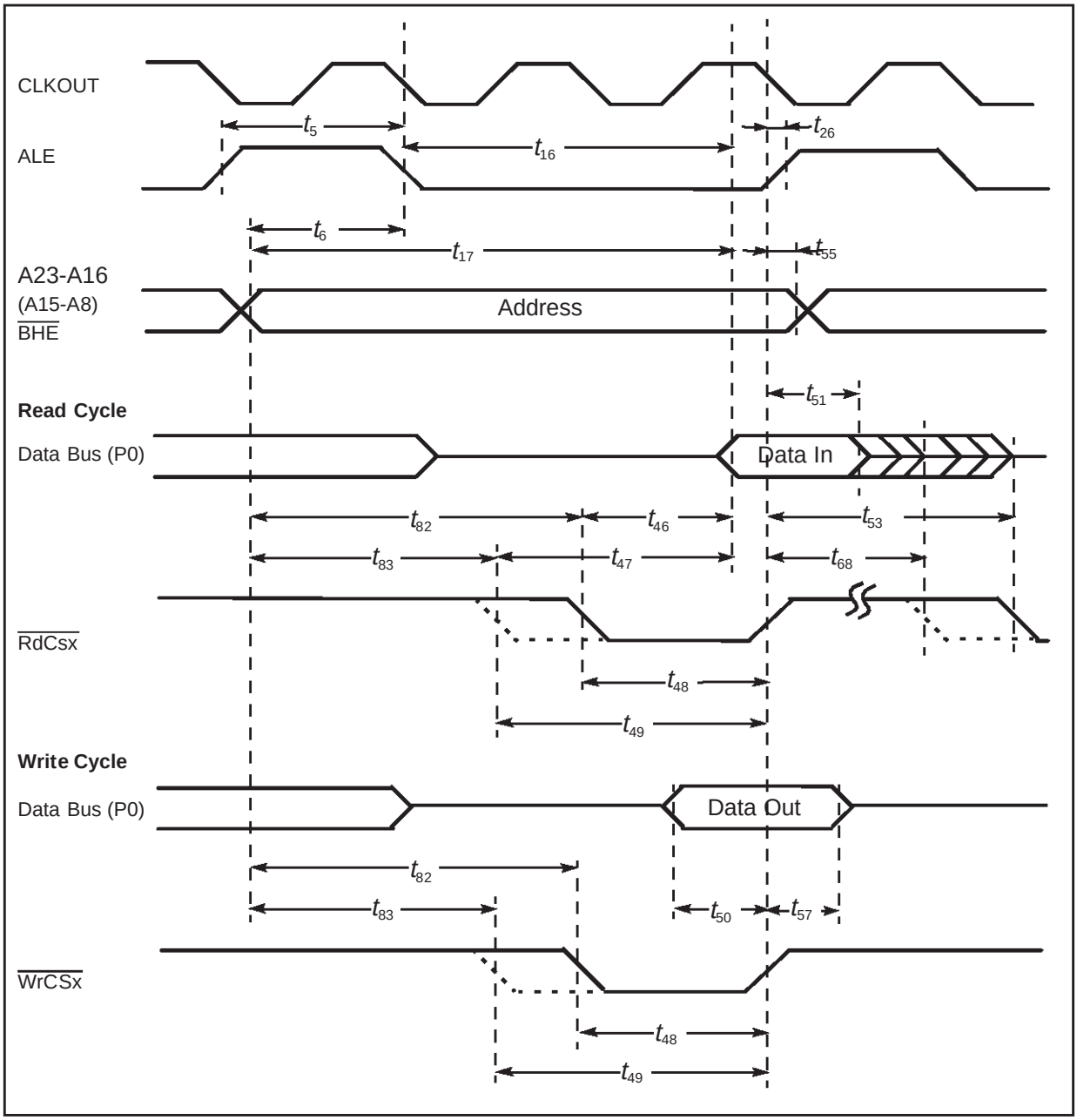


Figure 28 : External Memory Cycle: demultiplexed bus, no read/write delay, extended ALE, read/write chip select



20.5.12 - CLKOUT and $\overline{READY}$

V_{DD} = 5V ±10%, V_{SS} = 0V, for Q6 version : T_A = -40, +85°C and for Q3 version T_A = -40, +125°C, C_L = 100pF, unless otherwise specified

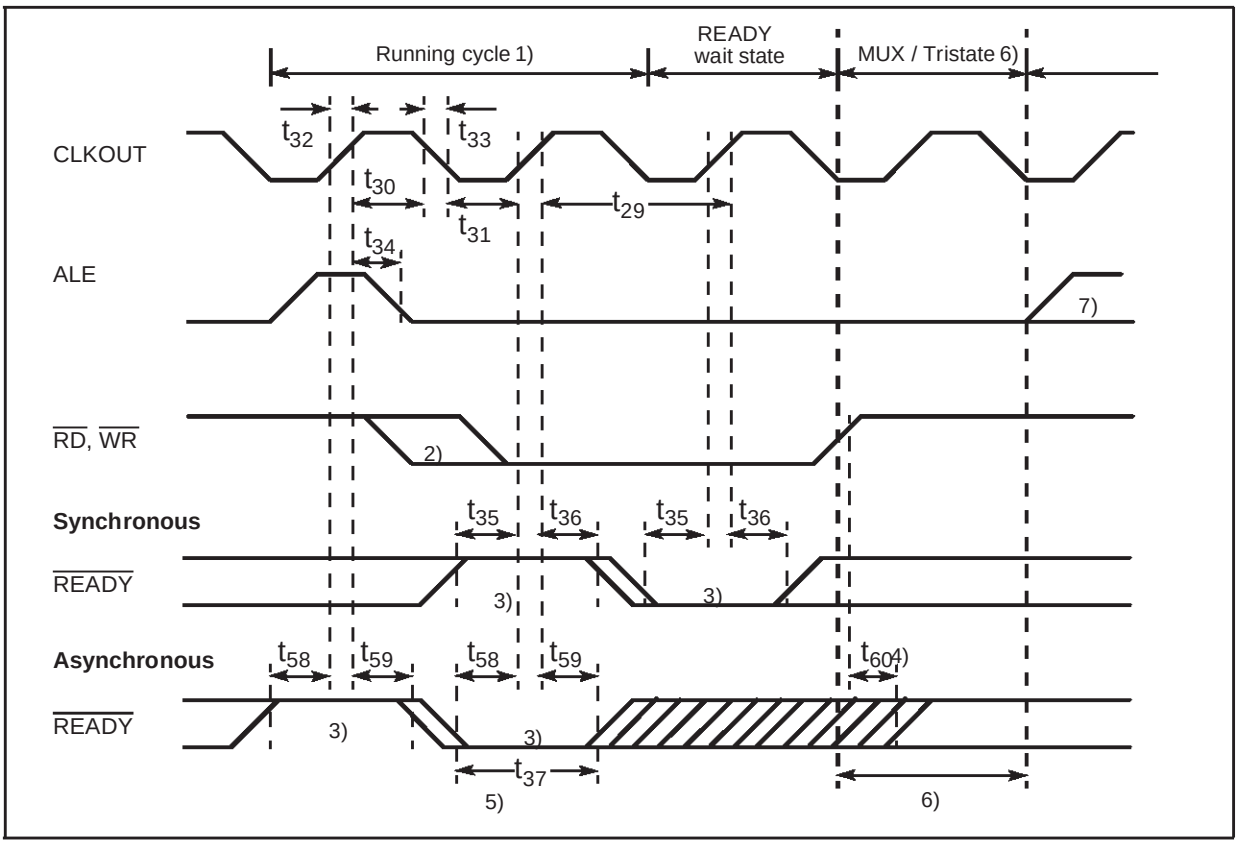
Table 26 : CLKOUT and $\overline{READY}$ characteristics

Symbol		Parameter	Max. CPU Clock 25MHz		Variable CPU Clock 1/2 TCL = 1 to 25MHz		Unit
			Minimum	Maximum	Minimum	Maximum	
t_{29}	CC	CLKOUT cycle time	40	40	2TCL	2TCL	ns
t_{30}	CC	CLKOUT high time	14	–	TCL – 6	–	ns
t_{31}	CC	CLKOUT low time	10	–	TCL – 10	–	ns
t_{32}	CC	CLKOUT rise time	–	4	–	4	ns
t_{33}	CC	CLKOUT fall time	–	4	–	4	ns
t_{34}	CC	CLKOUT rising edge to ALE falling edge	$-3 + t_A$	$+7 + t_A$	$-3 + t_A$	$7 + t_A$	ns
t_{35}	SR	Synchronous $\overline{READY}$ setup time to CLKOUT	14	–	14	–	ns
t_{36}	SR	Synchronous $\overline{READY}$ hold time after CLKOUT	4	–	4	–	ns
t_{37}	SR	Asynchronous $\overline{READY}$ low time	54	–	2TCL + 14	–	ns
t_{58}	SR	Asynchronous $\overline{READY}$ setup time [1]	14	–	14	–	ns
t_{59}	SR	Asynchronous $\overline{READY}$ hold time [1]	4	–	4	–	ns
t_{60}	SR	Async. $\overline{READY}$ hold time after $\overline{RD}$, $\overline{WR}$ high (Demultiplexed Bus) [2]	0	$0 + 2t_A + t_C + t_F$ [2]	0	TCL - 20 $+ 2t_A + t_C + t_F$ [2]	ns

Notes: 1. These timings are given for test purposes only, in order to assure recognition at a specific clock edge.

2. Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating READY.
The $2t_A$ and t_C refer to the next following bus cycle, t_F refers to the current bus cycle.

Figure 29 : CLKOUT and $\overline{\text{READY}}$



Notes: 1. Cycle as programmed, including MCTC wait states (Example shows 0 MCTC WS).

2. The leading edge of the respective command depends on RW-delay.

3. $\overline{\text{READY}}$ sampled HIGH at this sampling point generates a READY controlled wait state, $\overline{\text{READY}}$ sampled LOW at this sampling point terminates the currently running bus cycle.

4. $\overline{\text{READY}}$ may be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).

5. If the Asynchronous $\overline{\text{READY}}$ signal does not fulfill the indicated setup and hold times with respect to CLKOUT (e.g. because CLKOUT is not enabled), it must fulfill t_{37} in order to be safely synchronized. This is guaranteed, if READY is removed in response to the command (see Note 4)).

6. Multiplexed bus modes have a MUX wait state added after a bus cycle, and an additional MTTC wait state may be inserted here. For a multiplexed bus with MTTC wait state this delay is 2 CLKOUT cycles, for a demultiplexed bus without MTTC wait state this delay is zero.

7. The next external bus cycle may start here.

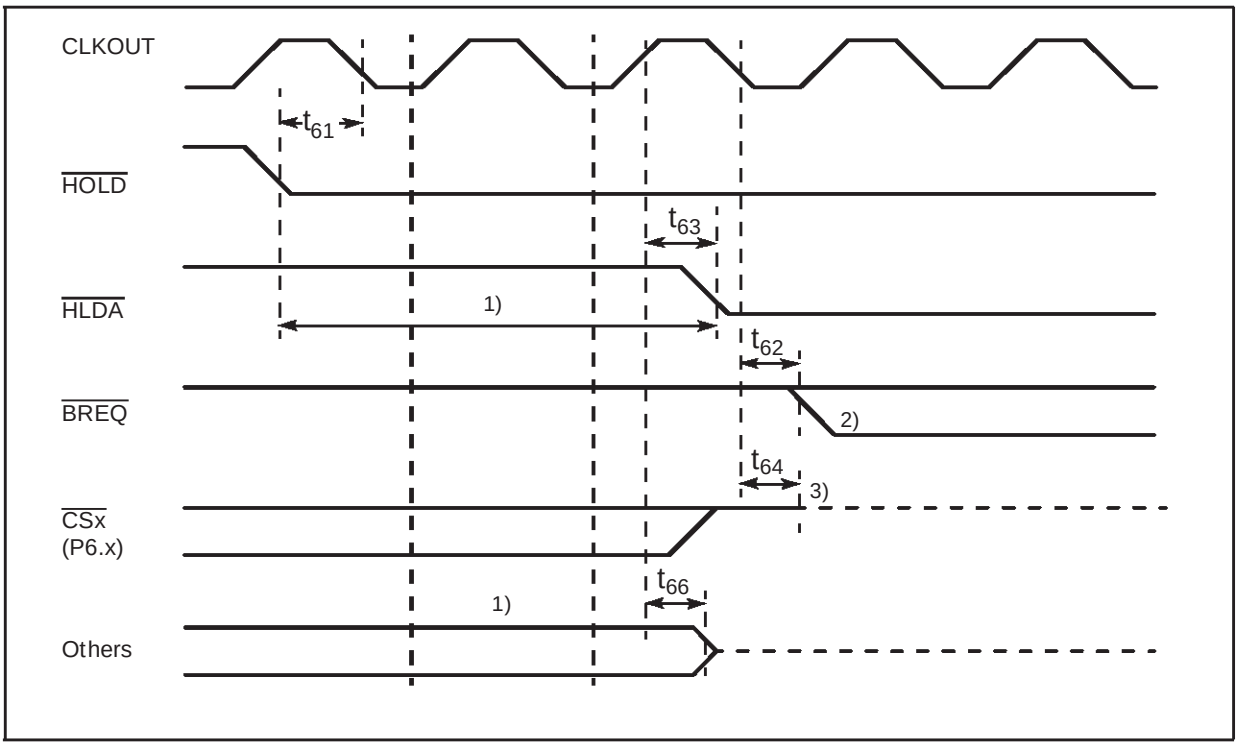
20.5.13 - External Bus Arbitration

V_{DD} = 5V ± 10%, V_{SS} = 0V, for Q6 version : T_A = -40, +85°C and for Q3 version T_A = -40, +125°C, C_L = 100pF, unless otherwise specified.

Symbol		Parameter	Max. CPU Clock 25MHz		Variable CPU Clock 1/2 TCL = 1 to 25MHz		Unit
			Minimum	Maximum	Minimum	Maximum	
t_{61}	SR	$\overline{HOLD}$ input setup time to CLKOUT	20	–	20	–	ns
t_{62}	CC	CLKOUT to $\overline{HLDA}$ high or $\overline{BREQ}$ low delay	–	20	–	20	ns
t_{63}	CC	CLKOUT to $\overline{HLDA}$ low or $\overline{BREQ}$ high delay	–	20	–	20	ns
t_{64}	CC	$\overline{CSx}$ release [1]	–	20	–	20	ns
t_{65}	CC	$\overline{CSx}$ drive	-4	24	-4	24	ns
t_{66}	CC	Other signals release [1]	–	20	–	20	ns
t_{67}	CC	Other signals drive	-4	24	-4	24	ns

Note: 1. Partially tested, guaranted by design characterization.

Figure 30 : External bus arbitration, releasing the bus

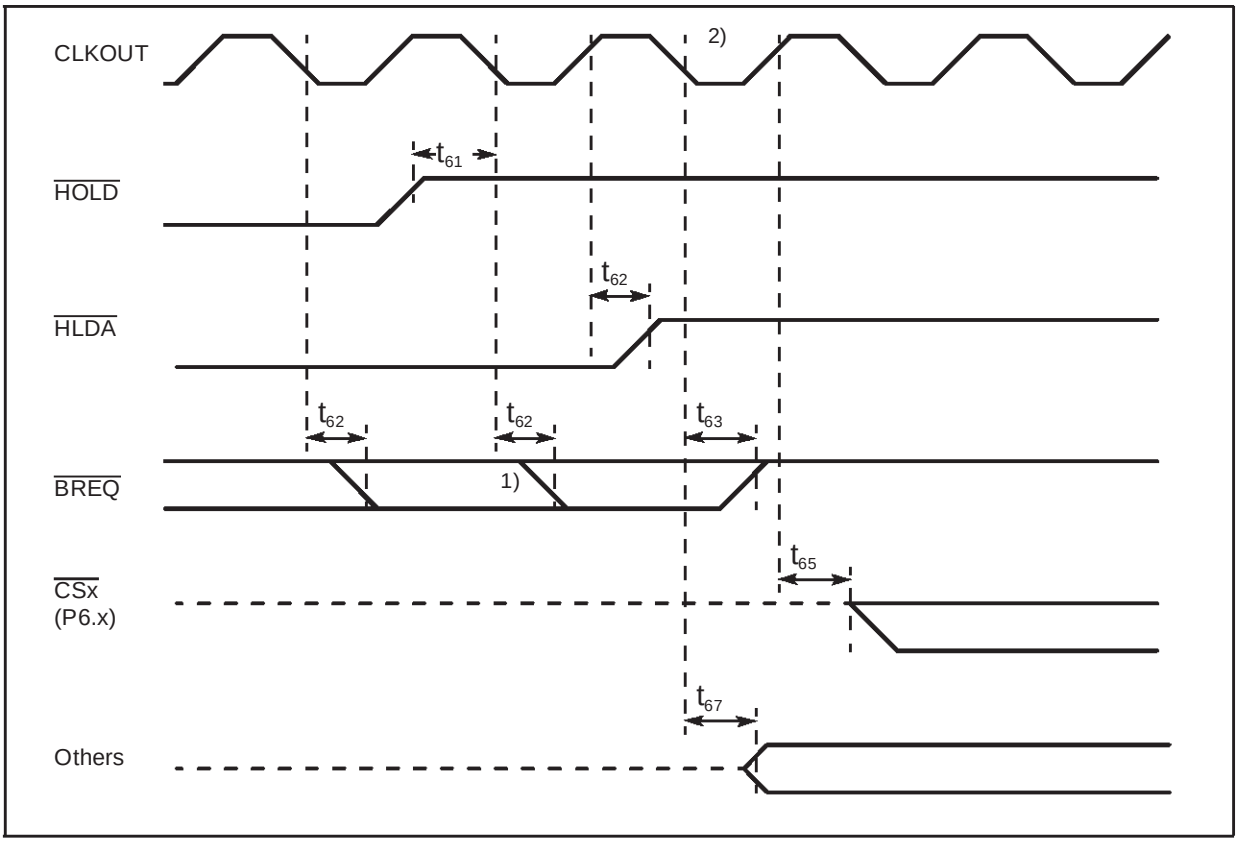


Notes: 1. The ST10F168 will complete the currently running bus cycle before granting bus access.

2. This is the first possibility for $\overline{BREQ}$ to become active.

3. The $\overline{CS}$ outputs will be resistive high (pullup) after t_{64}.

Figure 31 : External bus arbitration, (regaining the bus)

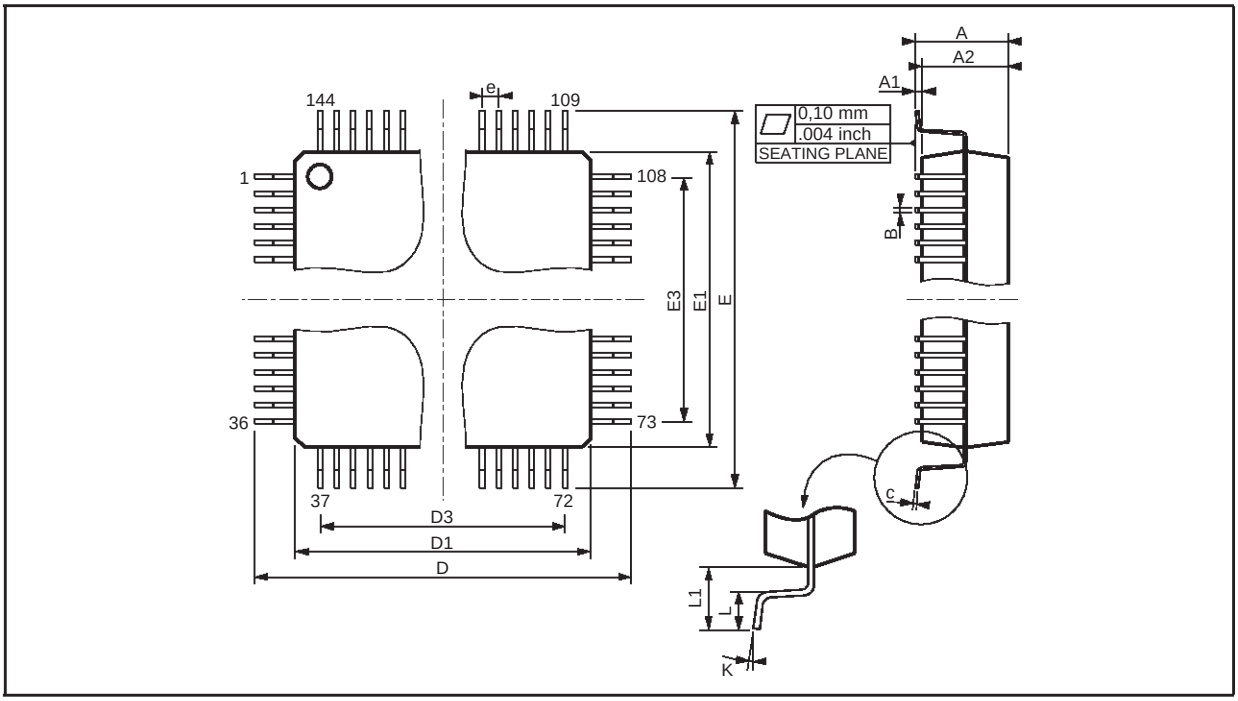


Notes: 1. This is the last opportunity for BREQ to trigger the indicated regain-sequence.
Even if BREQ is activated earlier, the regain-sequence is initiated by HOLD going high.
Please note that HOLD may also be deactivated without the ST10F168 requesting the bus.

2. The next ST10F168 driven bus cycle may start here.

21 - PACKAGE MECHANICAL DATA

Figure 32 : Package Outline PQFP144 (28 x 28mm)



Dimensions	Millimeters [1]			Inches (approx)		
	Minimum	Typical	Maximum	Minimum	Typical	Maximum
A			4.07			0.160
A1	0.25			0.010		
A2	3.17	3.42	3.67	0.125	0.133	0.144
B	0.22		0.38	0.009		0.015
c	0.13		0.23	0.005		0.009
D	30.95	31.20	31.45	1.219	1.228	1.238
D1	27.90	28.00	28.10	1.098	1.102	1.106
D3		22.75			0.896	
e		0.65			0.026	
E	30.95	31.20	31.45	1.219	1.228	1.238
E1	27.90	28.00	28.10	1.098	1.102	1.106
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0° (Min.), 7° (Max.)					

Note: 1. Package dimensions are in mm. The dimensions quoted in inches are rounded.

22 - ORDERING INFORMATION

Sales type	Temperature range	Package
ST10F168-Q6	-40°C to 85°C	PQFP144 (28 x 28mm)
ST10F168-Q3	-40°C to 125°C	PQFP144 (28 x 28mm)

F168Q3Q6.REF