

NP82N10PUF

MOS FIELD EFFECT TRANSISTOR

R07DS0444EJ0100 Rev.1.00 Aug 26, 2011

Description

The NP82N10PUF is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Super low on-state resistance
 - --- $R_{DS(on)}$ = 15 mΩ MAX. (V_{GS} = 10 V, I_D = 41 A)
- Low C_{iss} : $C_{iss} = 2900 \text{ pF TYP}$. $(V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V})$
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	Lead Plating	Pack	Package	
NP82N10PUF-E1-AY *1	Pure Sn (Tin)	Tape 800 p/reel	Taping (E1 type)	TO-263 (MP-25ZP)
NP82N10PUF-E2-AY *1			Taping (E2 type)	

Note: *1. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings ($T_A = 25^{\circ}C$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	100	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	±82	A
Drain Current (pulse) *1	I _{D(pulse)}	±164	A
Total Power Dissipation (T _C = 25°C)	P _{T1}	150	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.8	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	-55 to +175	°C
Single Avalanche Current *2	I _{AS}	34	А
Single Avalanche Energy *2	E _{AS}	117	mJ

Thermal Resistance

Notes: *1. T_C = 25°C, PW \leq 10 μ s, Duty Cycle \leq 1%

*2. $T_{ch(start)}$ = 25°C, V_{DD} = 50 V, R_{G} = 25 Ω , L = 100 μ H, V_{GS} = 20 V \rightarrow 0 V

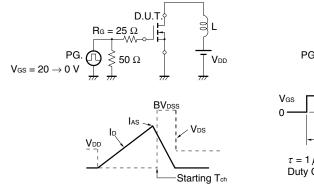
Electrical Characteristics ($T_A = 25^{\circ}C$)

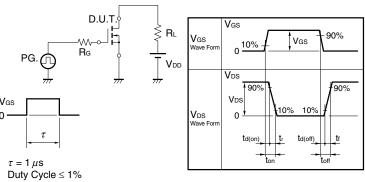
Item	Symbol	MAX.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			1	μΑ	V _{DS} = 100 V, V _{GS} = 0 V
Gate Leakage Current	I _{GSS}			±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	1.7	2.5	3.3	V	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$
Forward Transfer Admittance *1	y _{fs}	30	60		S	$V_{DS} = 5.0 \text{ V}, I_{D} = 41 \text{ A}$
Drain to Source On-state	R _{DS(on)1}		12	15	mΩ	V _{GS} = 10 V, I _D = 41 A
Resistance *1	R _{DS(on)2}		13	22	mΩ	$V_{GS} = 5.8 \text{ V}, I_D = 18 \text{ A}$
Input Capacitance	C _{iss}		2900	4350	pF	V _{DS} = 25 V,
Output Capacitance	Coss		340	510	pF	$V_{GS} = 0 V$,
Reverse Transfer Capacitance	C _{rss}		140	250	pF	f = 1 MHz
Turn-on Delay Time	t _{d(on)}		16	35	ns	V _{DD} = 50 V, ID = 41 A,
Rise Time	t _r		16	40	ns	V _{GS} = 10 V
Turn-off Delay Time	$t_{d(off)}$		60	120	ns	$R_G = 0 \Omega$
Fall Time	t _f		8	20	ns	
Total Gate Charge	Q_{G}		64	96	nC	V _{DD} = 80 V,
Gate to Source Charge	Q_{GS}		12		nC	$V_{GS} = 10 \text{ V},$
Gate to Drain Charge	Q_{GD}		22		nC	I _D = 82 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.95	1.5	V	I _F = 82 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		62		ns	I _F = 82 A, V _{GS} = 0 V,
Reverse Recovery Charge	Q _{rr}		135		nC	di/dt = 100 A/μs

Note: *1. Pulsed test

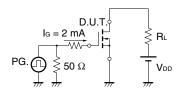
TEST CIRCUIT 1 AVALANCHE CAPABILITY

TEST CIRCUIT 2 SWITCHING TIME



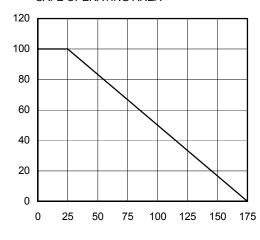


TEST CIRCUIT 3 GATE CHARGE



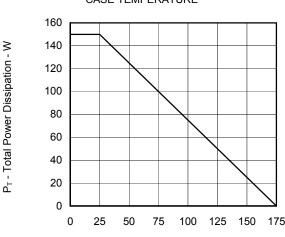
Typical Characteristics ($T_A = 25^{\circ}C$)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



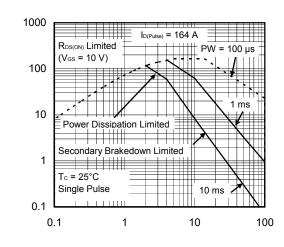
T_C - Case Temperature - °C

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



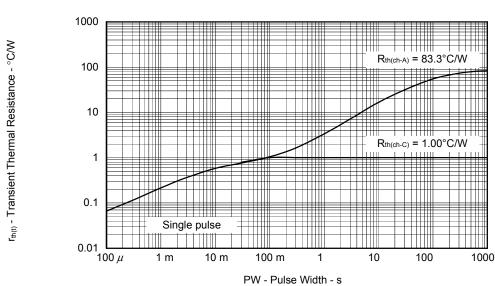
 T_{C} - Case Temperature - $^{\circ}\text{C}$

FORWARD BIAS SAFE OPERATING AREA



V_{DS} - Drain to Source Voltage - V

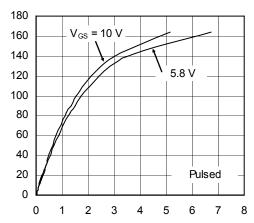
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



dT - Percentage of Rated Power - %

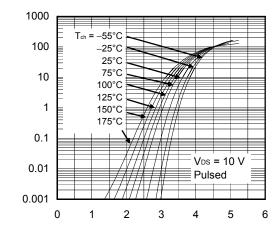
I_D - Drain Current - A

DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



V_{DS} - Drain to Source Voltage - V

FORWARD TRANSFER CHARACTERISTICS

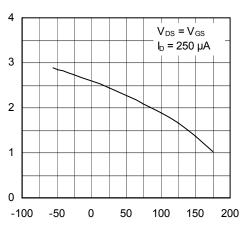


Ip - Drain Current - A

y_{fs} | - Forward Transfer Admittance - S

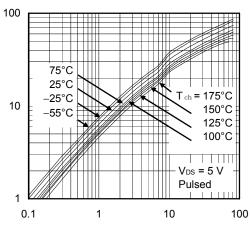
 V_{GS} - Gate to Source Voltage - V

GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



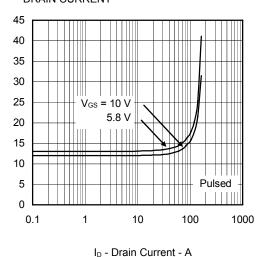
T_{ch} - Channel Temperature - °C

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

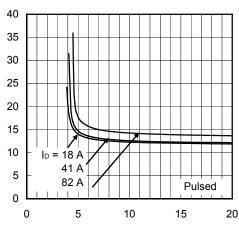


I_D - Drain Current - A

DRAIN TO SOURCE ON-STATE RESISTANCE vs. **DRAIN CURRENT**



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



V_{GS} - Gate to Source Voltage - V

 $R_{DS(on)}$ - Drain to Source On-state Resistance - $m\Omega$

 $R_{\text{DS(on)}}$ - Drain to Source On-state Resistance - $m\Omega$

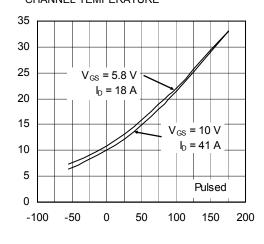
V_{GS(th)} - Gate to Source Threshold Voltage - V

 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$ - Drain to Source On-state Resistance - $m\Omega$

t_{d(on)}, t, t_{d(off)}, t_f - Switching Time - ns

IF - Diode Forward Current - A

DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



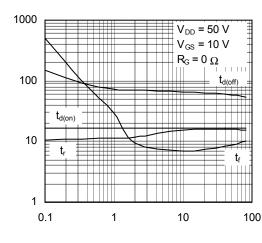
T_{ch} - Channel Temperature - $^{\circ}C$

10000 C_{iss} Ciss, Coss, Crss - Capacitance - pF 1000 Coss 100 Crss 10 $V_{GS} = 0 V$ f = 1 MHz 1 1 1 1 1 1 1 1 1 0.01 0.1 1 10 100

V_{DS} - Drain to Source Voltage - V

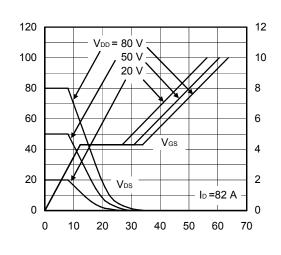
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

SWITCHING CHARACTERISTICS



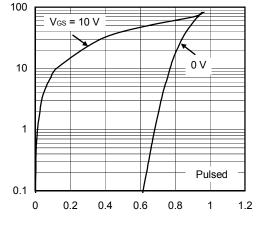
I_D - Drain Current - A

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



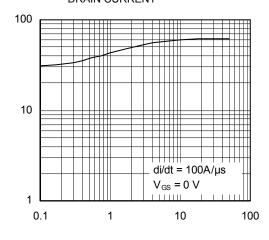
Q_G - Gate Charge - nC

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



 $V_{\text{F(S-D)}}$ - Source to Drain Voltage - V

REVERSE RECOVERY TIME vs. DRAIN CURRENT



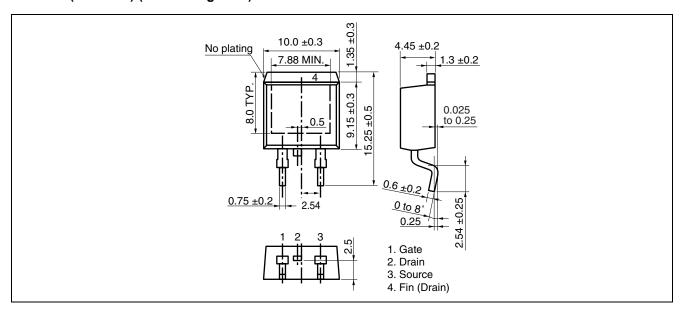
I_F - Drain Current - A

t_{rr} - Reverse Recovery Time - ns

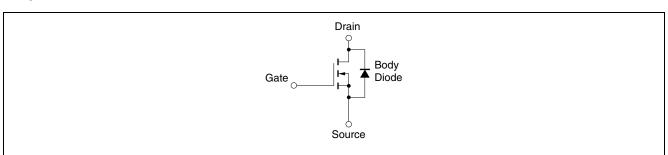
V_{DS} - Drain to Source Voltage - V

Package Drawings (Unit: mm)

TO-263 (MP-25ZP) (Mass: 1.5 g TYP.)



Equivalent Circuit



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History

NP82N10PUF Data Sheet

		Description		
Rev.	Date	Page	Summary	
1.00	Aug 26, 2011	_	First Edition Issued	

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