Development Board EPC9065
Quick Start Guide

EPC2007C, EPC2038

6.78 MHz, High Power ZVS Class-D Development Board

Revision 2.0

EPC

EFFICIENT POWER CONVERSION

DESCRIPTION

The EPC9065 is a high efficiency, Zero Voltage Switching (ZVS) differential mode Class-D amplifier development board that operates at, but is not limited to, 6.78 MHz (Lowest ISM band). The purpose of this development board is to simplify the evaluation process of a high power ZVS Class-D amplifier for use in applications such as A4WP wireless power using eGaN® FETs by including all the critical components on a single board that can be easily connected into an existing system. To support the increased power capability, two mounted heat sinks are included.

The amplifier board features the EPC2007C and the EPC2038, which are 100 V rated enhancement-mode gallium nitride FETs (eGaN® FET). The EPC2007C is used in the Class-D amplifier while the EPC2038 is used as a synchronous bootstrap FET. The amplifier can be set to operate in either differential mode or single ended mode and includes the gate drivers and 6.78 MHz oscillator.

For more information on the EPC2007C or EPC2038 eGaN FETs please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

Table 1: Performance Summary (T$_A$ = 25°C) EPC9065

Symbol	Parameter	Conditions	Min	Max	Units
V$_{DD}$	Logic Input Voltage Range		7.5	12	V
V$_{AMP}$	Amp Input Voltage Range		0	80	V
V$_{OUTA}$	Switch Node Output Voltage			80	V
V$_{OUTB}$	Switch Node Output Voltage			80	V
I$_{OUT}$	Switch Node Output Current (each)			1.8*	A$_{RMS}$
V$_{extosc}$	External Oscillator Input Threshold	Input 'Low' Input 'High'	-0.3 3.5	0.8 5	V V
V$_{Osc\_Disable}$	Oscillator Disable Voltage Range	Open drain/ collector	-0.3	5	V
I$_{Osc\_Disable}$	Oscillator Disable Current	Open drain/ collector	-25	25	mA

Maximum current depends on die temperature – actual maximum current will be subject to switching frequency, bus voltage and thermals.

DETAILED DESCRIPTION

The EPC9065 consists of a differential mode ZVS Class-D amplifier, a 6.78 MHz oscillator, and a separate heat sink for each Class-D section. The power schematic of the EPC9065 is shown in figure 1.

For operating frequencies other than 6.78 MHz, the oscillator can be disabled by placing a jumper into J60 or can be externally shutdown using an externally controlled open collector / drain transistor on the terminals of J60 (note which is the ground connection). The oscillator disable switch needs to be capable of sinking at least 25 mA. The external oscillator can then be connected to J71.

ZVS Timing Adjustment

Setting the correct time to establish ZVS transitions is critical to achieving high efficiency with the EPC9065 amplifier. This can be done by selecting the values for R71, R72, R73, and R74 respectively. This procedure is best performed using a potentiometer installed at the appropriate locations (P71, P72, P73, and P74) that is used to determine the fixed resistor values. The timing MUST initially be set without a load connected to the amplifier. The timing diagrams are given in figure 4 and should be referenced when following this procedure. Only perform these steps if changes have been made to the board as it is shipped preset. The steps are:

1. With power off, connect the logic input supply (7.5 - 12 V) to V$_{DD}$ connector (J90). Note the polarity of the supply connector.

2. Connect a LOW capacitance oscilloscope probe to the probe-hole of the half-bridge to be set and lean it against the ground post as shown in figure 3.

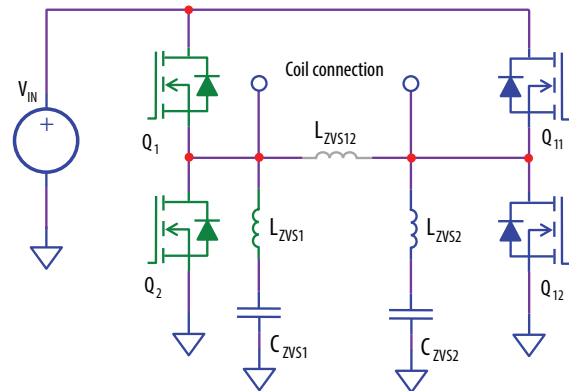3. Turn on the logic supply – make sure the supply is set to approximately 7.5 - 12 V.

Figure 1: Power schematic of the EPC9065 differential mode ZVS amplifier

4. Turn on the main supply voltage to 5 V to ensure that the switch node waveform looks similar to figure 4. If not, adjust the potentiometers. After verification, the main supply voltage can be set to the required predominant operating value (such as 24 V but NEVER exceed the absolute maximum voltage of 80 V).

5. While observing the oscilloscope, adjust the applicable potentiometers to achieve the green waveform of figure 4.

6. Repeat for the other half-bridge.

7. Replace the potentiometers with fixed value resistors if required.

Determining component values for L$_{ZVS}$

The ZVS tank circuit is not operated at resonance, and only provides the necessary negative device current for self-commutation of the output voltage at turn off. The capacitors C$_{ZVS1}$ and C$_{ZVS2}$ are chosen to have a very small ripple voltage component and are typically around 1 µF. The amplifier supply voltage, switch-node transition time will determine the value of inductance for L$_{ZVSx}$ which needs to be sufficient to maintain ZVS operation over the DC device load resistance range and coupling between the device and source coil range and can be calculated using the following equation:

$$L_{ZVS} = \frac{\Delta t_{vt}}{8 \cdot f_{sw} \cdot (2 \cdot C_{OSSQ} + C_{well})} \qquad (1)$$

Where:

Δt_{vt} = Voltage Transition Time [s]

f_{sw} = Operating Frequency [Hz]

C_{OSSQ} = Charge Equivalent Device Output Capacitance [F]

C_{well} = Gate Driver Well Capacitance [F]. For the LM5113, use 20 pF.

NOTE. The amplifier supply voltage V$_{AMP}$ is absent from the equation as it is accounted for by the voltage transition time. The per device charge equivalent capacitance can be determined using the following equation:

$$C_{OSSQ} = \frac{1}{V_{AMP}} \cdot \int_0^{V_{AMP}} C_{OSS\,(v)} \cdot dv \qquad (2)$$

To add additional immunity margin for shifts in load impedance, the value of L$_{ZVS}$ can be decreased to increase the current at turn off of the devices (which will increase device losses). Typical voltage transition times range from 2 ns through 12 ns. For the differential case the voltage and charge (C$_{OSSQ}$) are doubled when calculating the ZVS inductance.

QUICK START PROCEDURE

The EPC9065 amplifier board is easy to set up and evaluate the performance of the eGaN FET in a wireless power transfer application.

Please note that main power is connected directly to the amplifier. Hence, there is no thermal or over-current protection to ensure the correct operating conditions for the eGaN FETs. If the main power is sourced from a benchtop DC power supply, it is highly advised to set a reasonable current limit of 500 – 800 mA during initial evaluation.

1. Make sure the entire system, including the heat sink assembly, is fully assembled prior to making electrical connections. This includes any load to be connected.

2. With power off, connect the main input power supply bus to the bottom pin of J50 and the ground to the ground connection of J50 as shown in figure 2.

3. With power off, connect the logic input power supply bus to +V$_{DD}$ (J90). Note the polarity of the supply connector. This is used to power the gate drivers and logic circuits.

4. Make sure all instrumentation is connected to the system.

5. Turn on the logic supply – make sure the supply is between 7.5 - 12 V.

6. Turn on the main supply voltage, starting at 0 V and increasing slowly to the required value (it is recommended to start at 5 V for dead time tuning purposes and do not exceed the absolute maximum voltage of 80 V).

7. Once operation has been confirmed, adjust the main supply voltage within the operating range and observe the output voltage, efficiency and other parameters on both the amplifier and device boards.

8. For shutdown, please follow steps in the reverse order. Start by reducing the main supply voltage to 0 V followed by steps 6 through 2.

NOTE. When measuring the high frequency content switch-node (Source Coil Voltage), care must be taken to avoid long ground leads. An oscilloscope probe connection (preferred method) has been built into the board to simplify the measurement of the Source Coil Voltage (shown in figure 3).

For more information on measurement techniques, please refer to Application Note AN023: *Accurately Measuring High Speed GaN Transistors*.
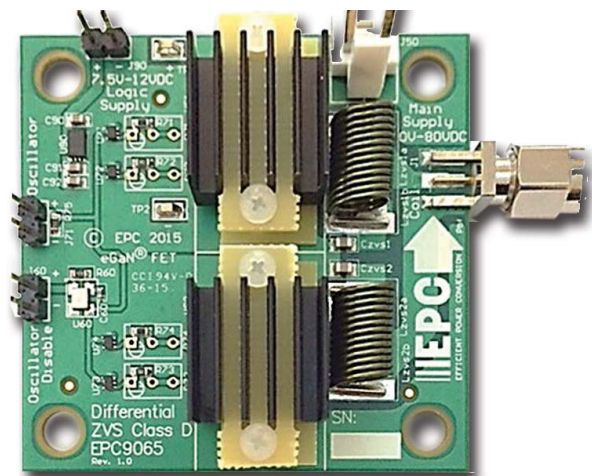
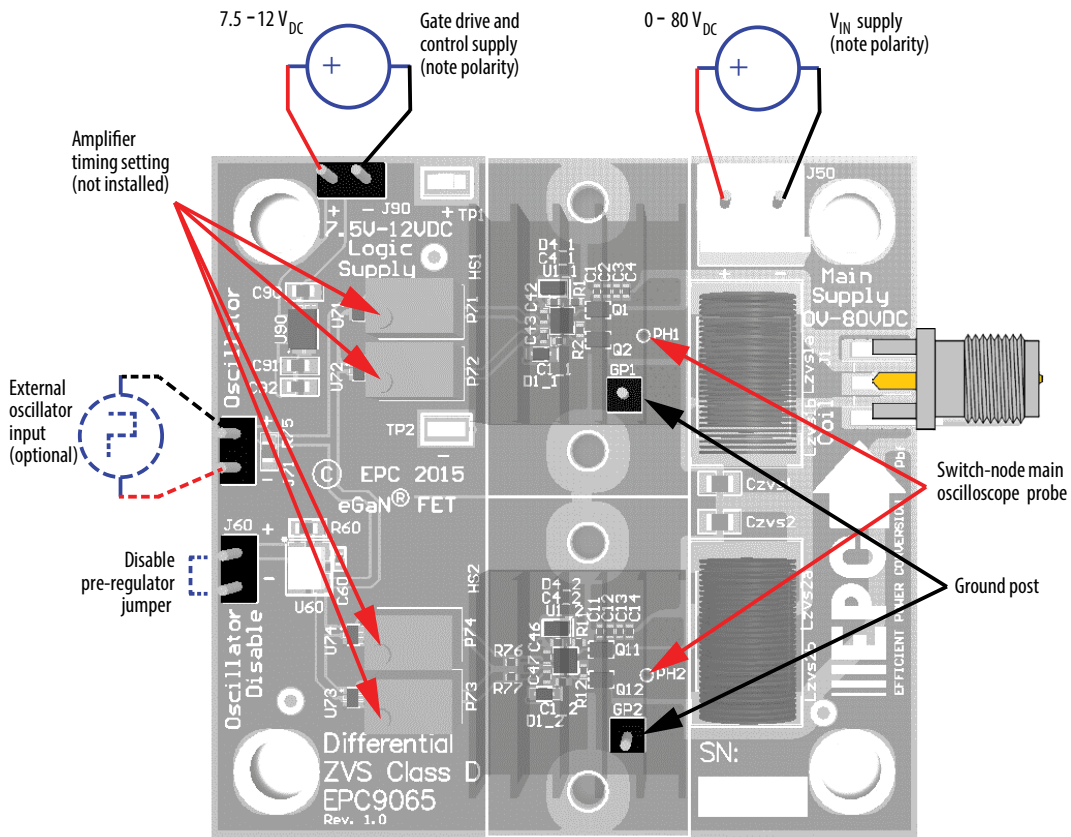EPC9065 amplifier board with heat sink photo

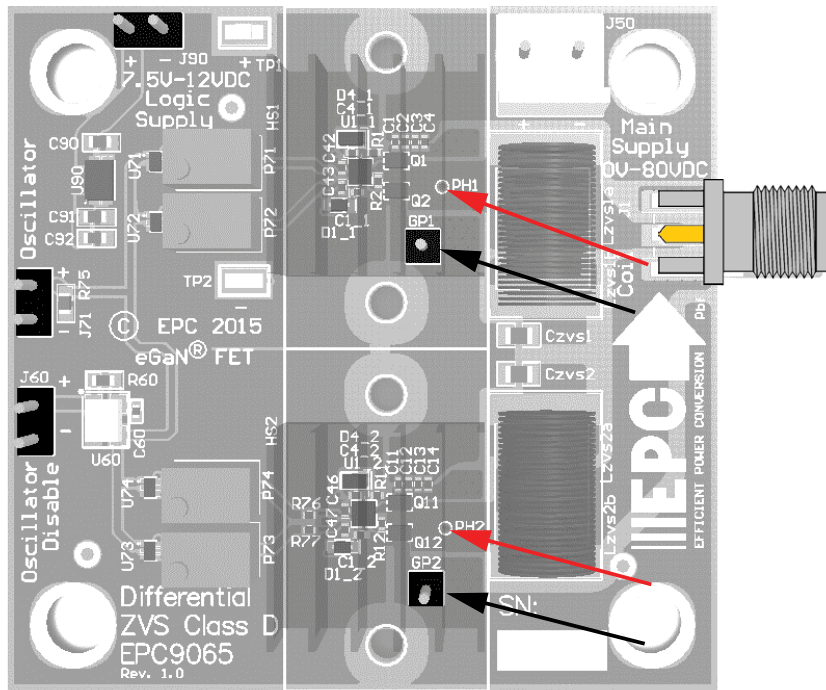Figure 2: Proper connection and measurement setup for the amplifier board

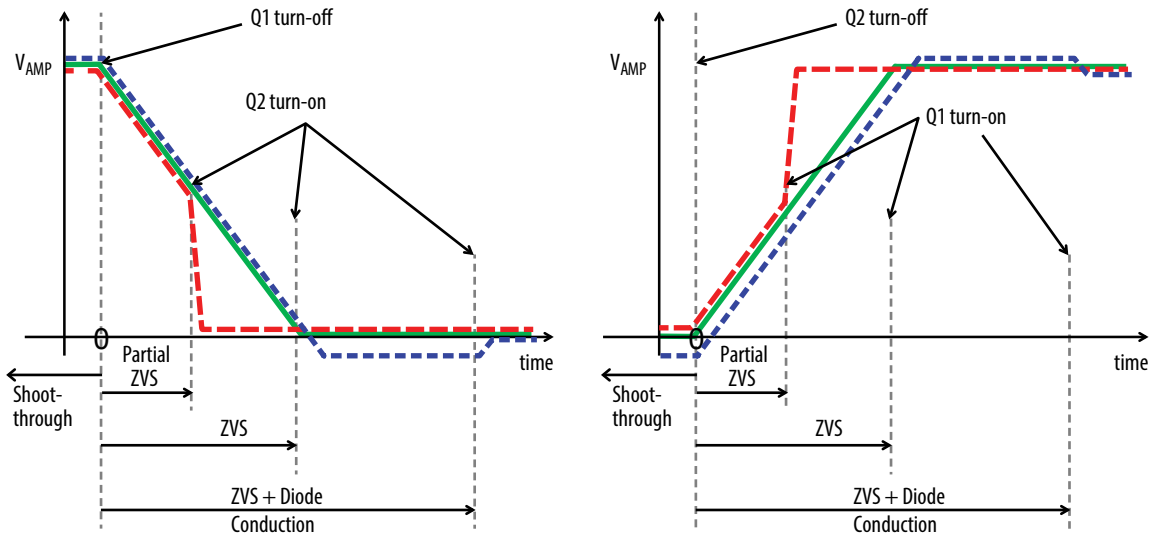Figure 3: Proper measurement of the switch nodes

Figure 4: ZVS timing diagrams

THERMAL CONSIDERATIONS

The EPC9065 development board showcases the EPC2007C and EPC2038 eGaN FETs in a ZVS Class-D amplifier application. Although the electrical performance surpasses that of traditional silicon devices, their relatively smaller size does magnify the thermal management requirements. The operator must observe the temperature of the gate driver and eGaN FETs to ensure that both are operating within the thermal limits as per the datasheets.

A heat sink kit is mounted on each half bridge of the EPC9065 board. Figure 5 shows the assembly order for the heat sink kit.

NOTE. The EPC9065 development board has no current protection on board and care must be exercised not to over-current or over-temperature the devices. Excessively wide coil coupling and load range variations can lead to increased losses in the devices.

Precautions

The EPC9065 development board has no controller or enhanced protection systems and therefore should be operated with caution. Some specific precautions are:

1. It is highly advised to set a reasonable current limit of 500 - 800 mA during initial evaluation.

2. Ensure that the gap pad included in the heat sink assembly is firmly compressed on the eGaN FETs prior to full power operation. Be careful not to damage the die by over-tightening of the bolts.

3. Please contact EPC at info@epc-co.com should there be questions regarding specific load range impedance requirements.
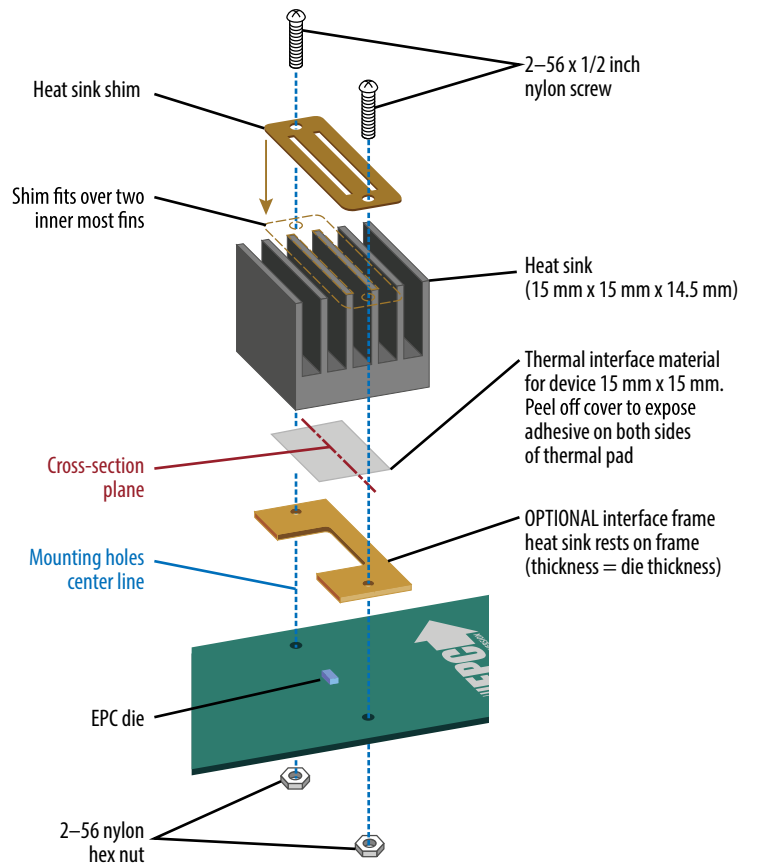

Figure 5: Heat sink kit assembly

Table 2: Bill of Materials - Amplifier Board

Item	Qty	Reference	Part Description	Manufacturer	Part Number
1	8	C1, C2, C3, C4, C11, C12, C13, C14	10 nF, 100 V	TDK	C1005X7S2A103K050BB
2	2	C1_1, C1_2	4.7 µF, 10 V	Samsung	CL05A475MP5NRNC
3	11	C2_1, C2_2, C4_1, C4_2, C5_1, C5_2, C60, C71, C72, C73, C74	100 nF, 25 V	Murata	GRM155R71C104KA88D
4	2	C3_1, C3_2	22 nF, 25 V	TDK	C1005X7R1E223K050BB
5	4	C5, C6, C15, C16	2.2 µF 100 V	Taiyo Yuden	HMK325B7225KN-T
6	4	C42, C43, C46, C47	22 pF, 50 V	KemΩt	C0402C220J5GACTU
7	3	C90, C91, C92	1 µF, 25 V	TDK	C1608X7R1E105K
8	2	Czvs1, Czvs2	1 µF 50 V	Taiyo Yuden	C2012X7R1H105K125AB
9	2	D1_1, D1_2	40 V 300 mA	ST	BAT54KFILM
10	8	D2_1, D2_2, D3_1, D3_2, D71, D72, D73, D74	40 V 30 mA	Diodes Inc.	SDM03U40
11	2	D4_1, D4_2	5 V1, 150 mΩ	Bournes	CD0603-Z5V1
12	1	J1	SMA Board Edge	Linx	CONREVSMA013.062
13	1	J50	.156" Male Vert.	Würth	645002114822
14	3	J60, J71, J90	.1" Male Vert.	Würth	61300211121
15	2	Lzvs1b, Lzvs2b	390 nH	CoilCraft	2929SQ-391JEB
16	4	Q1, Q2, Q11, Q12	100 V 6A 30 mΩ	EPC	EPC2007C
17	2	Q4_1, Q4_2	100 V 2800 mΩ	EPC	EPC2038
18	4	R1, R2, R11, R12	2.2 Ω	Yageo	RC0402JR-072R2L
19	2	R2_1, R2_2	20 Ω	Stackpole	RMCF0402JT20R0
20	2	R3_1, R3_2	2.7 k	Panasonic	ERJ-2GEJ272X
21	2	R4_1, R4_2	4.7 Ω	Panasonic	ERJ-2GEJ4R7X
22	1	R60	47 k	Stackpole	RMCF0603JT47K0
23	2	R71, R74	470 Ω	Stackpole	RMCF0603FT470R
24	2	R72, R73	390 Ω	Stackpole	RMCF0603FT390R
25	1	R75	10 k	Yageo	RC0603JR-0710KL
26	2	R76, R77	0 Ω	Yageo	RC0402JR-070RL
27	2	TP1, TP2	SMD probe loop	Keystone	5015
28	2	U1_1, U1_2	100 V eGaN Driver	National Semiconductor	LM5113TM
29	1	U60	Pgm Osc.	EPSON	SG-8002CE
30	2	U71, U73	2 In AND	Fairchild	NC7SZ08L6X
31	2	U72, U74	2 In NAND	Fairchild	NC7SZ00L6X
32	1	U90	5.0 V 250 mA DFN	Microchip	MCP1703T-5002E/MC

EPC would like to acknowledge Coilcraft (www.coilcraft.com) and KDS Daishinku America (www.kdsamerica.com) for their support of this project.

Table 3: Optional Components

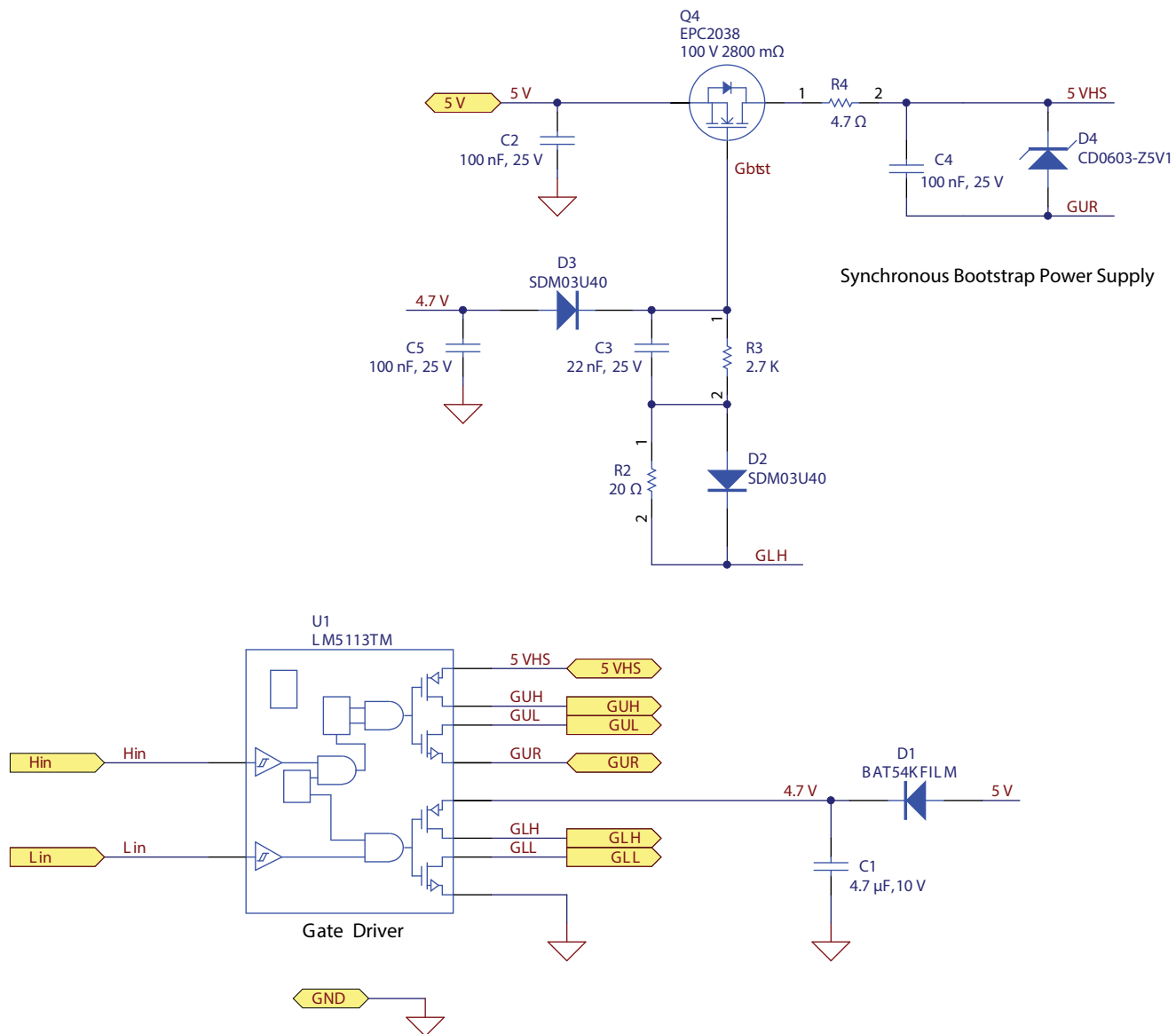| Item	Qty	Reference	Part Description	Footprint
1	2	Lzvs1a, Lzvs2a	Aircore inductor	CoilCraft 2222SQ
2	4	P71, P72, P73, P74	1 k Multi-turn potentiometer	PV37W
3	2	GP1, GP2	.1" Male Vertical Header	SIP1.1

Synchronous Bootstrap Power Supply

Figure 6: EPC9065 - Gate Driver Schematic

Oscillator Output

J71
1
2
Osc
.1" Male Vert.

5 V
U71
NC7SZ08L6X
A
B
Y
OSC
R71 470 Ω
Deadtime Right
P71 DNP 1K
H_Sig1
D71
40 V, 30 mA
SDM03U40

5 V
C71
100 nF, 25 V

5 V
U72
NC7SZ00L6X
A
B
OSC
R72 390 Ω
Deadtime Left
P72 DNP 1K
L_Sig1
D72
40 V, 30 mA
SDM03U40

5 V
C72
100 nF, 25 V

OSC
C75
DNP 100 pF, 25 V
R75 10 K

5 V
U73
NC7SZ08L6X
A
B
Y
OSC
R73 390 Ω
Deadtime Right
P73 DNP 1K
L_Sig2
D73
40 V, 30 mA
SDM03U40

5 V
C73
100 nF, 25 V

5 V
U74
NC7SZ00L6X
A
B
OSC
R74 470 Ω
Deadtime Left
P74 DNP 1K
H_Sig2
D74
40 V, 30 mA
SDM03U40

5 V
C74
100 nF, 25 V

Logic Supply
7.5 VDC - 12 VDC

J90
1
2
V7 in
.1" Male Vert.

U90
5.0 V 250 mA DFN
V_DD
IN
GND
OUT
5 V
C90
1 µF, 25 V
C91
1 µF, 25 V
C92
1 µF, 25 V

Logic Supply Regulator

J60
1
2
.1" Male Vert.

Oscillator Disable

5 V
R60 47 k
5 V
U60
Pgm Osc.
VCC
OE
GND
OUT
Osc
5 V
C60
100 nF, 25 V

Oscillator

C42
22 pF, 50 V
H_Sig1
Hin
C43
22 pF, 50 V
L_Sig1
Lin
5 VHS
GUH
GUL
GUR
5 V
GLH
GLL
GND
5 VHS1
GRH1
GRL 1
OutA
5 V
GLH1
GLL1
HighEffGateDrvr_r1_0.SchDoc
Gate Driver

H_Sig2
R76 0 Ω
C46
22 pF, 50 V
Hin
L_Sig2
R77 0 Ω
C47
22 pF, 50 V
Lin
5 VHS
GUH
GUL
GUR
5 V
GLH
GLL
GND
5 VHS2
GRH2
GRL2
OutB
5 V
GLH2
GLL2
HighEffGateDrvr_r1_0.SchDoc
Gate Driver

J50
.156" Male Vert.
1
2
Vamp
Main Supply
0 V ~ 80 V 4 A max

TP1
Vamp
SMD probe loop

GRH1 1
R1 2 Ω 2
GRL 1
Q1
EPC2007C
Vamp
Main Amplifier
OutA

GLH1 1
R2 2 Ω 2
GLL1
Q2
EPC2007C

TP2
SMD probe loop

GP1
EMPTY
.1" Male Vert.
Ground Post

GRH2 1
R11 2 Ω 2
GRL2
Q11
EPC2007C
Vamp
Secondary Amplifier
OutB

GLH21
R12 2 Ω 2
GLL2
Q12
EPC2007C

GP2
EMPTY
.1" Male Vert.
Ground Post

PH1 ProbeHole

Lzvs1b 390 nH
Lzvs1a DNP 270 nH
Czvs1 1 µF, 50 V

Czvs2 1 µF, 50 V

Lzvs2b 390 nH
Lzvs2a DNP 270 nH

PH2 ProbeHole

HS 1
HS- 15 mm x 15 mm WMount

HS 2
HS- 15 mm x 15 mm WMount

J1
SMA Board Edge
ZVS Tank Circuit

Vamp
C1 10 nF, 100 V
C2 10 nF, 100 V
C5 2.2 µF, 100 V
C3 10 nF, 100 V
C4 10 nF, 100 V
C6 2.2 µF, 100 V

C11 10 nF, 100 V
C12 10 nF, 100 V
C15 2.2 µF, 100 V
C13 10 nF, 100 V
C14 10nF, 100 V
C16 2.2 µF, 100 V
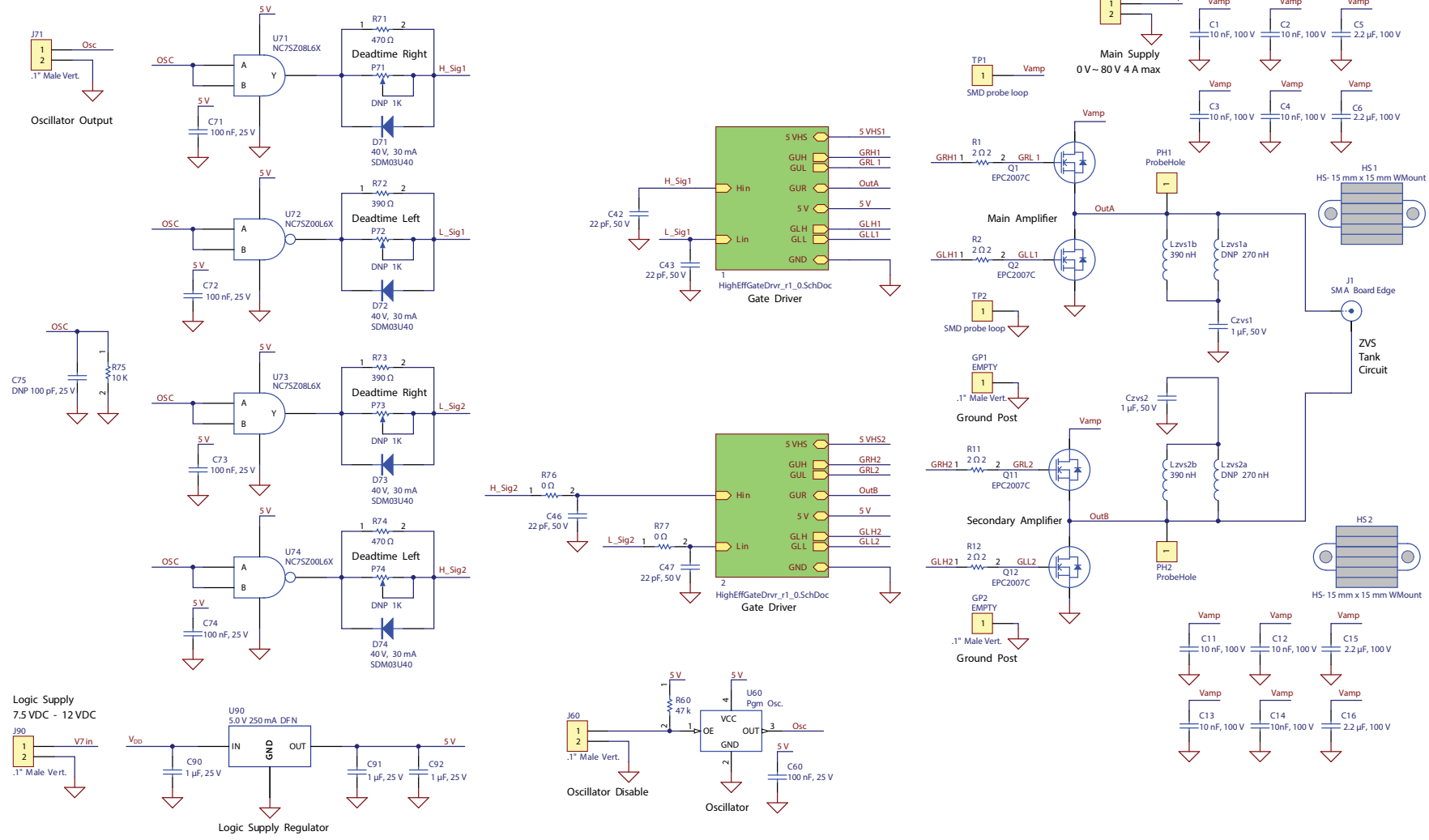
Figure 7: EPC9065 – ZVS Class D Schematic

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