ML630 Virtex-6 HXT FPGA Optical Transmission Network Evaluation Board

User Guide

UG828 (v1.0) September 28, 2011

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/28/11	1.0	Initial Xilinx release.

Table of Contents

About This Guide

This document describes the basic setup, features, and operation of the ML630 Virtex®-6 FPGA HXT Optical Transmission Network (OTN) evaluation board. The ML630 board provides the hardware environment for characterizing and evaluating the GTX and GTH transceivers available on the Virtex®-6 XC6VHX565T-2FFG1924C FPGA.

In this document Virtex-6 FPGA GTX transceiver is abbreviated as GTX transceiver. Similarly, Virtex-6 FPGA GTH transceiver is abbreviated as GTH transceiver.

Guide Contents

This user guide contains the following chapters and appendices:

- Chapter 1, ML630 Board Features and Operation, describes the components, features, and operation of the ML630 Virtex-6 HXT FPGA OTN evaluation board.
- Appendix A, Default Jumper Positions, lists the jumpers that must be installed on the board for proper operation.
- Appendix B, VITA 57.1 FMC HPC Connector Pinout, provides a pinout reference for the FPGA mezzanine card (FMC) connectors.
- Appendix C, ML630 Master UCF Listing for U1, provides a listing of the ML630 FPGA U1 user constraints file (UCF).
- Appendix D, ML630 Master UCF Listing for U2, provides a listing of the ML630 FPGA U2 user constraints file (UCF).
- Appendix E, ML630C Schematic Page List, provides a listing of schematic page numbers versus the detailed description callout numbers, for easy cross-referencing.
- Appendix F, Documents and Resources, lists documents relevant to Virtex®-6 devices, the ML630 Virtex-6 FPGA GTX Transceiver Characterization Board, and intellectual property.

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/support/documentation/index.htm.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	**`ngdbuild`** *design_name*
	References to other manuals	See the *Command Line Tools User Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

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Chapter 1

ML630 Board Features and Operation

This chapter describes the components, features, and operation of the ML630 Virtex®-6 HXT FPGA Optical Transmission Network (OTN) evaluation board. The ML630 board provides the hardware environment for characterizing and evaluating the GTX and GTH transceivers available on the Virtex -6 XC6VHX565T-2FFG1924C FPGA.

ML630 Board Features

- Two Virtex-6 XC6VHX565T-2FFG1924C FPGAs
- On-board power regulators for all necessary voltages with power status LEDs
- All ML630 FPGA U1 and U2 I/O banks V_{CCO} voltage is 2.5V
- Two types of external power supply jacks (12V "brick" DIN4 type, PC ATX type)
- USB JTAG configuration port for use with USB A-to-Mini-B cable
- System ACE™ controller with companion CompactFlash socket
- General purpose pushbutton and DIP switches, LEDs, and test I/O header for each FPGA
- VGA 2X5 male debug header for each FPGA
- USB-to-UART bridge with USB Mini-B pcb connector for each FPGA
- Two VITA 57.1 FMC HPC connectors
- I^2C bus hosting EEPROM, clock sources and FMC connectors
- A separate SiTime fixed 200 MHz 2.5V LVDS oscillator wired to each FPGAs global clock inputs
- Eight pairs of differential clock input SMA connectors
- Six I^2C programmable Silicon Labs Si570 3.3V LVPECL 10 MHz to 810 MHz oscillators
- Two differential input 8X8 crosspoint switches providing 16 selectable differential clock sources
- Four sets of plug and receptacle FCI Airmax 120 pin connectors implementing the Interlaken interconnect protocol

The ML630 board block diagram is shown in Figure 1-1.

Caution! The ML630 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

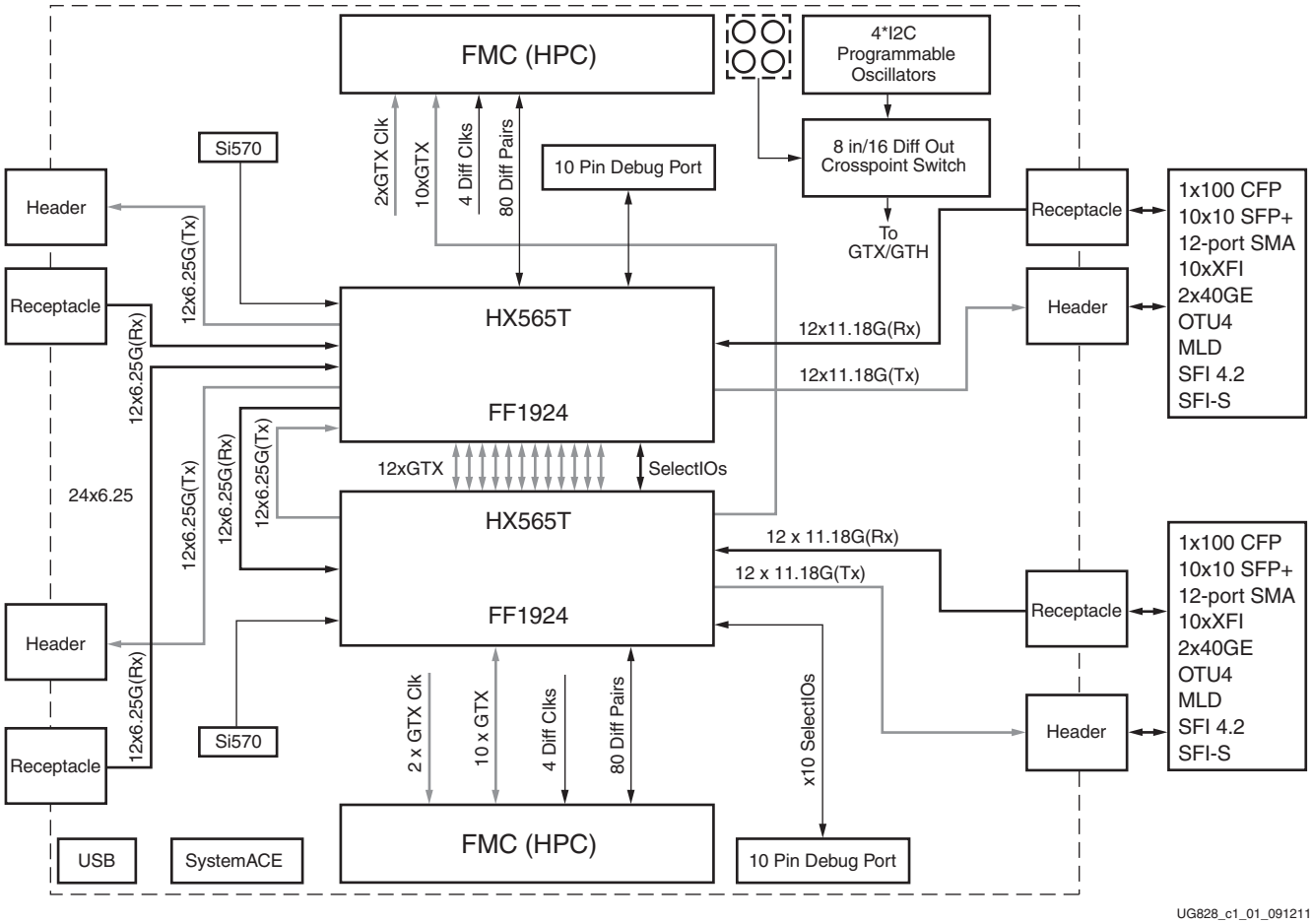

Figure 1-1: **ML630 Board Block Diagram**

Detailed Description

Note: This section of the user guide is intended to be read in conjunction with reference to the ML630 (pdf) Schematic 0381388. The ML630 board hosts a complicated clocking system and intricate FPGA-to-FPGA and Interlaken connector connectivity which the schematic helps clarify. Please refer to the schematic pages associated with the circuitry described in each section of this detailed description.

Figure 1-2 shows the ML630 board described in this user guide. Each numbered feature that is referenced in Figure 1-2 is described in the sections that follow.

Note: The image in Figure 1-2 is for reference only and might not reflect the current revision of the board.

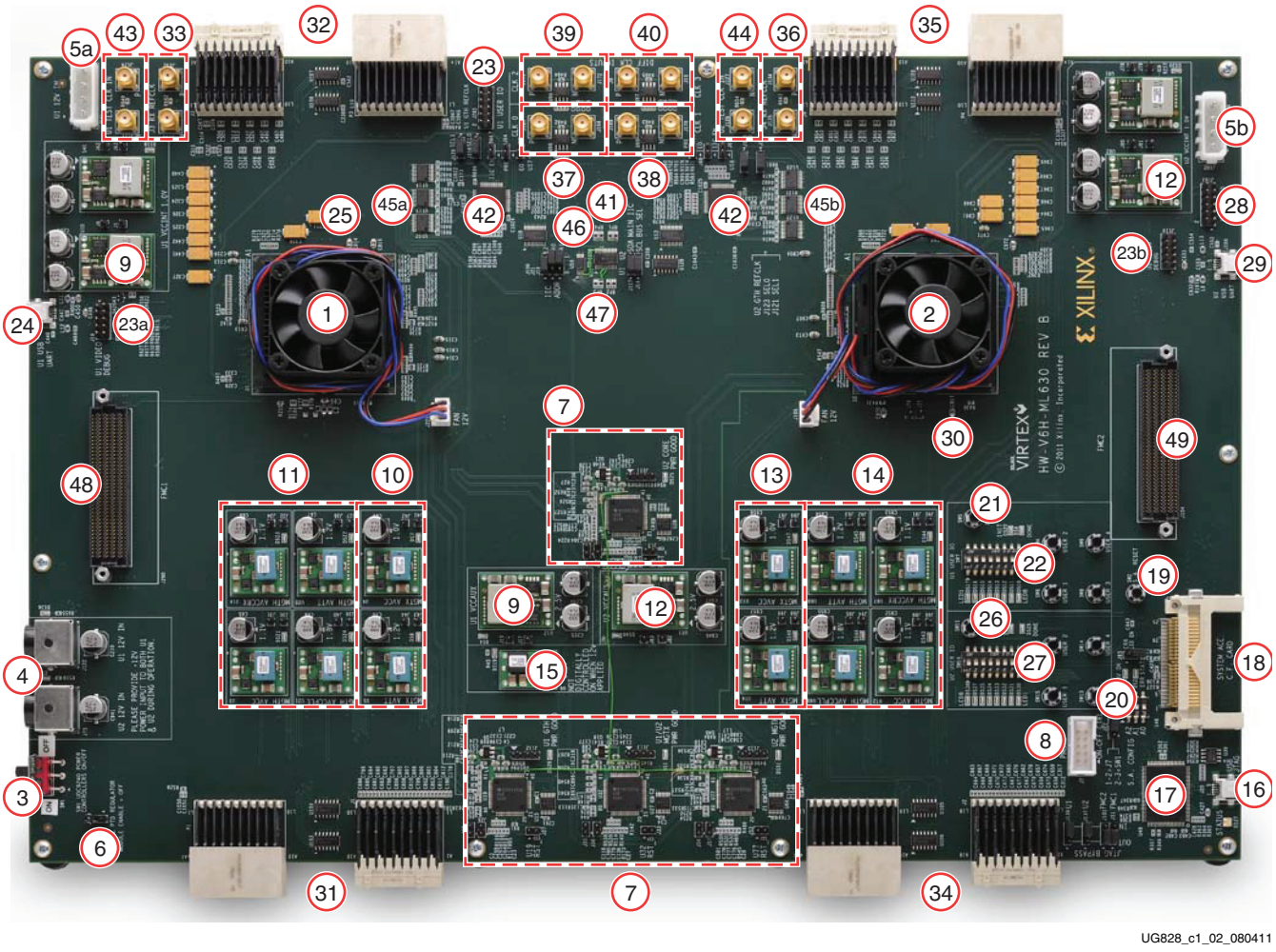

Figure 1-2: **Detailed Description of ML630 Board Components**

Virtex-6 HXT XC6VHX565T-2FFG1924 FPGA U1 and U2

1. FPGA U1
2. FPGA U2

ML630 12 VDC Power Input

3. Main power on-off "soft" slide switch (SW1)
4. U1/U2 12V DIN4 connectors (J122 and J75)
5. U1/U2 12V ATX connector (J141 and J102)

FPGA Power Inhibit Jumper

6. J289 regulator inhibit jumper

FPGA U1 and U2 Power System Controllers

7. U1 and U2 TI UCD9240 digital power controllers (U8, U19, U32 and U77)
8. PMBus connector (J7) for TI GPIO adapter (PMBus pod)

FPGA U1 Power Regulators

9. U1 V_{CCINT} (U10/U41) and V_{CCAUX} (U12) TI PTD08A020W regulators
10. U1 GTX (U4, U5) TI PTD08A101W regulators
11. U1 GTH (U3, U14, U21, U20) TI PTD08A010W and PTD08A006W regulators

FPGA U2 Power Regulators

12. U2 V_{CCINT} (U81/U82) and V_{CCAUX} (U83) TI PTD08A020W regulators
13. U2 GTX (U73, U74) TI PTD08A101W regulators
14. U2 GTH (U72, U67, U68, U69) TI PTD08A010W and PTD08A006W regulators

Board-wide 3.3V Regulator

15. TI PTH12000W 3.3V regulator (U6)

ML630 FPGA Configuration

16. USB JTAG Mini-B connector (J20)
17. Embedded JTAG (U48 top of board) and (U45 bottom of board) circuits
18. SystemACE CompactFlash (C.F.) Socket (U46 top of board), SystemACE IC (U47 bottom of board)
19. SystemACE reset pushbutton (SW2)
20. SystemACE C.F. image select DIP switch (SW3)

FPGA U1 Indicators and I/O

21. U1 PROG pushbutton (SW5), INIT LED (DS20) and DONE LED (DS6)
22. U1 User LEDs (DS10-DS17), User DIP switch (SW7) and user pushbutton switches (SW4, SW6, SW8, SW9)
23. 23a: U1 User GPIO 2X6 header (J285)
    23b: VGA video debug 2x5 header (J16)
24. U1 USB UART Mini-B connector (J54 top of board) and USB-to-UART bridge IC (U26 bottom of board)
25. U1 SiTime 200 MHz 2.5V LVDS fixed frequency oscillator (U22 bottom of board)

FPGA U2 Indicators and I/O

26. U2 PROG pushbutton (SW11), INIT LED (DS54) and DONE LED (DS29)
27. U2 User LEDs (DS30-DS38), User DIP switch (SW16) and user pushbutton switches (SW12-SW15)
28. U2 User GPIO 2X6 header (J103)
29. U2 USB UART Mini-B connector (J106) top of board) and USB-to-UART bridge IC (U26 bottom of board)
30. U2 SiTime 200 MHz 2.5V LVDS fixed frequency oscillator (U63 bottom of board)

FPGA U1 FCI Airmax Interlaken Connectors

31. P1, J1 FCI Airmax Interlaken plug and receptacle connectors

32. P3, J3 FCI Airmax Interlaken plug and receptacle connectors
33. J3 refclk (J132, J133) SMA connectors
34. P2, J2 FCI Airmax Interlaken plug and receptacle connectors

FPGA U2 FCI Airmax Interlaken Connectors

35. P4, J4 FCI Airmax Interlaken plug and receptacle connectors
36. J4 refclk (J134, J135) SMA connectors

FPGA U1 and FPGA U2 Clock Circuits

37. Differential clock input connectors CLK0 SMA (J167, J168) with 1-to-2 3.3V LVPECL buffer (U98)
38. Differential clock input connectors CLK1 SMA (J169,J170) with 1-to-2 3.3V LVPECL buffer (U99)
39. Differential clock input connectors CLK2 SMA (J171, J172) with 1-to-2 3.3V LVPECL buffer (U96)
40. Differential clock input connectors CLK3 SMA (J9, J10) with 1-to-2 3.3V LVPECL buffer (U97)
41. Four I^2C programmable Silicon Labs Si570 3.3V LVPECL 10 MHz-to-810 MHz oscillators (U43, U44, U51, U52) each with a 1-to-2 3.3V LVPECL buffer (U53, U54, U55, U56, bottom of board)
42. Two differential clock input-output 8x8 crosspoint switches (U57, U58)
43. FPGA U1 differential test clock input SMA connectors (J124, J125) with 1-to-6 3.3V LVDS buffer (U126)
44. FPGA U2 differential test clock input SMA connectors (J126, J127) with 1-to-6 3.3V LVDS buffer (U127)
45. Six dual 2-to-1 3.3V LVDS input, 3.3V LVPECL output differential clock multiplexers (U102, U115, U116, U120, U121, U122)
46. Two I^2C programmable Silicon Labs Si570 3.3V LVPECL 10 MHz-to-810 MHz oscillators, one for FPGA U1 (U64) and one for FPGA U2 (U65) (bottom of board), each with a 1-to-6 3.3V LVDS buffer (U13, U18), top of board)

ML630 I^2C Bus

47. I^2C Main Bus: M24C02 256x8 EEPROM (U59), TI PCA9548 (U31) 1-to-8 port I^2C expander (six ports wired to the Si570 oscillators, two ports wired to the 8x8 crosspoint switches); U1 I^2C: HPC FMC1 J290; U2 I^2C: HPC FMC2 J104

ML630 HPC FMC Connectors

48. FMC1 connector (J290)
49. FMC2 connector (J104)

Default Jumper Positions

A list of shunts and their required positions for normal board operation is provided in Appendix A, Default Jumper Positions.

Monitoring Voltage and Current

Voltage and current monitoring and control are available for all power rails except the fixed 3.3V through Texas Instruments' Fusion Digital Power graphical user interface (GUI). All onboard TI power controllers are wired to the same PMBus. The PMBus connector, J7, is provided for use with the TI GPIO Interface Adapter (PMBus pod) and associated TI Fusion Digital Power GUI.

References

More information about the power system components used by the ML630 board is available from the Texas Instruments digital power website at:

http://www.ti.com/ww/en/analog/digital-power/index.html

FPGA U1 and U2

Figure 1-2 callouts [1, 2]

The ML630 board hosts two Virtex-6 XC6VHX565T-2FFG1924C FPGAs. This FPGA provides six four-quad GTH and twelve four-quad GTX high speed interfaces.

References

For more detailed information refer to:
http://www.xilinx.com/products/silicon-devices/fpga/virtex-6/hxt.htm

Board Power and Switch

Figure 1-2 callouts [3, 4, 5]

The ML630 board is powered through two 4-pin DIN right angle type connectors J122 and J75 using the two 12V 15A AC-to-DC adapters included with the board.

Power can also be provided through J141 and J102 ATX hard disk type 4-pin power connectors. The DIN4 J122 and ATX J141 connectors are wired in parallel, as are J75 and J102.

Note: Use of a switchable “power bar” (multiple outlet power strip) is recommended for the two ML630 AC adapters. The two adapters can then be turned on and off simultaneously via the power bar on-off switch.

> ***Caution!*** Only use two power supplies of the same type. Power the ML630 board through two connectors at the same time (J122 and J75 or J141 and J102, depending on power supply type). Do NOT apply power to all four power input connectors J122/J75 and J141/J102 at the same time. Doing so may damage the ML630 board and void the board warranty.

When the 12V AC adapters are plugged into the ML630 board and turned on via the multiple outlet AC power strip, 12 VDC is applied to the ML630 12V power planes, and green LED indicators (DS36 and DS49) adjacent to each DIN4 power connector illuminate.

The ML630 board U1 and U2 FPGA power regulators are turned on and off by the “soft” slide switch, SW1. When this switch is in the ON position, power is applied to the FPGAs and the green LEDs adjacent to each active regulator illuminate.

The FPGA U1 and part of FPGA U2 power system block diagram is shown in Figure 1-3. The circuit details may be found on the schematic pages 8 and 51 through 67 as noted in the various function blocks.

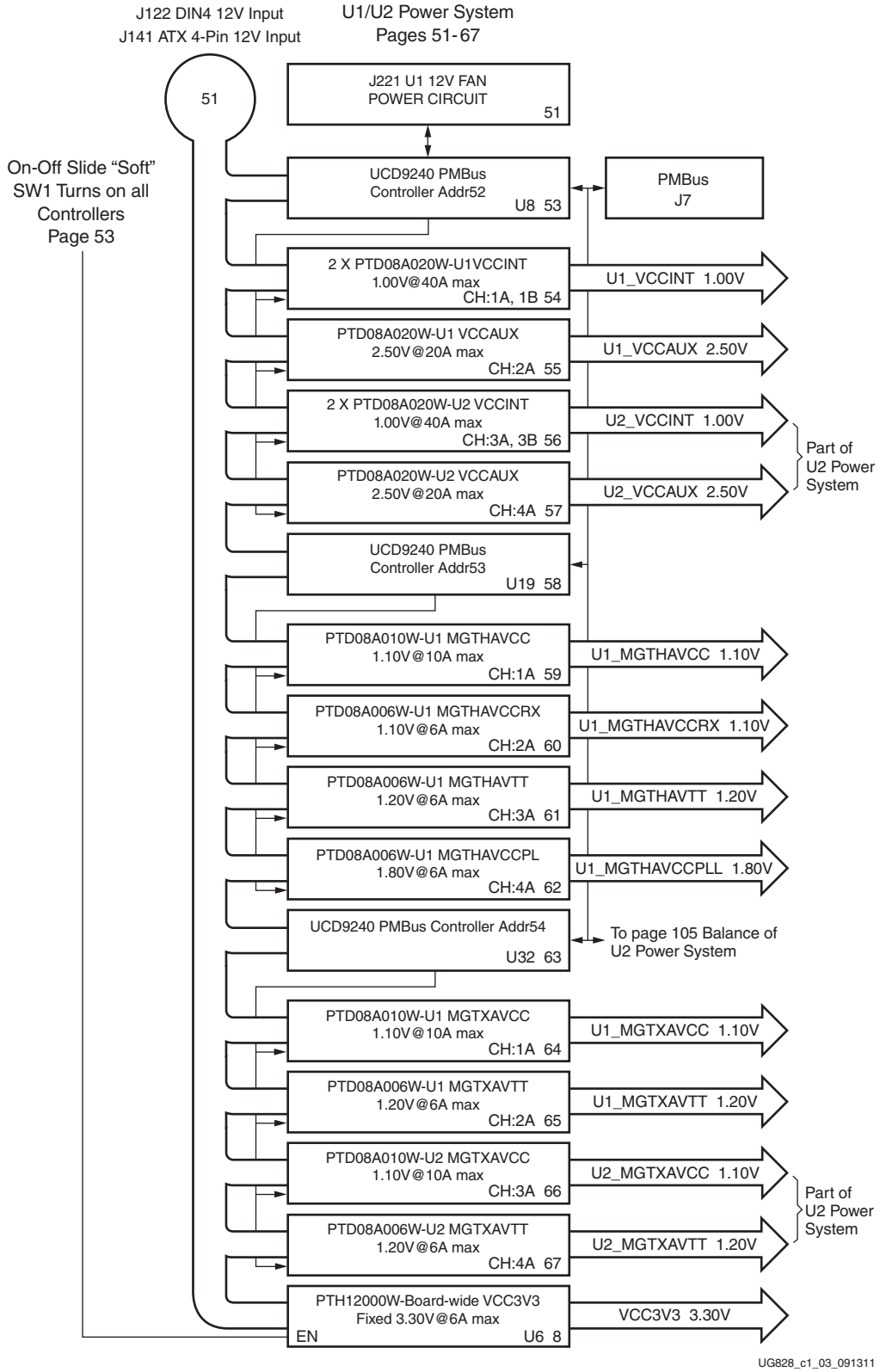

Figure 1-3: **ML630 Board FPGA U1 Power Block Diagram**

Part of the FPGA U2 power system block diagram is shown in, Figure 1-4. The circuit details may be found on the schematic, pages 103 through 109 as noted in the various function blocks.

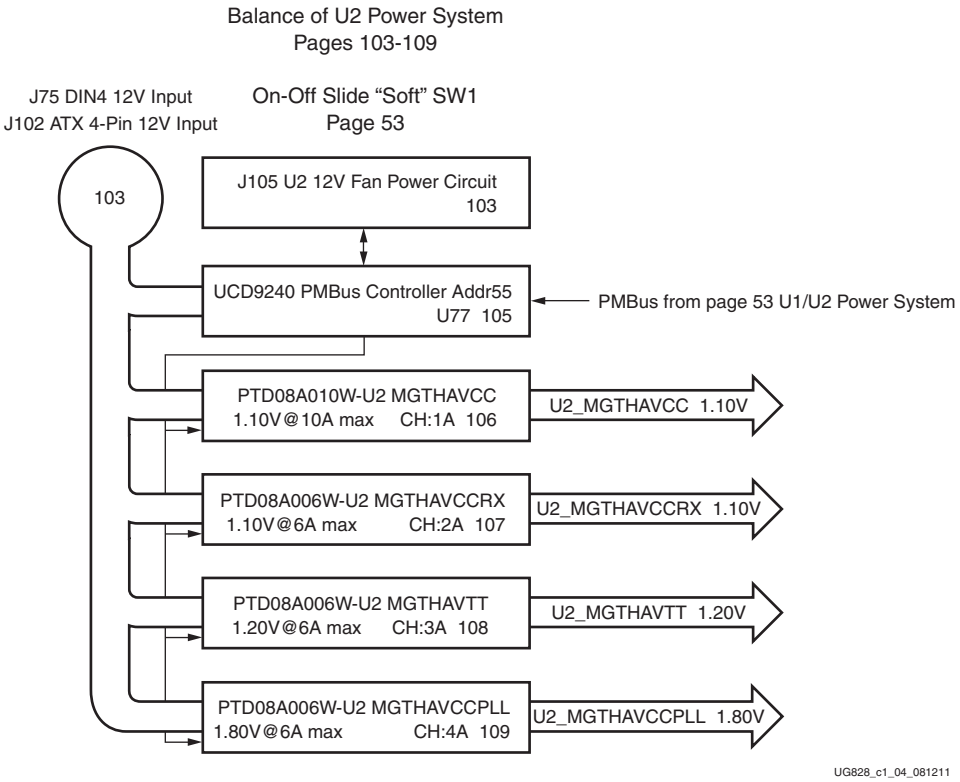

Figure 1-4: **ML630 Board FPGA U2 Power Block Diagram**

The ML630 board uses power regulators and PMBus compliant digital PWM system controllers from Texas Instruments to supply the U1 and U2 voltages listed in Table 1-1.

Table 1-1: **ML630 Onboard Power System Devices**

Device	Reference Designator	Description	Power Rail Net Name	Typical Voltage
U1 and U2 Core Voltage Controller and Regulators				
UCD9240PFC	U8	PMBus compliant digital PWM system controller (address = 52)		
PTD08A020W	U10	Adjustable switching regulator 20A, 0.6V to 3.6V, 1 0f 2 Phases	U1_VCCINT	1.0V
PTD08A020W	U41	Adjustable switching regulator 20A, 0.6V to 3.6V, 2 0f 2 Phases	U1_VCCINT	1.0V
PTD08A020W	U12	Adjustable switching regulator 20A, 0.6V to 3.6V	U1_VCCAUX	2.5V
PTD08A020W	U81	Adjustable switching regulator 20A, 0.6V to 3.6V, 1 0f 2 Phases	U2_VCCINT	1.0V
PTD08A020W	U82	Adjustable switching regulator 20A, 0.6V to 3.6V, 2 0f 2 Phases	U2_VCCINT	1.0V
PTD08A020W	U83	Adjustable switching regulator 20A, 0.6V to 3.6V	U2_VCCAUX	2.5V
U1 GTH Voltage Controller and Regulators				
UCD9240PFC	U19	PMBus compliant digital PWM system controller (address = 53)		
PTD08A010W	U3	Adjustable switching regulator 10A, 0.6V to 3.6V	U1_MGTHAVCC	1.1V
PTD08A006W	U14	Adjustable switching regulator 6A, 0.6V to 3.6V	U1_MGTXAVCCRX	1.1V
PTD08A006W	U20	Adjustable switching regulator 6A, 0.6V to 3.6V	U1_MGTHAVTT	1.2V
PTD08A006W	U21	Adjustable switching regulator 6A, 0.6V to 3.6V	U1_MGTXAVCCPLL	1.8V
U1 and U2 GTX Voltage Controller and Regulators				
UCD9240PFC	U32	PMBus compliant digital PWM system controller (address = 54)		
PTD08A010W	U4	Adjustable switching regulator 10A, 0.6V to 3.6V	U1_MGTXAVCC	1.1V
PTD08A010W	U5	Adjustable switching regulator 10A, 0.6V to 3.6V	U1_MGTXAVTT	1.2V
PTD08A010W	U73	Adjustable switching regulator 10A, 0.6V to 3.6V	U2_MGTXAVCC	1.1V
PTD08A010W	U74	Adjustable switching regulator 10A, 0.6V to 3.6V	U2_MGTXAVTT	1.2V
U2 GTH Voltage Controller and Regulators				
UCD9240PFC	U77	PMBus compliant digital PWM system controller (address = 55)		
PTD08A010W	U72	Adjustable switching regulator 10A, 0.6V to 3.6V	U2_MGTHAVCC	1.1V
PTD08A006W	U67	Adjustable switching regulator 6A, 0.6V to 3.6V	U2_MGTXAVCCRX	1.1V
PTD08A006W	U68	Adjustable switching regulator 6A, 0.6V to 3.6V	U2_MGTHAVTT	1.2V
PTD08A006W	U69	Adjustable switching regulator 6A, 0.6V to 3.6V	U2_MGTXAVCCPLL	1.8V
Auxiliary 3.3V Power				
PTH12000W	U6	Adjustable switching regulator 6A, 1.2 to 5.5V	VCC3V3	3.3V

Disabling FPGA Onboard Power

Figure 1-2 callout [6]

All TI controller PTD type voltage regulators are disabled by installing a jumper across pins 1–2 of header J289.

FPGA Configuration

Figure 1-2 callout [16, 17, 18]

The FPGA is configured in JTAG mode only using one of the following options:

- Embedded USB JTAG circuit (uses USB-A-to-Mini-B cable)
- System ACE controller (utilizing a CompactFlash card loaded with bit files)

The FPGA Embedded JTAG option is chosen by connecting a USB A-to-Mini-B cable to ML630 USB Mini-B connector J20. The USB A end of the cable plugs into the user's PC, which hosts the Xilinx FPGA configuration software tool (either ChipScope™ Pro or Impact) which is then used to configure the two ML630 FPGAs.

The FPGAs can also be configured through the System ACE controller by setting the 3-bit configuration address DIP switches (SW3) to select one of eight bitstreams stored on a CompactFlash memory card plugged into socket U46 (see Table 1-2, page 17).

Upon power-on, the System ACE controller checks for the presence of a flash card and loads the FPGA configuration files from it, if present.

The JTAG chain of the board is illustrated in Figure 1-5. Each component (except the System ACE IC) with a JTAG interface has a bypass jumper which permits the component to be in the chain or bypassed.

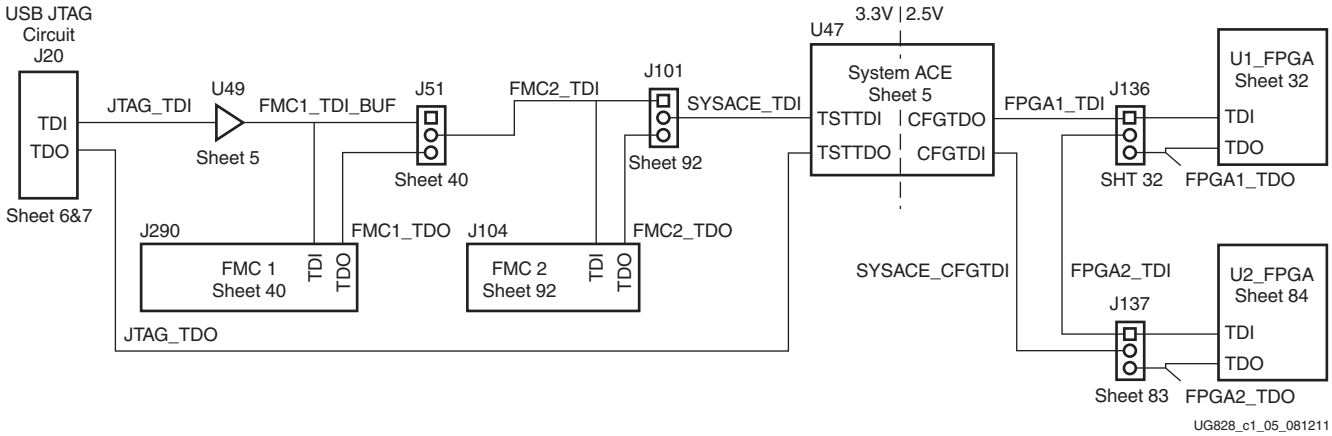

Figure 1-5: **ML630 JTAG Chain Diagram**

System ACE Controller

Figure 1-2 callout [18]

The onboard System ACE controller (U47) allows storage of multiple configuration files on a CompactFlash card. These configuration files can be used to program the FPGAs. The CompactFlash card plugs into the CompactFlash card socket (U46) located directly above the System ACE controller (which is on the bottom side of the board).

System ACE Controller Reset

Figure 1-2 callout [19]

Pressing pushbutton SW2 (RESET) resets the System ACE controller. Reset is an active-Low input.

Configuration Address DIP Switches

Figure 1-2 callout [20]

DIP switch SW3 selects one of the eight configuration bitstream addresses in the CompactFlash memory card. The switch settings for selecting each address are shown in Table 1-2.

Table 1-2: **System ACE SW3 DIP Switch Configuration**

Address	ADR2 (POS1)	ADR1 (POS2)	ADR0 (POS3)
0	O(1)	O	O
1	O	O	C(2)
2	O	C	O
3	O	C	C
4	C	O	O
5	C	O	C
6	C	C	O
7	C	C	C

Notes:

1. O indicates the open switch position (Logic 0).
2. C indicates the closed switch position (Logic 1).
3. The System ACE controller has internal pull-down resistors on its CFGADDR[2:0] pins.

References

More information on the System ACE controller is available in DS080, *System ACE CompactFlash Solution*.

FPGA U1 PROG Pushbutton, INIT LED and DONE LED

Figure 1-2 callout [21]

Pressing the U1 PROG push button (SW5) grounds the active-Low program pin of the FPGA. The INIT LED (DS20) lights during FPGA initialization. The DONE LED (DS56) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, the DONE LED lights indicating that the FPGA is successfully configured.

FPGA U1 User LEDs, DIP and Pushbutton Switches

Figure 1-2 callout [22]

DS10 through DS17 are eight active-High LEDs that are connected to user I/O pins on FPGA U1 as shown in Table 1-3. These LEDs can be used to indicate status or any other purpose determined by the user.

Table 1-3: **FPGA U1 User LEDs**

FPGA U1 Pin	Net Name	Reference Designator
K33	U1_USER_LED1	DS17
L33	U1_USER_LED2	DS16
A37	U1_USER_LED3	DS15
B37	U1_USER_LED4	DS14
B36	U1_USER_LED5	DS13
B35	U1_USER_LED6	DS12
A35	U1_USER_LED7	DS11
A34	U1_USER_LED8	DS10

User DIP Switches (Active High)

Figure 1-2 callout [22]

FPGA U1 DIP switch SW7 provides a set of eight active-High switches that are connected to user I/O pins on the FPGA as shown in Table 1-4. These switched signals can be used to set control bits or any other purpose determined by the user.

Table 1-4: **FPGA U1 User DIP Switches**

FPGA U1 Pin	Net Name	Reference Designator
J20	U1_USER_SW1	SW7
K21	U1_USER_SW2	
P21	U1_USER_SW3	
R21	U1_USER_SW4	
G20	U1_USER_SW5	
H21	U1_USER_SW6	
E20	U1_USER_SW7	
F20	U1_USER_SW8	

User Push Buttons (Active High)

Figure 1-2 callout [22]

SW4, SW6, SW8 and SW9 are active-High user pushbuttons that are connected to user I/O pins on FPGA U1 as shown in Table 1-5. These switches can be used for any purpose determined by the user.

Table 1-5: **FPGA U1 User Pushbuttons**

FPGA U1 Pin	Net Name	Reference Designator
H26	U1_USER_PB1	SW4
J26	U1_USER_PB2	SW6
N24	U1_USER_PB3	SW8
N23	U1_USER_PB4	SW9

FPGA U1 User GPIO Header

Figure 1-2 callout [23]

A standard 2 x 6, 100-mil pitch header (J285) brings out six FPGA I/Os for test purposes. Table 1-6 lists these pins. J285 odd pin numbers are wired to GND (ground).

Table 1-6: **FPGA U1 User GPIO Header J285**

FPGA U1 Pin	Net Name	J285 Pin
J35	U1_USER_IO_1	2
K35	U1_USER_IO_2	4
D35	U1_USER_IO_3	6
E35	U1_USER_IO_4	8
P35	U1_USER_IO_5	10
P34	U1_USER_IO_6	12

FPGA U1 USB to UART Bridge

Figure 1-2 callout [24]

Communications between the ML630 board FPGA U1 and a host computer are accomplished through a USB cable connected to J54. Control is provided by U26, a USB to UART bridge (Silicon Laboratories CP2103). Table 1-7 lists the pin assignments and signals for the USB connector J54.

Table 1-7: **: J54 USB Mini-B Connector Pin Assignments and Signals**

J54 Pin	Signal Name	Description
1	VBUS	+5V from host system
2	U1_USB_D_N	Bidirectional differential serial data (N-side)

Table 1-7: **: J54 USB Mini-B Connector Pin Assignments and Signals *(Cont'd)***

J54 Pin	Signal Name	Description
3	U1_USB_D_P	Bidirectional differential serial data (P-side)
4	ID	Not used

The CP2103 supports an I/O voltage range of 2.5V on the ML630 board. The connections between FPGA U1 and CP2103 should use the LVCMOS25 I/O standard. UART IP (for example, Xilinx® XPS UART Lite) must be implemented in the FPGA logic. FPGA U1 supports the USB to UART bridge using four signal pins:

- Transmit (TX)
- Receive (RX)
- Request to Send (RTS)
- Clear to Send (CTS)

Connections of these signals between the FPGA and the CP2103 at U26 are listed in Table 1-8.

Table 1-8: **FPGA U1 to U26 (CP2103 Bridge) Connections**

FPGA U1 Pin	FPGA Function	Net Name	U26 Pin	U26 Function
P11	RTS, output	U1_USB_CTS_I	22	CTS, input
P10	CTS, input	U1_USB_RTS_O	23	RTS, output
P10	TX, data out	U1_USB_RXD_I	24	RXD, data in
E10	RX, data in	U1_USB_TXD_O	25	TXD, data out

The bridge device also provides as many as four GPIO signals that can be defined by the user for status and control information (see Table 1-9).

Table 1-9: **FPGA U1 to U26 (CP2103 Bridge) User GPIO Connections**

FPGA U1 Pin	Net Name	U26 Pin
L10	U1_USB_GPIO_0	19
M11	U1_USB_GPIO_1	18
D10	U1_USB_GPIO_2	17
E11	U1_USB_GPIO_3	16

A royalty-free software driver named Virtual COM Port (VCP) is available from Silicon Laboratories. This driver permits the CP2103 USB to UART bridge to appear as a COM port to the host computer communications application software (for example, HyperTerminal or TeraTerm). The VCP driver must be installed on the host computer prior to establishing communications with the ML630 board.

References

More information on the Silicon Labs CP2103 USB-to-UART bridge is available at: http://www.silabs.com/products/interface/usbtouart/Pages/default.aspx.

FPGA U1 200 MHz 2.5V LVDS Oscillator

Figure 1-2 callout [25]

The ML630 board has one SiTime 2.5V LVDS differential fixed 200 MHz oscillator per FPGA. Oscillator U22 (located on the bottom of the board) is connected to FPGA U1 as listed in Table 1-10.

Table 1-10: **FPGA U1 LVDS Oscillator U22 Global Clock Connections**

FPGA U1 Pin	Net Name	U22 Pin
J33	U1_LVDS_OSC_P	4
H33	U1_LVDS_OSC_N	5

References

More information on the SiTime SI9102AI oscillator is available at: http://www.sitime.com/products/differential-oscillators/sit9102.

FPGA U2 PROG Push Button, INIT LED and DONE LED

Figure 1-2 callout [26]

Pressing the U2 PROG pushbutton (SW11) grounds the active-Low program pin of the FPGA. The INIT LED (DS54) lights during FPGA initialization. The DONE LED (DS29) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, the DONE LED lights indicating that the FPGA is successfully configured.

FPGA U2 User LEDs, DIP and Pushbutton Switches

Figure 1-2 callout [27]

DS30 through DS35, DS37, and DS38 are eight active-High LEDs that are connected to user I/O pins on FPGA U2 as shown in Table 1-11. These LEDs can be used to indicate status or any other purpose determined by the user.

Table 1-11: **FPGA U2 User LEDs**

FPGA U2 Pin	Net Name	Reference Designator
K33	U2_USER_LED1	DS38
L33	U2_USER_LED2	DS37
A37	U2_USER_LED3	DS35
B37	U2_USER_LED4	DS34
B36	U2_USER_LED5	DS33
B35	U2_USER_LED6	DS32
A35	U2_USER_LED7	DS31
A34	U2_USER_LED8	DS30

FPGA U2 User DIP Switches (Active High)

Figure 1-2 callout [27]

FPGA U1 DIP switch SW16 provides a set of eight active-High switches that are connected to user I/O pins on the FPGA as shown in Table 1-12. These switched signals can be used to set control bits or any other purpose determined by the user.

Table 1-12: **FPGA U2 User DIP Switches**

FPGA U2 Pin	Net Name	Reference Designator
J20	U2_USER_SW1	SW16
K21	U2_USER_SW2	
P21	U2_USER_SW3	
R21	U2_USER_SW4	
G20	U2_USER_SW5	
H21	U2_USER_SW6	
E20	U2_USER_SW7	
F20	U2_USER_SW8	

User Push Buttons (Active High)

Figure 1-2 callout [27]

SW12, SW13, SW14 and SW15 are active-High user pushbuttons that are connected to user I/O pins on FPGA U2 as shown in Table 1-13. These switches can be used for any purpose determined by the user.

Table 1-13: **FPGA U2 User Pushbuttons**

FPGA U2 Pin	Net Name	Reference Designator
H26	U2_USER_PB1	SW12
J26	U2_USER_PB2	SW13
N24	U2_USER_PB3	SW14
N23	U2_USER_PB4	SW15

FPGA U2 User GPIO Header

Figure 1-2 callout [28]

A standard 2 x 6, 100-mil pitch header (J103) brings out six FPGA I/Os for test purposes. Table 1-14 lists these pins. J103 odd pin numbers are wired to GND (ground).

Table 1-14: **FPGA U2 User GPIO Header J103**

FPGA U1 Pin	Net Name	J103 Pin
J35	U2_USER_IO_1	2
K35	U2_USER_IO_2	4
D35	U2_USER_IO_3	6
E35	U2_USER_IO_4	8
P35	U2_USER_IO_5	10
P34	U2_USER_IO_6	12

FPGA U2 USB to UART Bridge

Figure 1-2 callout [29]

Communications between the ML630 board FPGA U2 and a host computer are accomplished through a USB cable connected to J106. Control is provided by U79, a USB to UART bridge (Silicon Laboratories CP2103). Table 1-15 lists the pin assignments and signals for the USB connector J106.

Table 1-15: **J106 USB Mini-B Connector Pin Assignments and Signals**

J106 Pin	Signal Name	Description
1	VBUS	+5V from host system
2	U2_USB_D_N	Bidirectional differential serial data (N-side)
3	U2_USB_D_P	Bidirectional differential serial data (P-side)
4	ID	Not used8

The CP2103 supports an I/O voltage range of 2.5V on the ML630 board. The connections between FPGA U2 and CP2103 should use the LVCMOS25 I/O standard. UART IP (for example, Xilinx® XPS UART Lite) must be implemented in the FPGA logic. FPGA U2 supports the USB to UART bridge using four signal pins:

- Transmit (TX)
- Receive (RX)
- Request to Send (RTS)
- Clear to Send (CTS)

Connections of these signals between the FPGA and the CP2103 at U79 are listed in Table 1-16.

Table 1-16: **FPGA U2 to U79 (CP2103 Bridge) Connections**

FPGA U2 Pin	FPGA Function	Net Name	U79 Pin	U79 Function
P11	RTS, output	U2_USB_CTS_I	22	CTS, input
P10	CTS, input	U2_USB_RTS_O	23	RTS, output
F10	TX, data out	U2_USB_RXD_I	24	RXD, data in
E10	RX, data in	U2_USB_TXD_O	25	TXD, data out

The bridge device also provides as many as four GPIO signals that can be defined by the user for status and control information (see Table 1-17).

Table 1-17: **FPGA U2 to U79 (CP2103 Bridge) User GPIO Connections**

FPGA U2 Pin	Net Name	U79 Pin
L10	U2_USB_GPIO_0	19
M11	U2_USB_GPIO_1	18
D10	U2_USB_GPIO_2	17
E11	U2_USB_GPIO_3	16

A royalty-free software driver named Virtual COM Port (VCP) is available from Silicon Laboratories. This driver permits the CP2103 USB to UART bridge to appear as a COM port to the host computer communications application software (for example, HyperTerminal or TeraTerm). The VCP driver must be installed on the host computer prior to establishing communications with the ML630 board.

References

More information on the Silicon Labs CP2103 USB-to-UART bridge is available at: http://www.silabs.com/products/interface/usbtouart/Pages/default.aspx.

FPGA U2 200 MHz 2.5V LVDS Oscillator

Figure 1-2 callout [30]

Oscillator U63, located on the bottom of the board, is connected to FPGA U2 global clock inputs. Table 1-18 lists FPGA U2 pin connections to the LVDS oscillator U63.

Table 1-18: **FPGA U2 LVDS Oscillator U63 Global Clock Connections**

FPGA U2 Pin	Net Name	U63 Pin
AR33	U2_LVDS_OSC_P	4
AT33	U2_LVDS_OSC_N	5

References

More information on the SiTime SI9102AI oscillator is available at: http://www.sitime.com/products/differential-oscillators/sit9102.

FPGA U1 FCI Airmax Interlaken Connectors

Figure 1-2 callout [31, 32, 34]

The ML630 board provides four sets of FCI Airmax male/female (plug/receptacle) connector pairs implementing the Interlaken protocol.

Note: The Interlaken protocol definition and recommended connector pinouts can be found in the following documents located on the Interlaken Alliance website (http://www.interlakenalliance.com): Protocol: Interlaken Protocol Definition v1.x and Connector Pinouts: Interlaken Interop Recommendations v1.x. The Protocol Definition document also discusses the flow control functions provided by the TX and RX FC_CLK, FC_DATA and FC_SYNC connector pins.

Three sets of connector pairs (P1/J1, P2/J2, and P3/J3) are wired to FPGA U1. Table 1-19 through Table 1-24 show FPGA U1 to FCI connector details. Refer to the block diagram on the ML630 schematic, page 2, for an overview of the connectivity shown in these tables.

Table 1-19: **FCI Connector P1**

FCI Connector P1			U1 FPGA
Pin Name	**Pin No.**	**Net Name**	**Pin No.**
TX0_P	A7	U1_MGTTX0_115_P	AA3
TX0_N	B7	U1_MGTTX0_115_N	AA4
TX1_P	D6	U1_MGTTX1_115_P	Y1
TX1_N	E6	U1_MGTTX1_115_N	Y2
TX2_P	D8	U1_MGTTX2_115_P	W3
TX2_N	E8	U1_MGTTX2_115_N	W4
TX3_P	A9	U1_MGTTX3_115_P	V1
TX3_N	B9	U1_MGTTX3_115_N	V2
TX4_P	A3	U1_MGTTX1_114_P	AD1
TX4_N	B3	U1_MGTTX1_114_N	AD2
TX5_P	D2	U1_MGTTX0_114_P	AE3
TX5_N	E2	U1_MGTTX0_114_N	AE4
TX6_P	D4	U1_MGTTX2_114_P	AC3
TX6_N	E4	U1_MGTTX2_114_N	AC4
TX7_P	A5	U1_MGTTX3_114_P	AB1
TX7_N	B5	U1_MGTTX3_114_N	AB2
TX_REFCLK_P	A1	U1_P1_TX_REFCLK_C_P	U13.16
TX_REFCLK_N	B1	U1_P1_TX_REFCLK_C_N	U13.17
TX_FC_CK	E10	U1_AMH1_FC_CK	A10
TX8_P	G5	U1_MGTTX3_113_P	AF1
TX8_N	H5	U1_MGTTX3_113_N	AF2
TX9_P	G3	U1_MGTTX1_113_P	AH1
TX9_N	H3	U1_MGTTX1_113_N	AH2
TX10_P	J4	U1_MGTTX2_113_P	AG3
TX10_N	K4	U1_MGTTX2_113_N	AG4
TX11_P	G1	U1_MGTTX0_113_P	AJ3
TX11_N	H1	U1_MGTTX0_113_N	AJ4
TX12_P	J6	U1_AMH1_IO0	BB24
TX12_N	K6	U1_AMH1_IO1	BA24
TX13_P	J10	U1_AMH1_IO2	BC26
TX13_N	K10	U1_AMH1_IO3	BB26
TX14_P	J2	U1_AMH1_IO4	AP23
TX14_N	K2	U1_AMH1_IO5	AN23
TX15_P	J8	U1_AMH1_IO6	AY26
TX15_N	K8	U1_AMH1_IO7	AW26
TX_FC_DATA	H7	U1_AMH1_FC_DATA	B11
TX_FC_SYNC	H9	U1_AMH1_FC_SYNC	A12

Notes:
1. U1_P1_TX_REFCLK_C_P/N is AC coupled with 0.1 uF series capacitors.

Table 1-20: **FCI Connector J1**

FCI Connector J1			U1 FPGA
Pin Name	**Pin No.**	**Net Name**	**Pin No.**
RX0_P	A7	U1_MGTRX0_115_C_P	Y5
RX0_N	B7	U1_MGTRX0_115_C_N	Y6
RX1_P	D6	U1_MGTRX1_115_C_P	W7
RX1_N	E6	U1_MGTRX1_115_C_N	W8
RX2_P	D8	U1_MGTRX2_115_C_P	V5
RX2_N	E8	U1_MGTRX2_115_C_N	V6
RX3_P	A9	U1_MGTRX3_115_C_P	U7
RX3_N	B9	U1_MGTRX3_115_C_N	U8
RX4_P	A3	U1_MGTRX1_114_C_P	AC7
RX4_N	B3	U1_MGTRX1_114_C_N	AC8
RX5_P	D2	U1_MGTRX0_114_C_P	AD5
RX5_N	E2	U1_MGTRX0_114_C_N	AD6
RX6_P	D4	U1_MGTRX2_114_C_P	AB5
RX6_N	E4	U1_MGTRX2_114_C_N	AB6
RX7_P	A5	U1_MGTRX3_114_C_P	AA7
RX7_N	B5	U1_MGTRX3_114_C_N	AA8
RX_REFCLK_P	A1	U1_J1_RX_REFCLK_P	Y10
RX_REFCLK_N	B1	U1_J1_RX_REFCLK_N	Y9
RX_FC_CK	E10	U1_AMR1_FC_CK	A13
RX8_P	G5	U1_MGTRX3_113_C_P	AE7
RX8_N	H5	U1_MGTRX3_113_C_N	AE8
RX9_P	G3	U1_MGTRX1_113_C_P	AG7
RX9_N	H3	U1_MGTRX1_113_C_N	AG8
RX10_P	J4	U1_MGTRX2_113_C_P	AF5
RX10_N	K4	U1_MGTRX2_113_C_N	AF6
RX11_P	G1	U1_MGTRX0_113_C_P	AH5
RX11_N	H1	U1_MGTRX0_113_C_N	AH6
RX12_P	J6	NC	
RX12_N	K6	NC	
RX13_P	J10	NC	
RX13_N	K10	NC	
RX14_P	J2	NC	
RX14_N	K2	NC	
RX15_P	J8	NC	
RX15_N	K8	NC	
RX_FC_DATA	H7	U1_AMR1_FC_DATA	C11
RX_FC_SYNC	H9	U1_AMR1_FC_SYNC	C12

Notes:
1. U1_J1_RX_REFCLK_C_P/N is AC coupled with 0.1 uF series capacitors.
2. All MGTRXn receive nets are AC coupled with 0.1 uF series capacitors.

Table 1-21: **FCI Connector P2**

FCI Connector P2			U1 FPGA
Pin Name	**Pin No.**	**Net Name**	**Pin No.**
TX0_P	A7	U1_MGTTX1_111_P	AT1
TX0_N	B7	U1_MGTTX1_111_N	AT2
TX1_P	D6	U1_MGTTX0_111_P	AU3
TX1_N	E6	U1_MGTTX0_111_N	AU4
TX2_P	D8	U1_MGTTX2_111_P	AR3
TX2_N	E8	U1_MGTTX2_111_N	AR4
TX3_P	A9	U1_MGTTX3_111_P	AP1
TX3_N	B9	U1_MGTTX3_111_N	AP2
TX4_P	A3	U1_MGTTX0_110_P	BB1
TX4_N	B3	U1_MGTTX0_110_N	BB2
TX5_P	D2	U1_MGTTX2_110_P	AW3
TX5_N	E2	U1_MGTTX2_110_N	AW4
TX6_P	D4	U1_MGTTX1_110_P	AY1
TX6_N	E4	U1_MGTTX1_110_N	AY2
TX7_P	A5	U1_MGTTX3_110_P	AV1
TX7_N	B5	U1_MGTTX3_110_N	AV2
TX_REFCLK_P	A1	U1_P2_TX_REFCLK_C_P	U13.19
TX_REFCLK_N	B1	U1_P2_TX_REFCLK_C_N	U13.20
TX_FC_CK	E10	U1_AMH2_FC_CK	B12
TX8_P	G5	U1_MGTTX2_112_P	AL3
TX8_N	H5	U1_MGTTX2_112_N	AL4
TX9_P	G3	U1_MGTTX0_112_P	AN3
TX9_N	H3	U1_MGTTX0_112_N	AN4
TX10_P	J4	U1_MGTTX3_112_P	AK1
TX10_N	K4	U1_MGTTX3_112_N	AK2
TX11_P	G1	U1_MGTTX1_112_P	AM1
TX11_N	H1	U1_MGTTX1_112_N	AM2
TX12_P	J6	U1_AMH2_IO0	BD26
TX12_N	K6	U1_AMH2_IO1	BD25
TX13_P	J10	U1_AMH2_IO2	AL23
TX13_N	K10	U1_AMH2_IO3	AK23
TX14_P	J2	U1_AMH2_IO4	AY25
TX14_N	K2	U1_AMH2_IO5	AW25
TX15_P	J8	U1_AMH2_IO6	AV26
TX15_N	K8	U1_AMH2_IO7	AU26
TX_FC_DATA	H7	U1_AMH2_FC_DATA	C13
TX_FC_SYNC	H9	U1_AMH2_FC_SYNC	A8

Notes:
1. U1_P2_TX_REFCLK_C_P/N is AC coupled with 0.1 uF series capacitors.

Table 1-22: **FCI Connector J2**

FCI Connector J2			U1 FPGA
Pin Name	**Pin No.**	**Net Name**	**Pin No.**
RX0_P	A7	U1_MGTRX1_111_C_P	AV5
RX0_N	B7	U1_MGTRX1_111_C_N	AV6
RX1_P	D6	U1_MGTRX0_111_C_P	AY5
RX1_N	E6	U1_MGTRX0_111_C_N	AY6
RX2_P	D8	U1_MGTRX2_111_C_P	AT5
RX2_N	E8	U1_MGTRX2_111_C_N	AT6
RX3_P	A9	U1_MGTRX3_111_C_P	AP5
RX3_N	B9	U1_MGTRX3_111_C_N	AP6
RX4_P	A3	U1_MGTRX0_110_C_P	BD5
RX4_N	B3	U1_MGTRX0_110_C_N	BD6
RX5_P	D2	U1_MGTRX2_110_C_P	BB5
RX5_N	E2	U1_MGTRX2_110_C_N	BB6
RX6_P	D4	U1_MGTRX1_110_C_P	BC3
RX6_N	E4	U1_MGTRX1_110_C_N	BC4
RX7_P	A5	U1_MGTRX3_110_C_P	BA3
RX7_N	B5	U1_MGTRX3_110_C_N	BA4
RX_REFCLK_P	A1	U1_J2_RX_REFCLK_P	AR8
RX_REFCLK_N	B1	U1_J2_RX_REFCLK_N	AR7
RX_FC_CK	E10	U1_AMR2_FC_CK	B9
RX8_P	G5	U1_MGTRX2_112_C_P	AJ7
RX8_N	H5	U1_MGTRX2_112_C_N	AJ8
RX9_P	G3	U1_MGTRX0_112_C_P	AL7
RX9_N	H3	U1_MGTRX0_112_C_N	AL8
RX10_P	J4	U1_MGTRX3_112_C_P	AK5
RX10_N	K4	U1_MGTRX3_112_C_N	AK6
RX11_P	G1	U1_MGTRX1_112_C_P	AM5
RX11_N	H1	U1_MGTRX1_112_C_N	AM6
RX12_P	J6	NC	
RX12_N	K6	NC	
RX13_P	J10	NC	
RX13_N	K10	NC	
RX14_P	J2	NC	
RX14_N	K2	NC	
RX15_P	J8	NC	
RX15_N	K8	NC	
RX_FC_DATA	H7	U1_AMR2_FC_DATA	R12
RX_FC_SYNC	H9	U1_AMR2_FC_SYNC	R13

Notes:
1. U1_J2_RX_REFCLK_C_P/N is AC coupled with 0.1 uF series capacitors.
2. All MGTRXn receive nets are AC coupled with 0.1 uF series capacitors.

Table 1-23: **FCI Connector P3**

FCI Connector P3			U1 FPGA
Pin Name	**Pin No.**	**Net Name**	**Pin No.**
TX0_P	A7	U1_MGTTX1_107_P	K43
TX0_N	B7	U1_MGTTX1_107_N	K44
TX1_P	D6	U1_MGTTX0_107_P	L41
TX1_N	E6	U1_MGTTX0_107_N	L42
TX2_P	D8	U1_MGTTX1_106_P	P43
TX2_N	E8	U1_MGTTX1_106_N	P44
TX3_P	A9	U1_MGTTX0_106_P	T43
TX3_N	B9	U1_MGTTX0_106_N	T44
TX4_P	A3	U1_MGTTX0_108_P	F43
TX4_N	B3	U1_MGTTX0_108_N	F44
TX5_P	D2	U1_MGTTX1_108_P	D43
TX5_N	E2	U1_MGTTX1_108_N	D44
TX6_P	D4	U1_MGTTX0_118_P	F2
TX6_N	E4	U1_MGTTX0_118_N	F1
TX7_P	A5	U1_MGTTX1_118_P	D2
TX7_N	B5	U1_MGTTX1_118_N	D1
TX_REFCLK_P	A1	U1_P3_TX_REFCLK_C_P	U18.16
TX_REFCLK_N	B1	U1_P3_TX_REFCLK_C_N	U18.17
TX_FC_CK	E10	U1_AMH3_FC_CK	D11
TX8_P	G5	U1_MGTTX0_117_P	L4
TX8_N	H5	U1_MGTTX0_117_N	L3
TX9_P	G3	U1_MGTTX1_117_P	K2
TX9_N	H3	U1_MGTTX1_117_N	K1
TX10_P	J4	U1_MGTTX1_116_P	P2
TX10_N	K4	U1_MGTTX1_116_N	P1
TX11_P	G1	U1_MGTTX0_116_P	T2
TX11_N	H1	U1_MGTTX0_116_N	T1
TX12_P	J6	U1_AMH3_IO0	R32
TX12_N	K6	U1_AMH3_IO1	R31
TX13_P	J10	U1_AMH3_IO2	H34
TX13_N	K10	U1_AMH3_IO3	J34
TX14_P	J2	U1_AMH3_IO4	P33
TX14_N	K2	U1_AMH3_IO5	R33
TX15_P	J8	U1_AMH3_IO6	F34
TX15_N	K8	U1_AMH3_IO7	G34
TX_FC_DATA	H7	U1_AMH3_FC_DATA	E12
TX_FC_SYNC	H9	U1_AMH3_FC_SYNC	A9

Table 1-24: **FCI Connector J3**

FCI Connector J3			U1 FPGA
Pin Name	**Pin No.**	**Net Name**	**Pin No.**
RX0_P	A7	U1_MGTRX1_107_C_P	L37
RX0_N	B7	U1_MGTRX1_107_C_N	L38
RX1_P	D6	U1_MGTRX0_107_C_P	K39
RX1_N	E6	U1_MGTRX0_107_C_N	K40
RX2_P	D8	U1_MGTRX1_106_C_P	T39
RX2_N	E8	U1_MGTRX1_106_C_N	T40
RX3_P	A9	U1_MGTRX0_106_C_P	U41
RX3_N	B9	U1_MGTRX0_106_C_N	U42
RX4_P	A3	U1_MGTRX0_108_C_P	G37
RX4_N	B3	U1_MGTRX0_108_C_N	G38
RX5_P	D2	U1_MGTRX1_108_C_P	F39
RX5_N	E2	U1_MGTRX1_108_C_N	F40
RX6_P	D4	U1_MGTRX0_118_C_P	G8
RX6_N	E4	U1_MGTRX0_118_C_N	G7
RX7_P	A5	U1_MGTRX1_118_C_P	F6
RX7_N	B5	U1_MGTRX1_118_C_N	F5
RX_REFCLK_P	A1	U1_J3_RX_REFCLK_P	J132
RX_REFCLK_N	B1	U1_J3_RX_REFCLK_N	J133
RX_FC_CK	E10	U1_AMR3_FC_CK	B10
RX8_P	G5	U1_MGTRX0_117_C_P	K6
RX8_N	H5	U1_MGTRX0_117_C_N	K5
RX9_P	G3	U1_MGTRX1_117_C_P	L8
RX9_N	H3	U1_MGTRX1_117_C_N	L7
RX10_P	J4	U1_MGTRX1_116_C_P	T6
RX10_N	K4	U1_MGTRX1_116_C_N	T5
RX11_P	G1	U1_MGTRX0_116_C_P	U4
RX11_N	H1	U1_MGTRX0_116_C_N	U3
RX12_P	J6	NC	
RX12_N	K6	NC	
RX13_P	J10	NC	
RX13_N	K10	NC	
RX14_P	J2	NC	
RX14_N	K2	NC	
RX15_P	J8	NC	
RX15_N	K8	NC	
RX_FC_DATA	H7	U1_AMR3_FC_DATA	G10
RX_FC_SYNC	H9	U1_AMR3_FC_SYNC	H11

Notes:
1. U1_J3_RX_REFCLK_C_P/N is AC coupled with 0.1 uF series capacitors.
2. All MGTRXn receive nets are AC coupled with 0.1 uF series capacitors.

FPGA U1 FCI J3 RX Reference Clock to SMA Connection

Figure 1-2 callout [33]

The J3 FCI Airmax receptacle RX reference clock is wired to the SMA pair J132 and J133 as shown in Table 1-25.

Table 1-25: **FCI J3 RX Reference Clock to SMA Connection**

FCI Connector J3			SMA Connection
Pin Name	**Pin No.**	**Net Name**	**SMA Pin No.**
RX_REFCLK_P	A1	U1_J3_RX_REFCLK_P	J132.1
RX_REFCLK_N	B1	U1_J3_RX_REFCLK_N	J133.1

FPGA U2 FCI Airmax Interlaken Connectors

Figure 1-2 callout [35]

Table 1-26 and Table 1-27 show FPGA U2 to FCI connector P4/J4 details. Refer to the block diagram on the ML630 schematic, page 3, for an overview of the connectivity shown in these tables.

Table 1-26: **FCI Connector P4**

FCI Connector P4			U2 FPGA
Pin Name	**Pin No.**	**Net Name**	**Pin No.**
TX0_P	A7	U2_MGTTX1_107_P	K43
TX0_N	B7	U2_MGTTX1_107_N	K44
TX1_P	D6	U2_MGTTX0_107_P	L41
TX1_N	E6	U2_MGTTX0_107_N	L42
TX2_P	D8	U2_MGTTX1_106_P	P43
TX2_N	E8	U2_MGTTX1_106_N	P44
TX3_P	A9	U2_MGTTX0_106_P	T43
TX3_N	B9	U2_MGTTX0_106_N	T44
TX4_P	A3	U2_MGTTX0_108_P	F43
TX4_N	B3	U2_MGTTX0_108_N	F44
TX5_P	D2	U2_MGTTX1_108_P	D43
TX5_N	E2	U2_MGTTX1_108_N	D44
TX6_P	D4	U2_MGTTX0_118_P	F2
TX6_N	E4	U2_MGTTX0_118_N	F1
TX7_P	A5	U2_MGTTX1_118_P	D2
TX7_N	B5	U2_MGTTX1_118_N	D1
TX_REFCLK_P	A1	U2_P4_TX_REFCLK_C_P	U18.19
TX_REFCLK_N	B1	U2_P4_TX_REFCLK_C_N	U18.20
TX_FC_CK	E10	U2_AMH4_FC_CK	A10
TX8_P	G5	U2_MGTTX0_117_P	L4
TX8_N	H5	U2_MGTTX0_117_N	L3
TX9_P	G3	U2_MGTTX1_117_P	K2
TX9_N	H3	U2_MGTTX1_117_N	K1
TX10_P	J4	U2_MGTTX1_116_P	P2
TX10_N	K4	U2_MGTTX1_116_N	P1
TX11_P	G1	U2_MGTTX0_116_P	T2
TX11_N	H1	U2_MGTTX0_116_N	T1
TX12_P	J6	U2_AMH4_IO0	R32
TX12_N	K6	U2_AMH4_IO1	R31
TX13_P	J10	U2_AMH4_IO2	H34
TX13_N	K10	U2_AMH4_IO3	J34
TX14_P	J2	U2_AMH4_IO4	P33
TX14_N	K2	U2_AMH4_IO5	R33
TX15_P	J8	U2_AMH4_IO6	F34
TX15_N	K8	U2_AMH4_IO7	G34
TX_FC_DATA	H7	U2_AMH4_FC_DATA	B11
TX_FC_SYNC	H9	U2_AMH4_FC_SYNC	A12

Table 1-27: **FCI Connector J4**

FCI Connector J4			U2 FPGA
Pin Name	**Pin No.**	**Net Name**	**Pin No.**
RX0_P	A7	U2_MGTRX1_107_C_P	L37
RX0_N	B7	U2_MGTRX1_107_C_N	L38
RX1_P	D6	U2_MGTRX0_107_C_P	K39
RX1_N	E6	U2_MGTRX0_107_C_N	K40
RX2_P	D8	U2_MGTRX1_106_C_P	T39
RX2_N	E8	U2_MGTRX1_106_C_N	T40
RX3_P	A9	U2_MGTRX0_106_C_P	U41
RX3_N	B9	U2_MGTRX0_106_C_N	U42
RX4_P	A3	U2_MGTRX0_108_C_P	G37
RX4_N	B3	U2_MGTRX0_108_C_N	G38
RX5_P	D2	U2_MGTRX1_108_C_P	F39
RX5_N	E2	U2_MGTRX1_108_C_N	F40
RX6_P	D4	U2_MGTRX0_118_C_P	G8
RX6_N	E4	U2_MGTRX0_118_C_N	G7
RX7_P	A5	U2_MGTRX1_118_C_P	F6
RX7_N	B5	U2_MGTRX1_118_C_N	F5
RX_REFCLK_P	A1	U2_J4_RX_REFCLK_P	J134
RX_REFCLK_N	B1	U2_J4_RX_REFCLK_N	J135
RX_FC_CK	E10	U2_AMR4_FC_CK	A13
RX8_P	G5	U2_MGTRX0_117_C_P	K6
RX8_N	H5	U2_MGTRX0_117_C_N	K5
RX9_P	G3	U2_MGTRX1_117_C_P	L8
RX9_N	H3	U2_MGTRX1_117_C_N	L7
RX10_P	J4	U2_MGTRX1_116_C_P	T6
RX10_N	K4	U2_MGTRX1_116_C_N	T5
RX11_P	G1	U2_MGTRX0_116_C_P	U4
RX11_N	H1	U2_MGTRX0_116_C_N	U3
RX12_P	J6	NC	
RX12_N	K6	NC	
RX13_P	J10	NC	
RX13_N	K10	NC	
RX14_P	J2	NC	
RX14_N	K2	NC	
RX15_P	J8	NC	
RX15_N	K8	NC	
RX_FC_DATA	H7	U2_AMR4_FC_DATA	C11
RX_FC_SYNC	H9	U2_AMR4_FC_SYNC	C12

Notes:

1. U1_J4_RX_REFCLK_C_P/N is AC coupled with 0.1 uF series capacitors.
2. All MGTRXn receive nets are AC coupled with 0.1uF series capacitors.

PGA U2 FCI J4 RX Reference Clock to SMA Connection

Figure 1-2 callout [36]

The J4 FCI Airmax receptacle RX reference clock is wired to the SMA pair J134 and J135 as shown in Table 1-28.

Table 1-28: **FCI J4 RX Reference Clock to SMA Connection**

FCI Connector J4			SMA Connection
Pin Name	**Pin No.**	**Net Name**	**SMA Pin No.**
RX_REFCLK_P	A1	U1_J4_RX_REFCLK_P	J134.1
RX_REFCLK_N	B1	U1_J4_RX_REFCLK_N	J135.1

FPGA U1 GTX to FPGA U2 GTX Interface

Figure 1-2 callout [1, 2]

The ML630 board FPGAs implement six GTX direct U1-to-U2 connections. FPGA U1 Banks GTX100 through 105 are wired directly to FPGA U2 GTX110 through 115. Table 1-29 through Table 1-34 show the details of this U1 to U2 interconnectivity.

Table 1-29: **FPGA U1 GTX100 to FPGA U2 GTX110 Connections**

U1 Bank 100			FPGA U2 Bank MGTX110	
Pin Name	**Pin No.**	**Net Name**	**Pin No.**	**Pin Name**
MGTTXP0_100_BB44	BB44	U1_MGTTX0_100_P	BD5	MGTRXP0_110_BD5
MGTTXN0_100_BB43	BB43	U1_MGTTX0_100_N	BD6	MGTRXN0_110_BD6
MGTTXP1_100_AY44	AY44	U1_MGTTX1_100_P	BC3	MGTRXP1_110_BC3
MGTTXN1_100_AY43	AY43	U1_MGTTX1_100_N	BC4	MGTRXN1_110_BC4
MGTTXP2_100_AW42	AW42	U1_MGTTX2_100_P	BB5	MGTRXP2_110_BB5
MGTTXN2_100_AW41	AW41	U1_MGTTX2_100_N	BB6	MGTRXN2_110_BB6
MGTTXP3_100_AV44	AV44	U1_MGTTX3_100_P	BA3	MGTRXP3_110_BA3
MGTTXN3_100_AV43	AV43	U1_MGTTX3_100_N	BA4	MGTRXN3_110_BA4
MGTRXP0_100_BD40	BD40	U2_MGTTX0_110_P	BB1	MGTTXP0_110_BB1
MGTRXN0_100_BD39	BD39	U2_MGTTX0_110_N	BB2	MGTTXN0_110_BB2
MGTRXP1_100_BC42	BC42	U2_MGTTX1_110_P	AY1	MGTTXP1_110_AY1
MGTRXN1_100_BC41	BC41	U2_MGTTX1_110_N	AY2	MGTTXN1_110_AY2
MGTRXP2_100_BB40	BB40	U2_MGTTX2_110_P	AW3	MGTTXP2_110_AW3
MGTRXN2_100_BB39	BB39	U2_MGTTX2_110_N	AW4	MGTTXN2_110_AW4
MGTRXP3_100_BA42	BA42	U2_MGTTX3_110_P	AV1	MGTTXP3_110_AV1
MGTRXN3_100_BA41	BA41	U2_MGTTX3_110_N	AV2	MGTTXN3_110_AV2
MGTREFCLK0P_100_BA37	BA37	NC	BA8	MGTREFCLK0P_110_BA8
MGTREFCLK0N_100_BA38	BA38	NC	BA7	MGTREFCLK0N_110_BA7
MGTREFCLK1P_100_AW37	AW37	NC	AW8	MGTREFCLK1P_110_AW8
MGTREFCLK1N_100_AW38	AW38	NC	AW7	MGTREFCLK1N_110_AW7

Table 1-30: **FPGA U1 GTX101 to FPGA U2 GTX111 Connections**

U1 Bank 101			FPGA U2 Bank MGTX111	
Pin Name	**Pin No.**	**Net Name**	**Pin No.**	**Pin Name**
MGTTXP0_101_AU42	AU42	U1_MGTTX0_101_P	AY5	MGTRXP0_111_AY5
MGTTXN0_101_AU41	AU41	U1_MGTTX0_101_N	AY6	MGTRXN0_111_AY6
MGTTXP1_101_AT44	AT44	U1_MGTTX1_101_P	AV5	MGTRXP1_111_AV5
MGTTXN1_101_AT43	AT43	U1_MGTTX1_101_N	AV6	MGTRXN1_111_AV6
MGTTXP2_101_AR42	AR42	U1_MGTTX2_101_P	AT5	MGTRXP2_111_AT5
MGTTXN2_101_AR41	AR41	U1_MGTTX2_101_N	AT6	MGTRXN2_111_AT6
MGTTXP3_101_AP44	AP44	U1_MGTTX3_101_P	AP5	MGTRXP3_111_AP5
MGTTXN3_101_AP43	AP43	U1_MGTTX3_101_N	AP6	MGTRXN3_111_AP6
MGTRXP0_101_AY40	AY40	U2_MGTTX0_111_P	AU3	MGTTXP0_111_AU3
MGTRXN0_101_AY39	AY39	U2_MGTTX0_111_N	AU4	MGTTXN0_111_AU4
MGTRXP1_101_AV40	AV40	U2_MGTTX1_111_P	AT1	MGTTXP1_111_AT1
MGTRXN1_101_AV39	AV39	U2_MGTTX1_111_N	AT2	MGTTXN1_111_AT2
MGTRXP2_101_AT40	AT40	U2_MGTTX2_111_P	AR3	MGTTXP2_111_AR3
MGTRXN2_101_AT39	AT39	U2_MGTTX2_111_N	AR4	MGTTXN2_111_AR4
MGTRXP3_101_AP40	AP40	U2_MGTTX3_111_P	AP1	MGTTXP3_111_AP1
MGTRXN3_101_AP39	AP39	U2_MGTTX3_111_N	AP2	MGTTXN3_111_AP2
MGTREFCLK0P_101_AU37	AU37	U2_MGTREFCLK0_111_C_P	AU8	MGTREFCLK0P_111_AU8
MGTREFCLK0N_101_AU38	AU38	U2_MGTREFCLK0_111_C_N	AU7	MGTREFCLK0N_111_AU7
MGTREFCLK1P_101_AR37	AR37	U2_MGTREFCLK1_111_C_P	AR8	MGTREFCLK1P_111_AR8
MGTREFCLK1N_101_AR38	AR38	U2_MGTREFCLK1_111_C_N	AR7	MGTREFCLK1N_111_AR7

Table 1-31: **FPGA U1 GTX102 to FPGA U2 GTX112 Connections**

U1 Bank 102			FPGA U2 Bank MGTX112	
Pin Name	**Pin No.**	**Net Name**	**Pin No.**	**Pin Name**
MGTTXP0_102_AN42	AN42	U1_MGTTX0_102_P	AL7	MGTRXP0_112_AL7
MGTTXN0_102_AN41	AN41	U1_MGTTX0_102_N	AL8	MGTRXN0_112_AL8
MGTTXP1_102_AM44	AM44	U1_MGTTX1_102_P	AM5	MGTRXP1_112_AM5
MGTTXN1_102_AM43	AM43	U1_MGTTX1_102_N	AM6	MGTRXN1_112_AM6
MGTTXP2_102_AL42	AL42	U1_MGTTX2_102_P	AJ7	MGTRXP2_112_AJ7
MGTTXN2_102_AL41	AL41	U1_MGTTX2_102_N	AJ8	MGTRXN2_112_AJ8
MGTTXP3_102_AK44	AK44	U1_MGTTX3_102_P	AK5	MGTRXP3_112_AK5
MGTTXN3_102_AK43	AK43	U1_MGTTX3_102_N	AK6	MGTRXN3_112_AK6
MGTRXP0_102_AL38	AL38	U2_MGTTX0_112_P	AN3	MGTTXP0_112_AN3
MGTRXN0_102_AL37	AL37	U2_MGTTX0_112_N	AN4	MGTTXN0_112_AN4
MGTRXP1_102_AM40	AM40	U2_MGTTX1_112_P	AM1	MGTTXP1_112_AM1
MGTRXN1_102_AM39	AM39	U2_MGTTX1_112_N	AM2	MGTTXN1_112_AM2
MGTRXP2_102_AJ38	AJ38	U2_MGTTX2_112_P	AL3	MGTTXP2_112_AL3
MGTRXN2_102_AJ37	AJ37	U2_MGTTX2_112_N	AL4	MGTTXN2_112_AL4
MGTRXP3_102_AK40	AK40	U2_MGTTX3_112_P	AK1	MGTTXP3_112_AK1
MGTRXN3_102_AK39	AK39	U2_MGTTX3_112_N	AK2	MGTTXN3_112_AK2
MGTREFCLK0P_102_AN37	AN37	NC	AN8	MGTREFCLK0P_112_AN8
MGTREFCLK0N_102_AN38	AN38	NC	AN7	MGTREFCLK0N_112_AN7
MGTREFCLK1P_102_AH35	AH35	NC	AH10	MGTREFCLK1P_112_AH10
MGTREFCLK1N_102_AH36	AH36	NC	AH9	MGTREFCLK1N_112_AH9

Table 1-32: **FPGA U1 GTX103 to FPGA U2 GTX113 Connections**

U1 Bank 103			FPGA U2 Bank MGTX113	
Pin Name	Pin No.	Net Name	Pin No.	Pin Name
MGTTXP0_103_AJ42	AJ42	U1_MGTTX0_103_P	AH5	MGTRXP0_113_AH5
MGTTXN0_103_AJ41	AJ41	U1_MGTTX0_103_N	AH6	MGTRXN0_113_AH6
MGTTXP1_103_AH44	AH44	U1_MGTTX1_103_P	AG7	MGTRXP1_113_AG7
MGTTXN1_103_AH43	AH43	U1_MGTTX1_103_N	AG8	MGTRXN1_113_AG8
MGTTXP2_103_AG42	AG42	U1_MGTTX2_103_P	AF5	MGTRXP2_113_AF5
MGTTXN2_103_AG41	AG41	U1_MGTTX2_103_N	AF6	MGTRXN2_113_AF6
MGTTXP3_103_AF44	AF44	U1_MGTTX3_103_P	AE7	MGTRXP3_113_AE7
MGTTXN3_103_AF43	AF43	U1_MGTTX3_103_N	AE8	MGTRXN3_113_AE8
MGTRXP0_103_AH40	AH40	U2_MGTTX0_113_P	AJ3	MGTTXP0_113_AJ3
MGTRXN0_103_AH39	AH39	U2_MGTTX0_113_N	AJ4	MGTTXN0_113_AJ4
MGTRXP1_103_AG38	AG38	U2_MGTTX1_113_P	AH1	MGTTXP1_113_AH1
MGTRXN1_103_AG37	AG37	U2_MGTTX1_113_N	AH2	MGTTXN1_113_AH2
MGTRXP2_103_AF40	AF40	U2_MGTTX2_113_P	AG3	MGTTXP2_113_AG3
MGTRXN2_103_AF39	AF39	U2_MGTTX2_113_N	AG4	MGTTXN2_113_AG4
MGTRXP3_103_AE38	AE38	U2_MGTTX3_113_P	AF1	MGTTXP3_113_AF1
MGTRXN3_103_AE37	AE37	U2_MGTTX3_113_N	AF2	MGTTXN3_113_AF2
MGTREFCLK0P_103_AF35	AF35	NC	AF10	MGTREFCLK0P_113_AF10
MGTREFCLK0N_103_AF36	AF36	NC	AF9	MGTREFCLK0N_113_AF9
MGTREFCLK1P_103_AD35	AD35	NC	AD10	MGTREFCLK1P_113_AD10
MGTREFCLK1N_103_AD36	AD36	NC	AD9	MGTREFCLK1N_113_AD9

Table 1-33: **FPGA U1 GTX104 to FPGA U2 GTX114 Connections**

U1 Bank 104			FPGA U2 Bank MGTX114	
Pin Name	**Pin No.**	**Net Name**	**Pin No.**	**Pin Name**
MGTTXP0_104_AE42	AE42	U1_MGTTX0_104_P	AD5	MGTRXP0_114_AD5
MGTTXN0_104_AE41	AE41	U1_MGTTX0_104_N	AD6	MGTRXN0_114_AD6
MGTTXP1_104_AD44	AD44	U1_MGTTX1_104_P	AC7	MGTRXP1_114_AC7
MGTTXN1_104_AD43	AD43	U1_MGTTX1_104_N	AC8	MGTRXN1_114_AC8
MGTTXP2_104_AC42	AC42	U1_MGTTX2_104_P	AB5	MGTRXP2_114_AB5
MGTTXN2_104_AC41	AC41	U1_MGTTX2_104_N	AB6	MGTRXN2_114_AB6
MGTTXP3_104_AB44	AB44	U1_MGTTX3_104_P	AA7	MGTRXP3_114_AA7
MGTTXN3_104_AB43	AB43	U1_MGTTX3_104_N	AA8	MGTRXN3_114_AA8
MGTRXP0_104_AD40	AD40	U2_MGTTX0_114_P	AE3	MGTTXP0_114_AE3
MGTRXN0_104_AD39	AD39	U2_MGTTX0_114_N	AE4	MGTTXN0_114_AE4
MGTRXP1_104_AC38	AC38	U2_MGTTX1_114_P	AD1	MGTTXP1_114_AD1
MGTRXN1_104_AC37	AC37	U2_MGTTX1_114_N	AD2	MGTTXN1_114_AD2
MGTRXP2_104_AB40	AB40	U2_MGTTX2_114_P	AC3	MGTTXP2_114_AC3
MGTRXN2_104_AB39	AB39	U2_MGTTX2_114_N	AC4	MGTTXN2_114_AC4
MGTRXP3_104_AA38	AA38	U2_MGTTX3_114_P	AB1	MGTTXP3_114_AB1
MGTRXN3_104_AA37	AA37	U2_MGTTX3_114_N	AB2	MGTTXN3_114_AB2
MGTREFCLK0P_104_AB35	AB35	U2_MGTREFCLK0_114_C_P	AB10	MGTREFCLK0P_114_AB10
MGTREFCLK0N_104_AB36	AB36	U2_MGTREFCLK0_114_C_N	AB9	MGTREFCLK0N_114_AB9
MGTREFCLK1P_104_Y35	Y35	U2_MGTREFCLK1_114_C_P	Y10	MGTREFCLK1P_114_Y10
MGTREFCLK1N_104_Y36	Y36	U2_MGTREFCLK1_114_C_N	Y9	MGTREFCLK1N_114_Y9

Table 1-34: **FPGA U1 GTX105 to FPGA U2 GTX115 Connections**

U1 Bank 105			FPGA U2 Bank MGTX115	
Pin Name	Pin No.	Net Name	Pin No.	Pin Name
MGTTXP0_105_AA42	AA42	U1_MGTTX0_105_P	Y5	MGTRXP0_115_Y5
MGTTXN0_105_AA41	AA41	U1_MGTTX0_105_N	Y6	MGTRXN0_115_Y6
MGTTXP1_105_Y44	Y44	U1_MGTTX1_105_P	W7	MGTRXP1_115_W7
MGTTXN1_105_Y43	Y43	U1_MGTTX1_105_N	W8	MGTRXN1_115_W8
MGTTXP2_105_W42	W42	U1_MGTTX2_105_P	V5	MGTRXP2_115_V5
MGTTXN2_105_W41	W41	U1_MGTTX2_105_N	V6	MGTRXN2_115_V6
MGTTXP3_105_V44	V44	U1_MGTTX3_105_P	U7	MGTRXP3_115_U7
MGTTXN3_105_V43	V43	U1_MGTTX3_105_N	U8	MGTRXN3_115_U8
MGTRXP0_105_Y40	Y40	U2_MGTTX0_115_P	AA3	MGTTXP0_115_AA3
MGTRXN0_105_Y39	Y39	U2_MGTTX0_115_N	AA4	MGTTXN0_115_AA4
MGTRXP1_105_W38	W38	U2_MGTTX1_115_P	Y1	MGTTXP1_115_Y1
MGTRXN1_105_W37	W37	U2_MGTTX1_115_N	Y2	MGTTXN1_115_Y2
MGTRXP2_105_V40	V40	U2_MGTTX2_115_P	W3	MGTTXP2_115_W3
MGTRXN2_105_V39	V39	U2_MGTTX2_115_N	W4	MGTTXN2_115_W4
MGTRXP3_105_U38	U38	U2_MGTTX3_115_P	V1	MGTTXP3_115_V1
MGTRXN3_105_U37	U37	U2_MGTTX3_115_N	V2	MGTTXN3_115_V2
MGTREFCLK0P_105_V35	V35	NC	V10	MGTREFCLK0P_115_V10
MGTREFCLK0N_105_V36	V36	NC	V9	MGTREFCLK0N_115_V9
MGTREFCLK1P_105_T35	T35	NC	T10	MGTREFCLK1P_115_T10
MGTREFCLK1N_105_T36	T36	NC	T9	MGTREFCLK1N_115_T9
MGTAVTTRCAL_105_BC37	BC37	U2_MGTXAVTT	BC8	MGTAVTTRCAL_115_BC8
MGTRREF_105_BC38	BC38	U2_MGTRREF_115	BC7	MGTRREF_115_BC7

80 LVDS Pair Connection FPGA U1 to FPGA U2

There are 80 LVDS pairs wired directly between FPGA U1 and FPGA U2:

- 20 LVDS pairs (U1_B26_LVDS_[19:0]_P/N) wired directly between U1 Bank 26 (schematic page 36) and U2 Bank 26 (schematic page 88)
- 20 LVDS pairs (U1_B34_LVDS_[19:0]_P/N) wired directly between U1 Bank 22 (schematic page 34) and U2 Bank 34 (schematic page 89)
- 20 LVDS pairs (U1_B33_LVDS_[19:0]_P/N) wired directly between U1 Bank 23 (schematic page 34) and U2 Bank 33 (schematic page 89)
- 20 LVDS pairs (U1_B32_LVDS_[19:0]_P/N) wired directly between U1 Bank 24 (schematic page 35) and U2 Bank 32 (schematic page 88)

FPGA U1 and U2 Differential SMA Clock Inputs

Figure 1-2 callout [37, 38, 39, 40]

The ML630 board provides four pairs of differential input SMA connectors. Each pair is connected to a 1-to-2, 3.3V LVPECL ICS85311AMLF clock buffer. The eight clock buffer outputs have net names of CLK_DIFF_<CH#>_Q0 _P/N and CLK_DIFF_<CH#>_Q1 _P/N, where channel number <CH#> ranges from 0 to 3. These signal pairs connect to the four even differential inputs (0, 2, 4 and 6) on each of the two TI SN65LVCP408PAP 8X8 crosspoint switch ICs U57 and U58 (nets …Q0_P/N to U57 and nets …Q1_P/N to U58). Table 1-35 traces the path of the clock pair nets from the source SMA pair to the destination crosspoint switch input pins. Refer to schematic pages 9 and 14 for these circuits.

These four clocks can be routed to various GTX and GTH reference clock inputs through FPGA control over the I^2C interface to the crosspoint switches.

Table 1-35: **Differential SMA Connector to 8x8 Crosspoint Switch Clock Connections**

SMA Conn. Ref. Des.	Input SMA Clock Net Name	ICS85311AMLF Buffer Input Pin No.	ICS85311AMLF Buffer Input Pin No.	3.3V LVPECL Differential Clock Net Name	SN65LVCP408PAP 8x8 Crosspoint Switch Pin No.
J167	CLK_DIFF_0_P	U98.7	U98.1	CLK_DIFF_0_Q0_P	U57.5
J168	CLK_DIFF_0_N	U98.6	U98.2	CLK_DIFF_0_Q0_N	U57.6
			U98.3	CLK_DIFF_0_Q1_P	U58.5
			U98.4	CLK_DIFF_0_Q1_N	U58.6
J169	CLK_DIFF_1_P	U99.7	U99.1	CLK_DIFF_1_Q0_P	U57.11
J170	CLK_DIFF_1_P	U99.6	U99.2	CLK_DIFF_1_Q0_N	U57.12
			U99.3	CLK_DIFF_1_Q1_P	U58.11
			U99.4	CLK_DIFF_1_Q1_N	U58.12
J171	CLK_DIFF_2_P	U96.7	U96.1	CLK_DIFF_2_Q0_P	U57.18
J172	CLK_DIFF_2_P	U96.6	U96.2	CLK_DIFF_2_Q0_N	U57.19
			U96.3	CLK_DIFF_2_Q1_P	U58.18
			U96.4	CLK_DIFF_2_Q1_N	U58.19
J9	CLK_DIFF_3_P	U97.7	U97.1	CLK_DIFF_3_Q0_P	U57.24
J10	CLK_DIFF_3_P	U97.6	U97.2	CLK_DIFF_3_Q0_N	U57.25
			U97.3	CLK_DIFF_3_Q1_P	U58.24
			U97.4	CLK_DIFF_3_Q1_N	U58.25

Differential 2.5V Si570 LVDS Oscillators

Figure 1-2 callout [41]

The ML630 board provides four I2C programmable Silicon Labs Si570 3.3V LVDS 10 MHz-to-810 MHz oscillators. Each oscillator is connected to a 1-to-2 3.3V LVPECL ICS85311AMLF clock buffer (U43, U44, U51 and U52 respectively). The eight clock buffer outputs have net names of SI570_<CH#>_Q0 _P/N and SI570_<CH#>_Q1 _P/N, where channel number <CH#> ranges from 0 to 3. These connect to the four odd inputs (1, 3, 5 and 7) on each of the two TI SN65LVCP408PAP 8X8 crosspoint switch ICs U57 and U58 (nets …Q0_P/N to U57 and nets …Q1_P/N to U58). Table 1-36 traces the path of the clock pair nets from the source Si570 output pin pair to the destination crosspoint switch input pins. Refer to schematic pages 10, 11 and 14 for these circuits.

These four clocks can be routed to various GTX and GTH reference clock inputs through FPGA control over the I2C interface to the crosspoint switches.

Table 1-36: **Differential Si570 to 8x8 Crosspoint Switch Clock Connections**

Si570 Ref. Des.	Output Clock Net Name	ICS85311AMLF Buffer Input Pin No.	ICS85311AMLF Buffer Input Pin No.	3.3V LVPECL Differential Clock Net Name	SN65LVCP408PAP 8x8 Crosspoint Switch Pin No.
U52.4	SI570_0_P	U56.7	U56.1	SI570_0_Q0_P	U57.8
U52.5	SI570_0_N	U56.6	U56.2	SI570_0_Q0_N	U57.9
			U56.3	SI570_0_Q1_P	U58.8
			U56.4	SI570_0_Q1_N	U58.9
U51.4	SI570_1_P	U55.7	U55.1	SI570_1_Q0_P	U57.14
U51.5	SI570_1_P	U55.6	U55.2	SI570_1_Q0_N	U57.15
			U55.3	SI570_1_Q1_P	U58.14
			U55.4	SI570_1_Q1_N	U58.15
U44.4	SI570_2_P	U54.7	U54.1	SI570_2_Q0_P	U57.21
U44.5	SI570_2_P	U54.6	U54.2	SI570_2_Q0_N	U57.22
			U54.3	SI570_2_Q1_P	U58.21
			U54.4	SI570_2_Q1_N	U58.22
U43.4	SI570_3_P	U53.7	U531	SI570_3_Q0_P	U57.27
U43.5	SI570_3_P	U53.6	U53.2	SI570_3_Q0_N	U57.28
			U53.3	SI570_3_Q1_P	U58.27
			U53.4	SI570_3_Q1_N	U58.28

Differential SN65LVCP408PAP 8X8 Crosspoint switches

Figure 1-2 callout [42]

The ML630 board provides two I2C programmable TI SN65LVCP408PAP 8X8 crosspoint switch ICs U57 and U58. Each switch has its four even inputs (0, 2, 4 and 6) connected to the differential SMA clock sources discussed above. Each switch has its four odd inputs (1,

3, 5 and 7) connected to the Si570 clock sources discussed above. Refer to schematic page 14 to view U57 and U58 connectivity. The data sheet for the TI SN65LVCP408PAP can be found at www.ti.com.

FPGA U1 Differential SMA Test Clock Inputs

Figure 1-2 callout [43, 45a]

The ML630 board provides a differential input Test Clock SMA pair for each of the two FPGAs U1 and U2. FPGA U1 SMA pair J124 and J125 drive the inputs of a 3.3V LVDS 1-to-6 ICS854S006AGILF differential clock buffer. The six output pairs created are wired to three dual 2-to-1 ICS85356AGILF differential clock multiplexers. Each multiplexer gets two of the six pairs as inputs. The other two multiplexer input pairs are driven from 8x8 crosspoint switch outputs. Each of the two multiplexer outputs can therefore be sourced from either the Test Clock SMA clock, or a clock from the 8x8 crosspoint switch, which itself has SMA clock and Si570 clock input options as previously detailed.

The multiplexer output pairs drive U1 GTH 106, 107, and 108 and U1 GTX 116, 117 and 118 reference clock inputs.

The FPGA U1 differential SMA test clock input connections and expansion through the 1-to-6 buffer U126 are detailed in Table 1-37. Refer to schematic page 12 for this circuit.

Table 1-37: **FPGA U1 SMA to Buffered Differential Test Clock Connections**

FPGA U1 Test SMA	SMA Differential Clock Net Names	ICS854S006AGILF U126 1-to-6 Buffer Input Pin No.	ICS854S006AGILF U126 1-to-6 Buffer Output Pin No.	ICS854S006AGILF U126 1-to-6 Buffer Output Net Names	ICS8535AGILF 1-to-6 Buffer Input Pin No.
J124	TEST_CLK_1_P	U126.1	U126.5	U1_TEST_REFCLK0_P	U102.1
J125	TEST_CLK_1_N	U126.2	U126.6	U1_TEST_REFCLK0_N	U102.2
			U126.8	U1_TEST_REFCLK1_P	U102.6
			U126.9	U1_TEST_REFCLK1_N	U102.7
			U126.11	U1_TEST_REFCLK2_P	U115.1
			U126.12	U1_TEST_REFCLK2_N	U115.2
			U126.13	U1_TEST_REFCLK3_P	U115.6
			U126.14	U1_TEST_REFCLK3_N	U115.7
			U126.16	U1_TEST_REFCLK4_P	U116.1
			U126.17	U1_TEST_REFCLK4_N	U116.2
			U126.19	U1_TEST_REFCLK5_P	U116.6
			U126.20	U1_TEST_REFCLK5_N	U116.7

FPGA U2 Differential SMA Test Clock Inputs

Figure 1-2 callout [44, 45b]

Similar to the FPGA U1 test clock SMA input, the ML630 board provides a differential input Test Clock SMA pair for FPGA U2. SMA pair J126 and J127 drive the inputs of a 3.3V LVDS 1-to-6 ICS854S006AGILF differential clock buffer. The six output pairs created are wired to three dual 2-to-1 ICS85356AGILF differential clock multiplexers. Each multiplexer gets two of the six pairs as inputs. The other two multiplexer input pairs are driven from 8x8 crosspoint switch outputs. Each of the two multiplexer outputs can therefore be sourced from either the Test Clock SMA clock, or a clock from the 8x8 crosspoint switch, which itself has SMA clock and Si570 clock input options.

The multiplexer output pairs drive U2 GTH 106, 107, and 108 and U2 GTX 116, 117 and 118 reference clock inputs.

The FPGA U2 differential SMA test clock input connections and expansion through the 1-to-6 buffer U127 are detailed in Table 1-38. Refer to schematic page 13 for this circuit.

Table 1-38: **FPGA U2 SMA to Buffered Differential Test Clock Connections**

FPGA U2 Test SMA	SMA Differential Clock Net Names	ICS854S006AGILF U127 1-to-6 Buffer Output Net Names	ICS8535AGILF 1-to-6 Buffer Input Pin No.
J126	TEST_CLK_2_P	U2_TEST_REFCLK0_P	U120.1
J127	TEST_CLK_2_N	U2_TEST_REFCLK0_N	U120.2
		U2_TEST_REFCLK1_P	U120.6
		U2_TEST_REFCLK1_N	U120.7
		U2_TEST_REFCLK2_P	U121.1
		U2_TEST_REFCLK2_N	U121.2
		U2_TEST_REFCLK3_P	U121.6
		U2_TEST_REFCLK3_N	U121.7
		U2_TEST_REFCLK4_P	U122.1
		U2_TEST_REFCLK4_N	U122.2
		U2_TEST_REFCLK5_P	U122.6
		U2_TEST_REFCLK5_N	U122.7

FPGA U1 and U2 Si570 with 1-to-6 Clock Buffer (Two Circuits)

Figure 1-2 callout [46]

FPGA U1 and FPGA U2 each have an I^2C programmable Silicon Labs Si570 3.3V LVDS 10 MHz-to-810 MHz oscillator connected to a 1-to-6 ICS854S006AGILF differential clock buffer (U64–U13 and U65–U18, respectively). The six buffer output pairs are shared between U1 and U2 as shown in Table 1-39 and Table 1-40. Refer to schematic page 15 for U64 and page 69 for U65.

Table 1-39: **Si570 U64 Driven Additional U1 and U2 Differential Clock Sources**

FPGA U1 Si570 U64	Si570 Differential Clock Net Names	U13 ICS854S006AGILF 1-to-6 Buffer Output Net Names	Destination Pin No.
U64.4	SI570_4_P	U1_SI570_4_P	U1.N12
U64.5	SI570_4_N	U1_SI570_4_N	U1.M12
		U2_SI570_4_P	U2.N11
		U2_SI570_4_N	U2.M10
		U1_MGTREFCLK1_101_P	U1.AR37
		U1_MGTREFCLK1_101_N	U1.AR38
		U2_MGTREFCLK1_111_P	U2.AR8
		U2_MGTREFCLK1_111_N	U2.AR7
		U1_P1_TX_REFCLK_P	P1.A1
		U1_P1_TX_REFCLK_P	P1.B1
		U1_P2_TX_REFCLK_P	P2.A1
		U1_P2_TX_REFCLK_P	P2.B1

Table 1-40: **Si570 U65 Driven Additional U1 and U2 Differential Clock Sources**

FPGA U2 Si570 U65	Si570 Differential Clock Net Names	U18 ICS854S006AGILF 1-to-6 Buffer Output Net Names	Destination Pin No.
U65.4	SI570_5_P	U1_SI570_5_P	U1.N11
U65.5	SI570_5_N	U1_SI570_5_N	U1.M10
		U2_SI570_5_P	U2.N12
		U2_SI570_5_N	U2.M12
		U1_MGTREFCLK1_104_P	U1.Y35
		U1_MGTREFCLK1_104_N	U1.Y36
		U2_MGTREFCLK1_114_P	U2.Y10
		U2_MGTREFCLK1_114_N	U2.Y9
		U1_P3_TX_REFCLK_P	P3.A1
		U1_P3_TX_REFCLK_P	P3.B1
		U1_P4_TX_REFCLK_P	P4.A1
		U1_P4_TX_REFCLK_P	P4.B1

FPGA U1 and U2 Example GTH Clock Routing Example

Setup of U1 and U2 GTH Bank 106 and 107 Clocks

FPGA U1 and U2 GTH Banks 106 and 107 can be driven by Si570 oscillator U65 as follows:

Si570 U65 is programmed to the desired frequency. The block diagram in Figure 1-6 shows the example path.

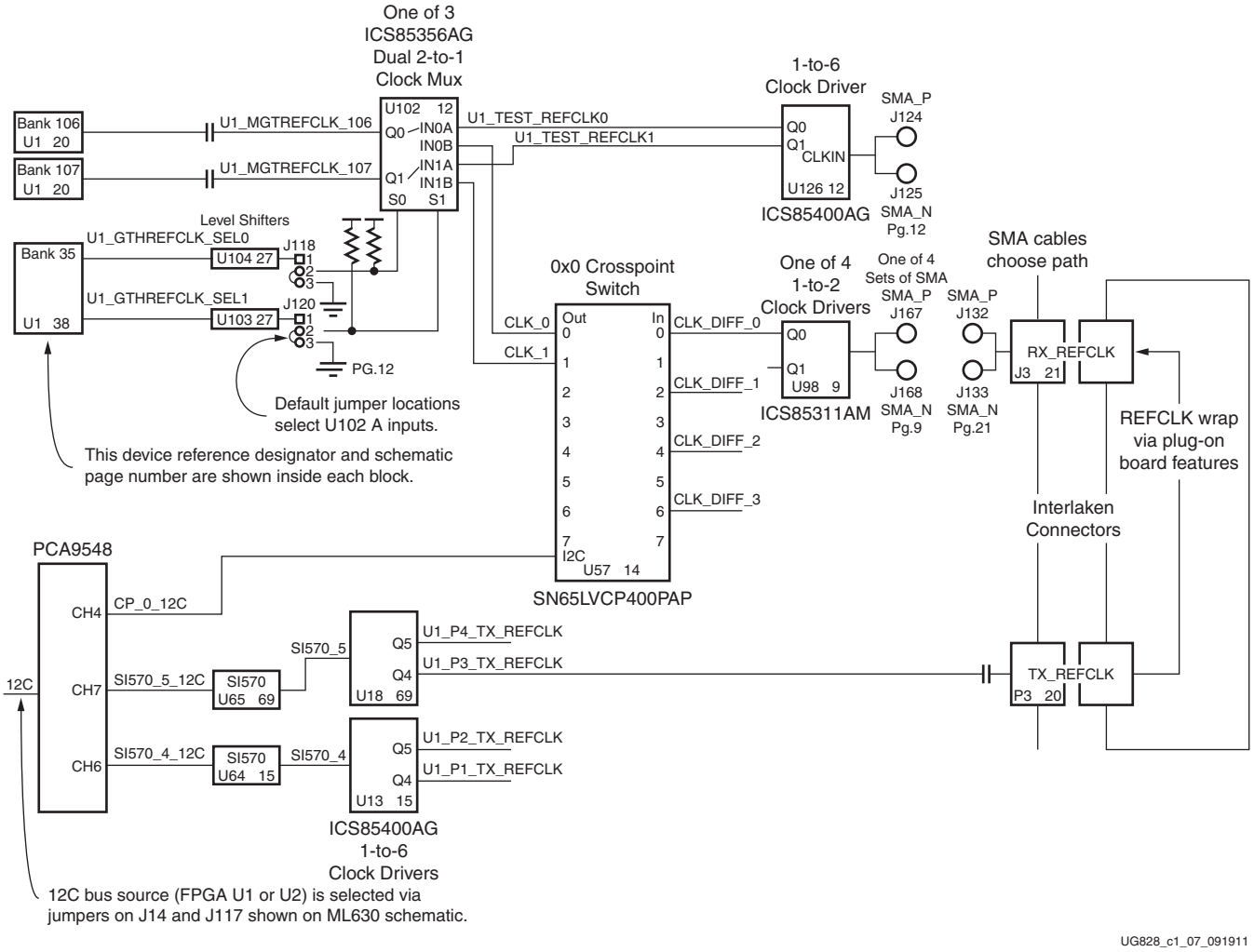

Figure 1-6: **Clock Routing Example Path**

Si570 U65 is connected to 1-to-6 clock driver U18, which in turn drives a TX REFCLK copy to the two Interlaken connectors P3 and P4.

In order to deliver the U65 Si570 frequency to FPGA U1 or U2 GTH 106 or 107, an external add-on card is required. This add-on card wraps the P3 or P4 TX REFCLK signal to J3 (U1) or J4 (U2) RX REFCLK.

J3 and J4 RX REFCLK signals are each wired to a pair of SMA connectors which make their REFCLKs available as a clock source.

This example describes routing J3 RX REFCLK on SMA pair J132/J133 to SMA pair J124/J125. J124/J125 are wired to 1-to-6 clock driver U126. Two outputs of U126 are connected to dual 2-to-1 clock mux U102, which in turn is wired to U1 GTH Banks 106 and 107.

Dual 2-to-1 clock mux U102 has two select pins, one for each independent mux. Each select pin is wired to a 3-pin header. Header J118 pin 2 is pulled up and sources the lower mux (0) select signal U1_SEL0. J118 pin 1 is connected to FPGA U1. Jumping J118 pin 1 to pin 2 allows the lower mux of U102 to be controlled from FPGA U1. J118 pin 3 is wired to ground. Jumping J118 pin 3 to pin 2 forces the lower mux to select its A input. When no jumper is installed on J118 its pin 2 is pulled up which forces the lower mux to select its B input.

Similarly, header J120 sources the upper mux (1) select signal U1_SEL1. J120 pin 1 is connected to FPGA U1. Jumping J120 pin 1 to pin 2 allows the upper mux of U102 to be controlled from FPGA U1. J120 pin 3 is wired to ground. Jumping J120 pin 3 to pin 2 forces the upper mux to select its A input. When no jumper is installed on J120 its pin 2 is pulled up which forces the upper mux to select its B input.

Table 1-41: **ML630 FPGA U1 GTH Reference Clocks**

U1 GTH Bank	Page	U1 Pin No.	Dual 2-to-1 Multiplexer Page 12				Input Clock Pair Net Name (P/N)	Input SMA J124/J125 Page 12 U6 1-to-6 Driver	
			Pin No.	Ref. Des.	Pin No.	Input		Pin No.	Output
106	20	R41	19	U102	1/2	CLK0A	U1_TEST_REFCLK0	5/6	Q0
		R42	18	U102	4/5	CLK0B	CLK0		
107	20	J41	13	U102	6/7	CLK1A	U1_TEST_REFCLK1	8/9	Q1
		J42	12	U102	9/10	CLK1B	CLK1		
108	20	E41	19	U115	1/2	CLK0A	U1_TEST_REFCLK2	11/12	Q2
		E42	18	U115	4/5	CLK0B	CLK2		
116	20	R4	19	U116	1/2	CLK0A	U1_TEST_REFCLK4	16/17	Q4
		R3	18	U116	4/5	CLK0B	CLK4		
117	20	J4	13	U116	6/7	CLK1A	U1_TEST_REFCLK5	19/20	Q5
		J3	12	U116	9/10	CLK1B	CLK5		
118	20	E4	13	U115	6/7	CLK1A	U1_TEST_REFCLK3	13/14	Q3
		E3	12	U115	9/10	CLK1B	CLK3		

Note: Dual 2-to-1 Mux "B" input clk_n clock nets are sourced from 8x8 crosspoint switch U57. All GTH REFCLK inputs are AC coupled.

FPGA U2 Banks 106 and 107 can similarly be driven from the J3 RX REFCLK or the J4 RX REFCLK, as shown in Figure 1-7.

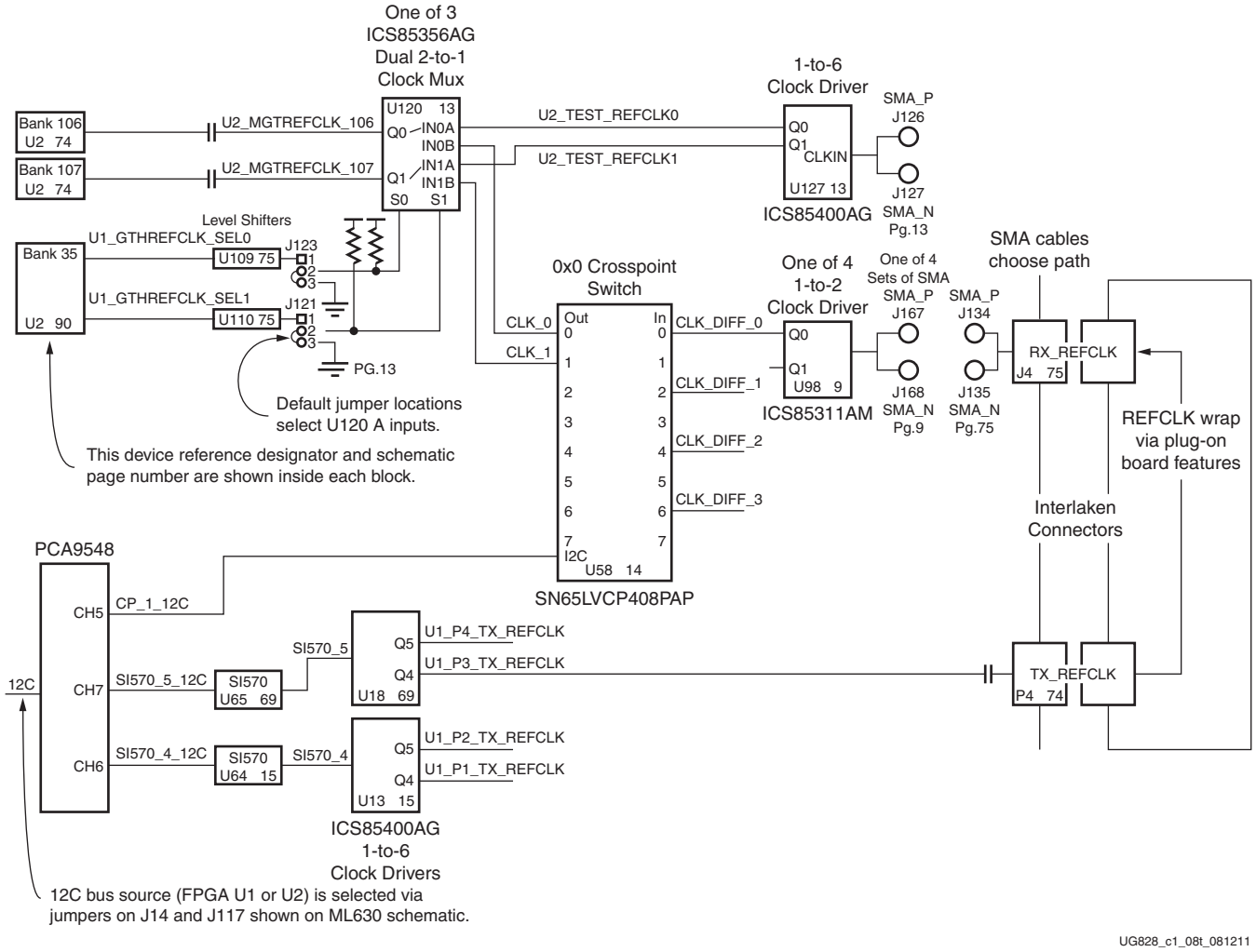

Figure 1-7: **Clock Routing Example Path**

Dual 2-to-1 clock mux U120 has two select pins, one for each independent mux. Each select pin is wired to a 3-pin header. Header J123 pin 2 is pulled up and sources the lower mux (0) select signal U2_SEL0. J123 pin 1 is connected to FPGA U2. Jumping J123 pin 1 to pin 2 allows the lower mux of U120 to be controlled from FPGA U2. J120 pin 3 is wired to ground. Jumping J123 pin 3 to pin 2 forces the lower mux to select its A input. When no jumper is installed on J123 its pin 2 is pulled up which forces the lower mux to select its B input.

Similarly, header J121 sources the upper mux (1) select signal U2_SEL1. J121 pin 1 is connected to FPGA U2. Jumping J121 pin 1 to pin 2 allows the upper mux of U120 to be controlled from FPGA U2. J121 pin 3 is wired to ground. Jumping J121 pin 3 to pin 2 forces the upper mux to select its A input. When no jumper is installed on J121 its pin 2 is pulled up which forces the upper mux to select its B input.

Table 1-42: **ML630 FPGA U2 GTH Reference Clocks**

U2 GTH Bank	Page	U2 Pin No.	Dual 2-to-1 Multiplexer Page 13				Input Clock Pair Net Name (P/N)	Input SMA J126/J127 Page 13 U127 1-to-6 Driver	
			Pin No.	Ref. Des.	Pin No.	Input		Pin No.	Output
106	74	R41	19	U120	1/2	CLK0A	U2_TEST_REFCLK0	5/6	Q0
		R42	18	U120	4/5	CLK0B	CLK8		
107	74	J41	13	U120	6/7	CLK1A	U2_TEST_REFCLK1	8/9	Q1
		J42	12	U120	9/10	CLK1B	CLK9		
108	74	E41	19	U121	1/2	CLK0A	U2_TEST_REFCLK2	11/12	Q2
		E42	18	U121	4/5	CLK0B	CLK10		
116	76	E4	13	U121	6/7	CLK1A	U2_TEST_REFCLK3	13/14	Q3
		E3	12	U121	9/10	CLK1B	CLK11		
117	76	R4	19	U122	1/2	CLK0A	U2_TEST_REFCLK4	16/17	Q4
		R3	18	U122	4/5	CLK0B	CLK12		
118	76	J4	13	U122	6/7	CLK1A	U2_TEST_REFCLK5	19/20	Q5
		J3	12	U122	9/10	CLK1B	CLK13		

Note: Dual 2-to-1 Mux “B” input clk_n clock nets are sourced from 8x8 crosspoint switch U58. All GTH REFCLK inputs are AC coupled.

FMC HPC Connectors

Figure 1-2 callout [48, 49]

The ML630 board features two high pin count (HPC) connectors as defined by the VITA 57.1.1 FPGA Mezzanine Card (FMC) specification. The FMC HPC connector is a 10 x 40 position socket that is fully populated with 400 pins. Refer to Appendix B, VITA 57.1 FMC HPC Connector Pinout for a cross-reference of signal names to pin coordinates.

Note: The FMC HPC J290 and J104 connectors are keyed so that a plug-on FMC card faces away from the ML630 board.

The 10 x 40 pin positions of a FMC HPC connector provide connectivity for up to:

- 160 single-ended or 80 differential pairs of user-defined signals
- 10 MGT differential transmit and 10 MGT differential receive channels
- 2 MGT differential clocks
- 4 additional differential clocks
- 159 ground, 15 power connections

Of the above signal and clock connectivity capability, the ML630 FMC HPC connectors implement the full set:

- 80 differential user-defined pairs:
- 34 LA pairs
- 24 HA pairs
- 22 HB pairs
- 10 MGT differential transmit and receive channels
- 2 MGT differential clocks
- 4 additional MGT differential clocks

Note: The V_{ADJ} voltage for the FMC HPC connectors on the ML630 board is fixed at 2.5V (non-adjustable). The 2.5V rail cannot be turned off. The VITA 57.1 FMC interfaces on the ML630 board are compatible with 2.5V mezzanine cards capable of supporting 2.5V V_{ADJ}.

The FMC HPC connectors on the ML630 board are identified as: FMC1 at J290 and FMC2 at J104. The connections for these connectors are listed in Table 1-43 and Table 1-44. Power supply voltages for the FMC HPC connectors are listed in Table 1-45.

Table 1-43: **FMC1 J290 HPC Connections**

J290 FMC1 HPC Connector		Schematic Net Name	U2 FPGA Pin No.	J290 FMC1 HPC Connector		Schematic Net Name	U2 FPGA Pin No.
Pin Name	Pin No.			Pin Name	Pin No.		
DP1_M2C_P	A2	U2_MGTRX1_100_P	BC42	RES1	B1	NC	
DP1_M2C_N	A3	U2_MGTRX1_100_N	BC41	DP9_M2C_P	B4	U2_MGTRX0_102_P	AL38
DP2_M2C_P	A6	U2_MGTRX2_100_P	BB40	DP9_M2C_N	B5	U2_MGTRX0_102_N	AL37
DP2_M2C_N	A7	U2_MGTRX2_100_N	BB39	DP8_M2C_P	B8	U2_MGTRX0_102_P	AM40
DP3_M2C_P	A10	U2_MGTRX3_100_P	BA41	DP9_M2C_N	B9	U2_MGTRX0_102_N	AM39
DP3_M2C_N	A11	U2_MGTRX3_100_N	BA41	DP8_M2C_P	B12	U2_MGTRX0_102_P	AY40
DP4_M2C_P	A14	U2_MGTRX1_101_P	AV40	DP9_M2C_N	B13	U2_MGTRX0_102_N	AY39
DP4_M2C_N	A15	U2_MGTRX1_101_N	AV39	DP8_M2C_P	B16	U2_MGTRX0_102_P	AT40
DP5_M2C_P	A18	U2_MGTRX3_101_P	AP40	DP9_M2C_N	B17	U2_MGTRX0_102_N	AT39
DP5_M2C_N	A19	U2_MGTRX3_101_N	AP39	GBTCLK1_M2C_P	B20	U2_MGTREFCLK0_101_P	AU37
DP1_C2M_P	A22	U2_MGTTX1_100_P	AY44	GBTCLK1_M2C_N	B21	U2_MGTREFCLK0_101_N	AU39
DP1_C2M_N	A23	U2_MGTTX1_100_N	AY43	DP9_C2M_P	B24	U2_MGTTX0_102_P	AN42
DP2_C2M_P	A26	U2_MGTTX2_100_P	AW42	DP9_C2M_N	B25	U2_MGTTX0_102_N	AN41
DP2_C2M_N	A27	U2_MGTTX2_100_N	AW41	DP8_C2M_P	B28	U2_MGTTX1_102_P	AM44
DP3_C2M_P	A30	U2_MGTTX3_100_P	AV44	DP8_C2M_N	B29	U2_MGTTX1_102_N	AM43
DP3_C2M_P	A31	U2_MGTTX3_100_N	AV43	DP7_C2M_P	B32	U2_MGTTX0_101_P	AU42
DP4_C2M_N	A34	U2_MGTTX1_101_P	AT44	DP7_C2M_N	B33	U2_MGTTX0_101_N	AU41
DP4_C2M_N	A35	U2_MGTTX1_101_N	AT43	DP6_C2M_P	B36	U2_MGTTX2_101_P	AR42
DP5_C2M_N	A38	U2_MGTTX3_101_P	AP44	DP6_C2M_N	B37	U2_MGTTX2_101_N	AR41
DP5_C2M_N	A39	U2_MGTTX3_101_N	AP43	RES0	B40	NC	
				PG_C2M	D1	10K P/U TO VCC3V3	
DP0_C2M_P	C2	U2_MGTTX0_100_P	BB44	GBTCLK0_M2C_P	D4	U2_MGTREFCLK0_100_P	BA37
DP0_C2M_N	C3	U2_MGTTX0_100_N	BB43	GBTCLK0_M2C_N	D5	U2_MGTREFCLK0_100_N	BA38
DP0_M2M_P	C6	U2_MGTRX0_100_P	BD40				
DP0_M2M_N	C7	U2_MGTRX0_100_N	BD39	LA01_P_CC	D8	FMC1_LA01_CC_P	AW13
				LA0_N_CC	D9	FMC1_LA01_CC_N	AY13
LA06_P	C10	FMC1_LA06_P	AP15	LA05_P	D11	FMC1_LA05_P	AP16
LA06_N	C11	FMC1_LA06_N	AP14	LA05_N	D12	FMC1_LA05_N	AR16
LA10_P	C14	FMC1_LA010_P	AU13	LA09_P	D14	FMC1_LA09_P	AT15
LA10_N	C15	FMC1_LA10_N	AV13	LA09_N	D15	FMC1_LA09_N	AU15
LA14_P	C18	FMC1_LA14_P	BA14	LA13_P	D17	FMC1_LA13_P	AU16
LA14_N	C19	FMC1_LA14_N	BA13	LA13_N	D18	FMC1_LA13_N	AV16

Table 1-43: **FMC1 J290 HPC Connections *(Cont'd)***

J290 FMC1 HPC Connector		Schematic Net Name	U2 FPGA Pin No.	J290 FMC1 HPC Connector		Schematic Net Name	U2 FPGA Pin No.
Pin Name	Pin No.			Pin Name	Pin No.		
LA18_P_CC	C22	FMC1_LA18_CC_P	AN19	LA17_P_CC	D20	FMC1_LA17_CC_P	AL19
LA18_N_CC	C23	FMC1_LA18_CC_N	AP19	LA17_N_CC	D21	FMC1_LA17_CC_N	AL18
LA27_P	C26	FMC1_LA27_P	BB17	LA23_P	D23	FMC1_LA23_P	BA17
LA27_N	C27	FMC1_LA27_N	BC16	LA23_N	D24	FMC1_LA23_N	BA16
SCL	C30	U1_SCL (Ref. Schem. PG.10)		LA26_P	D26	FMC1_LA26_P	AY17
SDA	C31	U1_SDA (Ref. Schem. PG.10)		LA26_N	D27	FMC1_LA26_N	AY16
GA0	C34	GA0 (Ref. Schematic PG.5)	J104.C34	TCK	D29	FMC1_TCK_BUF (Ref. Schematic PG.5)	PG5
12P0V_1	C25	U1_VCC12_P		TDI	D30	FMC1_TDI_BUF	J51.1
12P0V_2	C37	U1_VCC12_P		TDO	D31	FMC1_TDO	J51.3
3P3V_1	C39	VCC3V3		3P3VAUX	D32	VCC3V3	
				TMS	D33	FMC1_TMS_BUF (Ref. Schematic PG.5)	
				TRST_L	D34	NC	
				GA1	D35	GA1 (Ref. Schematic PG.10)	J104.D35
				3P3V_2	D36	VCC3V3	
				3P3V_3	D38	VCC3V3	
				3P3V_4	D40	VCC3V3	
HA01_P_CC	E2	FMC1_HA01_CC_P	AW10	PG_M2C	F1	10K P/U TO VCC3V3	
HA01_N_CC	E3	FMC1_HA01_CC_N	AY10	HA00_P_CC	F4	FMC1_HA00_CC_P	BA10
HA05_P	E6	FMC1_HA05_P	AY12	HA00_N_CC	F5	FMC1_HA00_CC_N	BB10
HA05_N	E7	FMC1_HA05_N	BA12	HA04_P	F7	FMC1_HA04_P	BD11
HA09_P	E9	FMC1_HA09_P	BB12	HA04_N	F8	FMC1_HA04_N	BD10
HA09_N	E10	FMC1_HA09_N	BC12	HA08_P	F10	FMC1_HA08_P	AV12
HA13_P	E12	FMC1_HA13_P	AW11	HA08_N	F11	FMC1_HA08_N	AV11
HA13_N	E13	FMC1_HA13_N	AY11	HA12_P	F13	FMC1_HA12_P	AT13
HA16_P	E15	FMC1_HA16_P	AN11	HA12_N	F14	FMC1_HA12_N	AU12
HA16_N	E16	FMC1_HA16_N	AP10	HA15_P	F16	FMC1_HA15_P	AK10
HA20_P	E18	FMC1_HA20_P	BC23	HA15_N	F17	FMC1_HA15_N	AL10
HA20_N	E19	FMC1_HA20_N	BD23	HA19_P	F19	FMC1_HA19_P	AT24
HB03_P	E21	FMC1_HB03_P	AY22	HA19_N	F20	FMC1_HA19_N	AU24

Table 1-43: **FMC1 J290 HPC Connections *(Cont'd)***

J290 FMC1 HPC Connector		Schematic Net Name	U2 FPGA Pin No.	J290 FMC1 HPC Connector		Schematic Net Name	U2 FPGA Pin No.
Pin Name	Pin No.			Pin Name	Pin No.		
HB03_N	E22	FMC1_HB03_N	AY21	HB02_P	F22	FMC1_HB02_P	BB22
HB05_P	E24	FMC1_HB05_P	BC21	HB02_N	F23	FMC1_HB02_N	BC22
HB05_N	E25	FMC1_HB05_N	BD21	HB04_P	F25	FMC1_HB04_P	BB19
HB09_P	E27	FMC1_HB09_P	AW20	HB04_N	F26	FMC1_HB04_N	BC19
HB09_N	E28	FMC1_HB09_N	AW19	HB08_P	F28	FMC1_HB08_P	AY20
HB13_P	E30	FMC1_HB13_P	AT22	HB08_N	F29	FMC1_HB08_N	BA19
HB13_N	E31	FMC1_HB31_N	AU22	HB012_P	F31	FMC1_HB12_P	AL22
HB19_P	E33	FMC1_HB19_P	AU21	HB012_N	F32	FMC1_HB12_N	AM21
HB19_N	E34	FMC1_HB19_N	AV21	HB16_P	F34	FMC1_HB16_P	AK22
HB21_P	E36	FMC1_HB21_P	AN24	HB16_N	F35	FMC1_HB16_N	AK21
HB21_P	E37	FMC1_HB21_N	AP24	HB20_P	F37	FMC1_HB20_P	BA25
VADJ_1	E39	U1_VCCAUX (2.50V)		HB20_N	F38	FMC1_HB20_N	BB25
				VADJ_2	F40	U1_VCCAUX (2.50V)	
				VREF_A_M2C	H1	NC	
CLK1_M2C_P	G2	FMC1_CLK1_M2C_P	AK15	PRSNT_M2C_L	H2	FMC1_PRSNT_M2C_L	BD15
CLK1_M2C_N	G3	FMC1_CLK1_M2C_N	AL14	CLK0_M2C_P	H4	FMC1_CLK0_M2C_P	AL12
LA00_P_CC	G6	FMC1_LA00_CC_P	BC14	CLK0_M2C_N	H5	FMC1_CLK0_M2C_N	AM12
LA00_N_CC	G7	FMC1_LA00_CC_N	BD13	LA02_P	H7	FMC1_LA02_P	AJ15
LA03_P	G9	FMC1_LA03_P	AM16	LA02_N	H8	FMC1_LA02_N	AJ14
LA03_N	G10	FMC1_LA03_N	AN16	LA04_P	H10	FMC1_LA04_P	AJ16
LA08_P	G12	FMC1_LA08_P	AM14	LA04_N	H11	FMC1_LA04_N	AK16
LA08_N	G13	FMC1_LA08_N	AN14	LA04_P	H13	FMC1_LA07_P	AR15
LA12_P	G15	FMC1_LA12_P	AV14	LA07_N	H14	FMC1_LA07_N	AT14
LA12_N	G16	FMC1_LA123_N	AW14	LA11_P	H16	FMC1_LA11_P	AW15
LA16_P	G18	FMC1_LA16_P	BB14	LA11_N	H17	FMC1_LA11_N	AY15
LA16_N	G19	FMC1_LA16_N	BC13	LA15_P	H19	FMC1_LA15_P	BA15
LA20_P	G21	FMC1_LA20_P	AK17	LA15_N	H20	FMC1_LA15_N	BB15
LA20_N	G22	FMC1_LA20_N	AL17	LA19_P	H22	FMC1_LA19_P	AM17
LA22_P	G24	FMC1_LA22_P	AJ18	LA19_N	H23	FMC1_LA19_N	AN17
LA22_N	G25	FMC1_LA22_N	AK18	LA21_P	H25	FMC1_LA21_P	AJ20
LA25_P	G27	FMC1_LA25_P	BC18	LA21_N	H26	FMC1_LA21_N	AJ19
LA25_N	G28	FMC1_LA25_N	BD18	LA24_P	H28	FMC1_LA24_P	AY18

Table 1-43: **FMC1 J290 HPC Connections *(Cont'd)***

J290 FMC1 HPC Connector		Schematic Net Name	U2 FPGA Pin No.	J290 FMC1 HPC Connector		Schematic Net Name	U2 FPGA Pin No.
Pin Name	Pin No.			Pin Name	Pin No.		
LA29_P	G30	FMC1_LA29_P	AV17	LA24_N	H29	FMC1_LA24_N	BA18
LA29_N	G31	FMC1_LA29_N	AW16	LA28_P	H31	FMC1_LA28_P	AV18
LA31_P	G33	FMC1_LA31_P	AT17	LA28_N	H32	FMC1_LA28_N	AW18
LA31_N	G34	FMC1_LA31_N	AU17	LA30_P	H34	FMC1_LA30_P	AT19
LA33_P	G36	FMC1_LA33_P	AR18	LA30_N	H35	FMC1_LA30_N	AT18
LA33_N	G37	FMC1_LA33_N	AR17	LA32_P	H37	FMC1_LA32_P	AN18
VADJ_3	G39	U1_VCCAUX (2.50V)		LA32_N	H38	FMC1_LA32_N	AP18
				VADJ_4	H40	U1_VCCAUX (2.50V)	
				VREF_B_M2C	K1	NC	
CLK3_M2C_P	J2	U2_MGTREFCLK1 _100_P	AW37	CLK2_M2C_P	K4	U2_MGTREFCLK1 _101_P	AR37
CLK3_M2C_N	J3	U2_MGTREFCLK1 _100_P	AW38	CLK2_M2C_N	K5	U2_MGTREFCLK1 _101_P	AR38
HA03_P	J6	FMC1_HA03_P	BB11	HA02_P	K7	FMC1_HA02_N	AU11
HA03_N	J7	FMC1_HA03_N	BC11	HA02_N	K8	FMC1_HA02_N	AU10
HA07_P	J9	FMC1_HA07_P	AR10	HA06_P	K10	FMC1_HA06_N	AR12
HA07_N	J10	FMC1_HA07_N	AT10	HA06_N	K11	FMC1_HA06_N	AT12
HA11_P	J12	FMC1_HA11_P	AM11	HA10_P	K13	FMC1_HA10_N	AN13
HA11_N	J13	FMC1_HA11_N	AM10	HA10_N	K14	FMC1_HA10_N	AN12
HA14_P	J15	FMC1_HA14_P	AK13	HA17_P_CC	K16	FMC1_HA17_CC_P	AR23
HA14_N	J16	FMC1_HA14_N	AL13	HA17_N_CC	K17	FMC1_HA17_CC_N	AT23
HA18_P	J18	FMC1_HA18_P	BC24	HA21_P	K19	FMC1_HA21_P	AV24
HA18_N	J19	FMC1_HA18_N	BD24	HA21_N	K20	FMC1_HA21_N	AW24
HA22_P	J21	FMC1_HA22_P	AP25	HA23_P	K22	FMC1_HA23_P	AL24
HA22_N	J22	FMC1_HA22_N	AR25	HA23_N	K23	FMC1_HA23_N	AM24
HB01_P	J24	FMC1_HB01_P	BD20	HB00_P_CC	K25	FMC1_HB00_CC_P	BA22
HB01_N	J25	FMC1_HB01_N	BD19	HB00_N_CC	K26	FMC1_HB00_CC_N	BB21
HB07_P	J27	FMC1_HB07_P	BA20	HB06_P_CC	K28	FMC1_HB06_CC_P	AV22
HB07_N	J28	FMC1_HB07_N	BB20	HB06_N_CC	K29	FMC1_HB06_CC_N	AW21
HB11_P	J30	FMC1_HB11_P	AU19	HB10_P	K31	FMC1_HB10_P	AT20
HB11_N	J31	FMC1_HB11_N	AV19	HB10_N	K32	FMC1_HB10_N	AU20
HB15_P	J33	FMC1_HB15_P	AN21	HB14_P	K34	FMC1_HB14_P	AM22
HB15_N	J34	FMC1_HB15_N	AP20	HB14_N	K35	FMC1_HB14_N	AN22

Table 1-43: **FMC1 J290 HPC Connections *(Cont'd)***

J290 FMC1 HPC Connector		Schematic Net Name	U2 FPGA Pin No.	J290 FMC1 HPC Connector		Schematic Net Name	U2 FPGA Pin No.
Pin Name	Pin No.			Pin Name	Pin No.		
HB18_P	J36	FMC1_HB18_P	BC24	HB17_P_CC	K37	FMC1_HB17_CC_P	AP21
HB18_N	J37	FMC1_HB18_N	BD24	HB17_N_CC	K38	FMC1_HB17_CC_N	AR20
VIO_B_M2C_1	J39	NC		VIO_B_M2C_2	K40	NC	

Table 1-44: **FMC2 J104 HPC Connections**

J104 FMC2 HPC Connector		Schematic Net Name	U2 FPGA Pin No.	J104 FMC2 HPC Connector		Schematic Net Name	U2 FPGA Pin No.
Pin Name	Pin No.			Pin Name	Pin No.		
DP1_M2C_P	A2	U2_MGTRX1_103_P	AG38	RES1	B1	NC	
DP1_M2C_N	A3	U2_MGTRX1_103_N	AG37	DP9_M2C_P	B4	U2_MGTRX0_105_P	AD40
DP2_M2C_P	A6	U2_MGTRX2_103_P	AF40	DP9_M2C_N	B5	U2_MGTRX0_105_N	AD39
DP2_M2C_N	A7	U2_MGTRX2_103N	AF39	DP8_M2C_P	B8	U2_MGTRX0_105_P	AC38
DP3_M2C_P	A10	U2_MGTRX3_103_P	AE38	DP9_M2C_N	B9	U2_MGTRX0_105_N	AC37
DP3_M2C_N	A11	U2_MGTRX3_103_N	AE37	DP8_M2C_P	B12	U2_MGTRX0_104_P	Y40
DP4_M2C_P	A14	U2_MGTRX1_104_P	W38	DP9_M2C_N	B13	U2_MGTRX0_104_N	Y39
DP4_M2C_N	A15	U2_MGTRX1_104_N	W37	DP8_M2C_P	B16	U2_MGTRX0_104_P	V40
DP5_M2C_P	A18	U2_MGTRX3_104_P	U38	DP9_M2C_N	B17	U2_MGTRX0_104_N	V39
DP5_M2C_N	A19	U2_MGTRX3_104_N	U37	GBTCLK1_M2C_P	B20	U2_MGTREFCLK0_104_P	AB35
DP1_C2M_P	A22	U2_MGTTX1_103_P	AH44	GBTCLK1_M2C_N	B21	U2_MGTREFCLK0_104_N	AB36
DP1_C2M_N	A23	U2_MGTTX1_103_N	AH43	DP9_C2M_P	B24	U2_MGTTX0_105_P	AE42
DP2_C2M_P	A26	U2_MGTTX2_103_P	AG42	DP9_C2M_N	B25	U2_MGTTX0_105_N	AE41
DP2_C2M_N	A27	U2_MGTTX2_103_N	AG41	DP8_C2M_P	B28	U2_MGTTX1_105_P	AD44
DP3_C2M_P	A30	U2_MGTTX3_103_P	AF44	DP8_C2M_N	B29	U2_MGTTX1_105_N	AD43
DP3_C2M_P	A31	U2_MGTTX3_103_N	AF43	DP7_C2M_P	B32	U2_MGTTX0_104_P	AA42
DP4_C2M_N	A34	U2_MGTTX1_104_P	Y44	DP7_C2M_N	B33	U2_MGTTX0_104_N	AA41
DP4_C2M_N	A35	U2_MGTTX1_104_N	Y43	DP6_C2M_P	B36	U2_MGTTX2_104_P	W42
DP5_C2M_N	A38	U2_MGTTX3_104_P	V44	DP6_C2M_N	B37	U2_MGTTX2_104_N	W41
DP5_C2M_N	A39	U2_MGTTX3_104_N	V43	RES0	B40	NC	
				PG_C2M	D1	10K P/U TO VCC3V3	
DP0_C2M_P	C2	U2_MGTTX0_103_P	AJ42	GBTCLK0_M2C_P	D4	U2_MGTREFCLK0_103_P	AF35
DP0_C2M_N	C3	U2_MGTTX0_103_N	AJ4‘	GBTCLK0_M2C_N	D5	U2_MGTREFCLK0_103_N	AF36
DP0_M2M_P	C6	U2_MGTRX0_103_P	AH40	LA01_P_CC	D8	FMC2_LA01_CC_P	AY23
DP0_M2M_N	C7	U2_MGTRX0_103_N	AH39	LA0_N_CC	D9	FMC2_LA01_CC_N	BA23
LA06_P	C10	FMC2_LA06_P	AU26	LA05_P	D11	FMC2_LA05_P	AT25
LA06_N	C11	FMC2_LA06_N	AV26	LA05_N	D12	FMC2_LA05_N	AU25
LA10_P	C14	FMC2_LA010_P	AW25	LA09_P	D14	FMC2_LA09_P	BA24
LA10_N	C15	FMC2_LA10_N	AY25	LA09_N	D15	FMC2_LA09_N	BB24
LA14_P	C18	FMC2_LA14_P	BC24	LA13_P	D17	FMC2_LA13_P	BC23
LA14_N	C19	FMC2_LA14_N	BD24	LA13_N	D18	FMC2_LA13_N	BD23
LA18_P_CC	C22	FMC2_LA18_CC_P	AJ26	LA17_P_CC	D20	FMC2_LA17_CC_P	AN26

Table 1-44: **FMC2 J104 HPC Connections *(Cont'd)***

J104 FMC2 HPC Connector		Schematic Net Name	U2 FPGA Pin No.	J104 FMC2 HPC Connector		Schematic Net Name	U2 FPGA Pin No.
Pin Name	Pin No.			Pin Name	Pin No.		
LA18_N_CC	C23	FMC2_LA18_CC_N	AK27	LA17_N_CC	D21	FMC2_LA17_CC_N	AP26
LA27_P	C26	FMC2_LA27_P	AY28	LA23_P	D23	FMC2_LA23_P	BA27
LA27_N	C27	FMC2_LA27_N	BA29	LA23_N	D24	FMC2_LA23_N	BB27
SCL	C30	U2_SCL (Ref. Schem. PG.10)		LA26_P	D26	FMC2_LA26_P	AY27
SDA	C31	U2_SDA (Ref. Schem. PG.10)		LA26_N	D27	FMC2_LA26_N	BA28
GA0	C34	GA0 (Ref. Schematic PG.5)	J290.C34	TCK	D29	FMC2_TCK_BUF (Ref. Schematic PG.5)	
12P0V_1	C25	U2_VCC12_P		TDI	D30	FMC2_TDI_BUF	J101.1
12P0V_2	C37	U2_VCC12_P		TDO	D31	FMC2_TDO	J101.3
3P3V_1	C39	VCC3V3		3P3VAUX	D32	VCC3V3	
				TMS	D33	FMC2_TMS_BUF (Ref. Schematic PG.5)	
				TRST_L	D34	NC	
				GA1	D35	GA1 (Ref. Schematic PG.10)	J290.D35
				3P3V_2	D36	VCC3V3	
				3P3V_3	D38	VCC3V3	
				3P3V_4	D40	VCC3V3	
HA01_P_CC	E2	FMC2_HA01_CC_P	AV22	PG_M2C	F1	10K P/U TO VCC3V3	
HA01_N_CC	E3	FMC2_HA01_CC_N	AW21	HA00_P_CC	F4	FMC2_HA00_CC_P	BA22
HA05_P	E6	FMC2_HA05_P	AY20	HA00_N_CC	F5	FMC2_HA00_CC_N	BB21
HA05_N	E7	FMC2_HA05_N	BA19	HA04_P	F7	FMC2_HA04_P	AW20
HA09_P	E9	FMC2_HA09_P	AL22	HA04_N	F8	FMC2_HA04_N	AW19
HA09_N	E10	FMC2_HA09_N	AM21	HA08_P	F10	FMC2_HA08_P	AT20
HA13_P	E12	FMC2_HA13_P	BC21	HA08_N	F11	FMC2_HA08_N	AU20
HA13_N	E13	FMC2_HA13_N	BD21	HA12_P	F13	FMC2_HA12_P	BB19
HA16_P	E15	FMC2_HA16_P	BB22	HA12_N	F14	FMC2_HA12_N	BC19
HA16_N	E16	FMC2_HA16_N	BC22	HA15_P	F16	FMC2_HA15_P	BA20
HA20_P	E18	FMC2_HA20_P	AN32	HA15_N	F17	FMC2_HA15_N	BB20
HA20_N	E19	FMC2_HA20_N	AN33	HA19_P	F19	FMC2_HA19_P	BA33
HB03_P	E21	FMC2_HB03_P	BD30	HA19_N	F20	FMC2_HA19_N	BA34
HB03_N	E22	FMC2_HB03_N	BD31	HB02_P	F22	FMC2_HB02_P	BA30

Table 1-44: **FMC2 J104 HPC Connections *(Cont'd)***

J104 FMC2 HPC Connector		Schematic Net Name	U2 FPGA Pin No.	J104 FMC2 HPC Connector		Schematic Net Name	U2 FPGA Pin No.
Pin Name	Pin No.			Pin Name	Pin No.		
HB05_P	E24	FMC2_HB05_P	AW30	HB02_N	F23	FMC2_HB02_N	BB30
HB05_N	E25	FMC2_HB05_N	AY30	HB04_P	F25	FMC2_HB04_P	AY32
HB09_P	E27	FMC2_HB09_P	AU31	HB04_N	F26	FMC2_HB04_N	BA32
HB09_N	E28	FMC2_HB09_N	AV31	HB08_P	F28	FMC2_HB08_P	AU32
HB13_P	E30	FMC2_HB13_P	AR30	HB08_N	F29	FMC2_HB08_N	AV32
HB13_N	E31	FMC2_HB31_N	AT30	HB012_P	F31	FMC2_HB12_P	AP31
HB19_P	E33	FMC2_HB19_P	AM31	HB012_N	F32	FMC2_HB12_N	AR31
HB19_N	E34	FMC2_HB19_N	AN31	HB16_P	F34	FMC2_HB16_P	AL29
HB21_P	E36	FMC2_HB21_P	AL32	HB16_N	F35	FMC2_HB16_N	AM30
HB21_P	E37	FMC2_HB21_N	AM32	HB20_P	F37	FMC2_HB20_P	BC33
VADJ_1	E39	U2_VCCAUX (2.50V)		HB20_N	F38	FMC2_HB20_N	BD33
				VADJ_2	F40	U2_VCCAUX (2.50V)	
				VREF_A_M2C	H1	NC	
CLK1_M2C_P	G2	FMC2_CLK1_M2C_P	AR23	PRSNT_M2C_L	H2	FMC2_PRSNT_M2C_L	BA25
CLK1_M2C_N	G3	FMC2_CLK1_M2C_N	AT23	CLK0_M2C_P	H4	FMC2_CLK0_M2C_P	
LA00_P_CC	G6	FMC2_LA00_CC_P	AV23	CLK0_M2C_N	H5	FMC2_CLK0_M2C_N	
LA00_N_CC	G7	FMC2_LA00_CC_N	AW23	LA02_P	H7	FMC2_LA02_P	AL24
LA03_P	G9	FMC2_LA03_P	AN24	LA02_N	H8	FMC2_LA02_N	AM24
LA03_N	G10	FMC2_LA03_N	AP24	LA04_P	H10	FMC2_LA04_P	AN23
LA08_P	G12	FMC2_LA08_P	AT24	LA04_N	H11	FMC2_LA04_N	AP23
LA08_N	G13	FMC2_LA08_N	AU24	LA04_P	H13	FMC2_LA07_P	AV24
LA12_P	G15	FMC2_LA12_P	AK23	LA07_N	H14	FMC2_LA07_N	AW24
LA12_N	G16	FMC2_LA123_N	AL23	LA11_P	H16	FMC2_LA11_P	AW26
LA16_P	G18	FMC2_LA16_P	BD25	LA11_N	H17	FMC2_LA11_N	AY26
LA16_N	G19	FMC2_LA16_N	BD26	LA15_P	H19	FMC2_LA15_P	BB26
LA20_P	G21	FMC2_LA20_P	BC27	LA15_N	H20	FMC2_LA15_N	BC26
LA20_N	G22	FMC2_LA20_N	BD28	LA19_P	H22	FMC2_LA19_P	AN27
LA22_P	G24	FMC2_LA22_P	AT27	LA19_N	H23	FMC2_LA19_N	AP28
LA22_N	G25	FMC2_LA22_N	AU27	LA21_P	H25	FMC2_LA21_P	BB29
LA25_P	G27	FMC2_LA25_P	AV27	LA21_N	H26	FMC2_LA21_N	BC29
LA25_N	G28	FMC2_LA25_N	AW28	LA24_P	H28	FMC2_LA24_P	AV28
LA29_P	G30	FMC2_LA29_P	AR26	LA24_N	H29	FMC2_LA24_N	AW29

Table 1-44: **FMC2 J104 HPC Connections *(Cont'd)***

J104 FMC2 HPC Connector		Schematic Net Name	U2 FPGA Pin No.	J104 FMC2 HPC Connector		Schematic Net Name	U2 FPGA Pin No.
Pin Name	Pin No.			Pin Name	Pin No.		
LA29_N	G31	FMC2_LA29_N	AR27	LA28_P	H31	FMC2_LA28_P	AR28
LA31_P	G33	FMC2_LA31_P	AM27	LA28_N	H32	FMC2_LA28_N	AT28
LA31_N	G34	FMC2_LA31_N	AN28	LA30_P	H34	FMC2_LA30_P	AL27
LA33_P	G36	FMC2_LA33_P	AJ28	LA30_N	H35	FMC2_LA30_N	AL28
LA33_N	G37	FMC2_LA33_N	AK28	LA32_P	H37	FMC2_LA32_P	AM25
VADJ_3	G39	U2_VCCAUX (2.50V)		LA32_N	H38	FMC2_LA32_N	AM26
				VADJ_4	H40	U2_VCCAUX (2.50V)	
				VREF_B_M2C	K1	NC	
CLK3_M2C_P	J2	U2_MGTREFCLK1 _103_P	AD35	CLK2_M2C_P	K4	U2_MGTREFCLK1 _104_P	Y35
CLK3_M2C_N	J3	U2_MGTREFCLK1 _103_P	AD36	CLK2_M2C_N	K5	U2_MGTREFCLK1 _104_P	Y36
HA03_P	J6	FMC2_HA03_P	AN21	HA02_P	K7	FMC2_HA02_N	AK22
HA03_N	J7	FMC2_HA03_N	AP20	HA02_N	K8	FMC2_HA02_N	AK21
HA07_P	J9	FMC2_HA07_P	AM22	HA06_P	K10	FMC2_HA06_N	AR22
HA07_N	J10	FMC2_HA07_N	AN22	HA06_N	K11	FMC2_HA06_N	AR21
HA11_P	J12	FMC2_HA11_P	AT22	HA10_P	K13	FMC2_HA10_N	AU21
HA11_N	J13	FMC2_HA11_N	AU22	HA10_N	K14	FMC2_HA10_N	AV21
HA14_P	J15	FMC2_HA14_P	AY22	HA17_P_CC	K16	FMC2_HA17_CC_P	AL33
HA14_N	J16	FMC2_HA14_N	AY21	HA17_N_CC	K17	FMC2_HA17_CC_N	AM34
HA18_P	J18	FMC2_HA18_P	AN34	HA21_P	K19	FMC2_HA21_P	AW33
HA18_N	J19	FMC2_HA18_N	AP35	HA21_N	K20	FMC2_HA21_N	AY33
HA22_P	J21	FMC2_HA22_P	BB34	HA23_P	K22	FMC2_HA23_P	BD34
HA22_N	J22	FMC2_HA22_N	BC34	HA23_N	K23	FMC2_HA23_N	BD35
HB01_P	J24	FMC2_HB01_P	BB32	HB00_P_CC	K25	FMC2_HB00_CC_P	BB31
HB01_N	J25	FMC2_HB01_N	BC32	HB00_N_CC	K26	FMC2_HB00_CC_N	BC31
HB07_P	J27	FMC2_HB07_P	AU29	HB06_P_CC	K28	FMC2_HB06_CC_P	AW31
HB07_N	J28	FMC2_HB07_N	AV29	HB06_N_CC	K29	FMC2_HB06_CC_N	AY31
HB11_P	J30	FMC2_HB11_P	AT29	HB10_P	K31	FMC2_HB10_P	AP29
HB11_N	J31	FMC2_HB11_N	AU30	HB10_N	K32	FMC2_HB10_N	AP30
HB15_P	J33	FMC2_HB15_P	AK30	HB14_P	K34	FMC2_HB14_P	AJ31
HB15_N	J34	FMC2_HB15_N	AL30	HB14_N	K35	FMC2_HB14_N	AK31
HB18_P	J36	FMC2_HB18_P	AM29	HB17_P_CC	K37	FMC2_HB17_CC_P	AJ29

Table 1-44: **FMC2 J104 HPC Connections *(Cont'd)***

J104 FMC2 HPC Connector		Schematic Net Name	U2 FPGA Pin No.	J104 FMC2 HPC Connector		Schematic Net Name	U2 FPGA Pin No.
Pin Name	Pin No.			Pin Name	Pin No.		
HB18_N	J37	FMC2_HB18_N	AN29	HB17_N_CC	K38	FMC2_HB17_CC_N	AJ30
VIO_B_M2C_1	J39	NC		VIO_B_M2C_2	K40	NC	

Table 1-45: **Power Supply Voltages for the FMC HPC Connectors**

Voltage Supply	Voltage	Number of Pins	Maximum Amps	Tolerance	Maximum Capacitive Load
V_{ADJ}	Fixed 2.5V	4	4	±5%	1,000 µF
$3P3V_{AUX}$	Fixed 3.3V	1	0.020	±5%	150 µF
3P3V	Fixed 3.3V	4	3	±5%	1,000 µF
12P0V	Fixed 12V	2	1	±5%	1,000 µF

System Monitor

Figure 1-2 callout [1, 2]

The FPGA U1 and U2 System Monitor Bank 0 AVDD and AVSS power pins are tied to filtered FPGA V_{CCAUX} (see schematic pages 17 and 71 for U1 and U2 respectively) to allow internal use of the System Monitor functions. The external System Monitor pins are used for general purpose I/O.

I^{2}C Bus Management

Figure 1-2 callout [47]

The ML630 board implements two I^{2}C buses. FPGA U2 has a local I^{2}C bus for FMC2 HPC connector J104. This bus is 2.50V at the FPGA and is level-shifted to 3.3V via U129. The connections for this bus are shown in Figure 1-8.

The ML630 main I^{2}C bus can be sourced from either FPGA U1 or U2. Each FPGA has a I2C_SCL/SDA_MAIN bus connected to bus selection 3-pin headers. The headers allow selection of either the U1 or U2 I^{2}C bus as the I^{2}C active bus. The header is wired to a level-shifter IC (U128) so the selected low voltage 2.5V FPGA bus is translated to 3.3V for interfacing to the bus residents.

There are three bus targets on the main 3.3V I^{2}C bus:

- FMC1 HPC Connector J290
- I^{2}C EEPROM M24C02 256x8 U59 Address 50 or 54
- I^{2}C 1-to-8 Bus Switch PCS9548 U31 Address 70 or 74

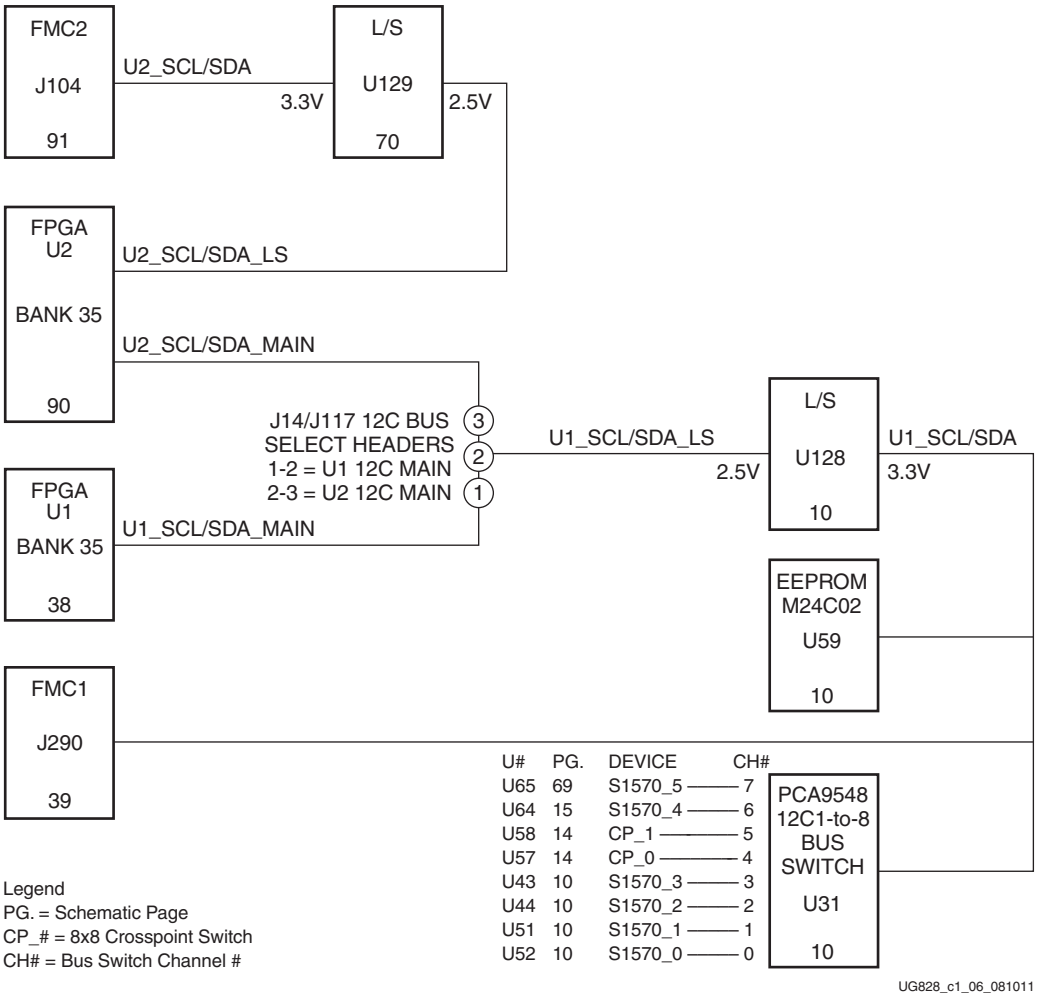

Figure 1-8: **ML630 I²C Bus Connection Diagram**

Notes relevant to Figure 1-8:

- L/S = TI TXS0104 level-shifter device. The number at the bottom of each box is the schematic page number for that component.
- Schematic PG.10 shows 3-pin headers J21, J18 and J100 which may be used to change the I²C address of U59 and U31.
- I²C ADDR = `0x50` or `0x54`.
- I²C ADDR = `0x70` or `0x74`.

The pin connections of the I2C bus components are detailed in Table 1-46 andTable 1-47.

Table 1-46: **ML630 I2C Bus Connections: FPGA U1 and U2 Main I2C Bus**

FPGA Pin No.	I2C Bus Net Name	I2C Bus Headers	I2C Bus Headers	I2C Bus Net Name	L/S U128 2.5V	L/S U128 3.3V	I2C Bus Net Name	PCA9548 U31	M24C02 EEPROM U59	FMC1 HPC J290
U1.G11	U1_SCL_MAIN	J14.1								
U1.H12	U1_SDA_MAIN	J117.1	J14.2	U1_SCL_LS	U128.2	U128.13	U1_SCL	U31.22	U59.6	J290.C30
U2.G11	U2_SCL_MAIN	J14.3	J117.2	U1_SDA_LS	U128.3	U128.12	U1_SDA	U31.23	U59.5	J290.C31
U2.H12	U2_SDA_MAIN	J117.3								

Table 1-47: **FPGA U2 LOCAL I2C BUS**

FPGA Pin No.	I2C Bus Net Name	L/S U129 2.5V	L/S U129 3.3V	I2C Bus Net Name	FMC2 HPC J104
U2.J10	U2_SCL_LS	U129.2	U129.13	U2_SCL	J104.C30
U2.K10	U2_SDA_LS	U129.3	U129.12	U2_SDA	J104.C31

An I2C component on the "back side" of the I2C switch can be accessed by selecting the appropriate channel through the control register of the PCS9548 I2C Bus Switch U31 as shown in Table 1-48.

Table 1-48: **I2C Bus Switch Channel Assignments**

U31 Channel	I2C Component
0	Si570_0 I2C Programmable Clock U52 Address 5D
1	Si570_1 I2C Programmable Clock U51 Address 5D
2	Si570_2 I2C Programmable Clock U44 Address 5D
3	Si570_3 I2C Programmable Clock U43 Address 5D
4	CP_0 8x8 Crosspoint Switch U57 Address Bx
5	CP_1 8x8 Crosspoint Switch U58 Address Bx
6	Si570_3 I2C Programmable Clock U64 Address 5D
7	Si570_3 I2C Programmable Clock U65 Address 5D

Note: Refer to schematic PG.10. U31 I2C ADDR = 0x70 with E2 = 0 and 0x74 with E2=1.

ML630 FCI Airmax Interlaken Plug and Receptacle Level-Shifted Control Signals

FCI Airmax Interlaken Plug (P1, P2, P3 and P4) and Receptacle (J1, J2, J3 and J4) Connectors each support a group of three 3.3V control signals requiring level shifting. The three signals on each of the eight connectors are called CK, DATA and SYNC. The connections are detailed in Table 1-49. The level shifters for P1/J1, P2/J2, P3/J3, and P4/J4 are on are on schematic pages 27, 24, 21, and 75, respectively.

Table 1-49: **ML630 Airmax Connector Level-Shifted Control Signals**

FCI Connector Reference Designator	Net Name (3.3V Side)	TXB0104DR Level Shifter Pin No.	Net Name (2.5V Side)	FPGA U1 Pin No.
P1		*U104*		
P1.E10	U1_AMH1_FC_CK	U104.13	U1_AMH1_FC_LS_CK	U1.A10
P1.H7	U1_AMH1_FC_DATA	U104.12	U1_AMH1_FC_LS_DATA	U1.B11
P1.H9	U1_AMH1_FC_SYNC	U104.11	U1_AMH1_FC_LS_SYNC	U1.A12
J1		*U103*		
J1.E10	U1_AMR1_FC_CK	U103.13	U1_AMR1_FC_LS_CK	U1.A13
J1.H7	U1_AMR1_FC_DATA	U103.12	U1_AMR1_FC_LS_DATA	U1.C11
J1.H9	U1_AMR1_FC_SYNC	U103.11	U1_AMR1_FC_LS_SYNC	U1.C12
P2		*U105*		
P1.E10	U1_AMH2_FC_CK	U105.13	U1_AMH2_FC_LS_CK	U1.B12
P1.H7	U1_AMH2_FC_DATA	U105.12	U1_AMH2_FC_LS_DATA	U1.C13
P1.H9	U1_AMH2_FC_SYNC	U105.11	U1_AMH2_FC_LS_SYNC	U1.A8
J2		*U106*		
J1.E10	U1_AMR2_FC_CK	U106.13	U1_AMR2_FC_LS_CK	U1.B9
J1.H7	U1_AMR2_FC_DATA	U106.12	U1_AMR2_FC_LS_DATA	U1.R12
J1.H9	U1_AMR2_FC_SYNC	U106.11	U1_AMR2_FC_LS_SYNC	U1.R13
P3		*U107*		
P1.E10	U1_AMH3_FC_CK	U107.13	U1_AMH3_FC_LS_CK	U1.D11
P1.H7	U1_AMH3_FC_DATA	U107.12	U1_AMH3_FC_LS_DATA	U1.E12
P1.H9	U1_AMH3_FC_SYNC	U107.11	U1_AMH3_FC_LS_SYNC	U1.A9
J3		*U108*		
J1.E10	U1_AMR3_FC_CK	U108.13	U1_AMR3_FC_LS_CK	U1.B10
J1.H7	U1_AMR3_FC_DATA	U108.12	U2_AMR3_FC_LS_DATA	U1.G10
J1.H9	U1_AMR3_FC_SYNC	U108.11	U2_AMR3_FC_LS_SYNC	U1.H11
P4		*U109*		
P1.E10	U2_AMH4_FC_CK	U109.13	U2_AMH4_FC_LS_CK	U2.A10

Table 1-49: **ML630 Airmax Connector Level-Shifted Control Signals *(Cont'd)***

FCI Connector Reference Designator	Net Name (3.3V Side)	TXB0104DR Level Shifter Pin No.	Net Name (2.5V Side)	FPGA U1 Pin No.
P1.H7	U2_AMH4_FC_DATA	U109.12	U2_AMH4_FC_LS_DATA	U2.B11
P1.H9	U2_AMH4_FC_SYNC	U109.11	U2_AMH4_FC_LS_SYNC	U2.A12
J4		*U110*		
J1.E10	U2_AMR4_FC_CK	U110.13	U2_AMR4_FC_LS_CK	U2.A13
J1.H7	U2_AMR4_FC_DATA	U110.12	U2_AMR4_FC_LS_DATA	U2.C11
J1.H9	U2_AMR4_FC_SYNC	U110.11	U2_AMR4_FC_LS_SYNC	U2.C12

FPGA U1 VGA Debug Connector

Each FPGA supports a 2x5 VGA debug header. The debug header provides three color signals (RGB) along with VSYNC and HSYNC. Each of the color signals is generated by the summation of four FPGA pin outputs driven through stepped resistor values. To see the implementation for FPGA U1 debug connector J16, refer to ML630 schematic pages 35 and 40, and Table 1-50.

Table 1-50: **FPGA U1 VGA Debug J16**

FPGA U1 Pin No.	Net Name	Scaling Resistor	Net Name	J16 Debug Connector Pin No.
E33	U1_VGA_VSYNC			2
F33	U1_VGA_HSYNC			4
N32	U1_VGA_B_0	R596	U1_BLUE	6
P31	U1_VGA_B_1	R625		
F35	U1_VGA_B_2	R615		
G35	U1_VGA_B_3	R606		
L35	U1_VGA_G_0	R597	U1_GREEN	8
M35	U1_VGA_G_1	R626		
N34	U1_VGA_G_2	R616		
N33	U1_VGA_G_3	R609		
D34	U1_VGA_R_0	R598	U1_RED	10
D33	U1_VGA_R_1	R627		
B34	U1_VGA_R_2	R617		
C34	U1_VGA_R_3	R610		

FPGA U2 VGA Debug Connector

Each FPGA supports a 2x5 VGA debug header. The debug header provides three color signals (RGB) along with VSYNC and HSYNC. Each of the color signals is generated by the summation of four FPGA pin outputs driven through stepped resistor values. To see the implementation for FPGA U2 debug connector J110, refer to ML630 schematic pages 87 and 92, and Table 1-51.

Table 1-51: **FPGA U2 VGA Debug J16**

FPGA U2 Pin No.	Net Name	Scaling Resistor	Net Name	J110 Debug Connector Pin No.
E33	U2_VGA_VSYNC			2
F33	U2_VGA_HSYNC			4
N32	U2_VGA_B_0	R596	U2_BLUE	6
P31	U2_VGA_B_1	R625		
F35	U2_VGA_B_2	R615		
G35	U2_VGA_B_3	R606		
L35	U2_VGA_G_0	R597	U2_GREEN	8
M35	U2_VGA_G_1	R626		
N34	U2_VGA_G_2	R616		
N33	U2_VGA_G_3	R609		
D34	U2_VGA_R_0	R598	U2_RED	10
D33	U2_VGA_R_1	R627		
B34	U2_VGA_R_2	R617		
C34	U2_VGA_R_3	R610		

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Appendix A

Default Jumper Positions

Table A-1 shows the 15 standard (black) shunts that must be installed on the board for proper operation. Refer to PCB Assembly Drawing 0431631 for the default placement of all on-board jumpers and their respective connectors as they are located on the board.

Table A-1: **ML630 Default Jumper Positions**

Shunts on Headers	Description	Schematic Page
J65-1 to J65-2	Enable System ACE Red Error LED	5
J14-1 to J14-2	Set U1 SCL as IIC Bus Master	10
J117-1 to J117-2	Set U1 SDA as IIC Bus Master	10
J21-2 to J21-3	ML630 GA0 strap to 0	10
J18-2 to J18-3	ML630 GA1 strap to 0	10
J100-2 to J100-3	Set EEPROM address E2 = 1	10
J118-1 to J118-2	U1_MGTREFCLK_106, 108, 116 J118 U1_SEL0 SELECT: 1–2 = U57 MUX CLK_0, 2, 4 2–3 = SMA J124/J125	12
J120-1 to J120-2	U1_MGTREFCLK_107, 117, 118 J120 U1_SEL1 SELECT: 1–2 = U57 MUX CLK_1, 5, 3 2–3 = SMA J124/J125	12
J123-1 to J123-2	U2_MGTREFCLK_106, 108, 116 J123 U2_SEL0 SELECT: 1–2 = U58 MUX CLK_8, 12, 10 2–3 = SMA J126/J127	13
J121-1 to J121-2	U2_MGTREFCLK_107, 117, 118 J121 U2_SEL1 SELECT: 1–2 = U58 MUX CLK_9, 13, 11 2–3 = SMA J126/J127	13
J136-2 to J136-3	Enable FPGA U1 in JTAG chain	32
J51-1 to J51-2	Bypass FMC1 connector JTAG chain	40
J22-2 to J22-3	Enable ON/OFF switch to turn on UCD9240 controllers	53

Table A-1: **ML630 Default Jumper Positions *(Cont'd)***

Shunts on Headers	Description	Schematic Page
J137-2 to J137-3	Enable FPGA U2 in JTAG chain	84
J101-1 to J101-2	Bypass FMC2 JTAG chain	92

Appendix B

VITA 57.1 FMC HPC Connector Pinout

Figure B-1 provides a cross-reference of signal names to pin coordinates for the VITA 57.1 FMC HPC connector.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

UG828_aB_01_080411

Figure B-1: **FMC Connector Pinout**

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Appendix C

ML630 Master UCF Listing for U1

The ML630 master user constraints file (UCF) template provides for designs targeting the ML630 board. Net names in the constraints listed below correlate with net names on the ML630 board schematic. Users must identify the appropriate pins and replace the net names below with net names in the user RTL. See the Constraints Guide for more information.

```
##############################################################
##
##  ML630 FPGA U1 PIN LOCS: INITIAL RELEASE
##
##  FPGA = HX565T-2FFG1924
##
##############################################################

##
## GLOBAL CLOCK INPUTS (LVDS):
## ALL SI570 @I2C 0x5D, STARTUP FREQUENCY = 156.25MHz
##
NET  U1_LVDS_OSC_P              LOC = J33 ; # 200MHz Bank 25
NET  U1_LVDS_OSC_N              LOC = H33 ; # 200MHz Bank 25
NET  U1_SI570_5_P               LOC =  N11; # 156.25MHz Bank  35
NET  U1_SI570_5_N               LOC =  M10; # 156.25MHz Bank  35
NET  U1_SI570_4_P               LOC =  N12; # 156.25MHz Bank  35
NET  U1_SI570_4_N               LOC =  M12; # 156.25MHz Bank  35

##
## GTH REFCLK MUX FPGA CONTROLS:
##
NET  U1_GTHREFCLK_LS_SEL0       LOC =  K10; # Bank  35 - IO_L11P_SRCC_35
NET  U1_GTHREFCLK_LS_SEL1       LOC =  J10; # Bank  35 - IO_L11N_SRCC_35

##
## FPGA I2C INTERFACE
##
NET  U1_SCL_MAIN                LOC =  H12; # Bank  35 - IO_L17P_35
NET  U1_SDA_MAIN                LOC =  G11; # Bank  35 - IO_L17N_35

##
## USER LEDS:
##
NET  U1_USER_LED8               LOC =  A34; # Bank  25 - IO_L0P_25
NET  U1_USER_LED7               LOC =  A35; # Bank  25 - IO_L0N_25
NET  U1_USER_LED6               LOC =  B35; # Bank  25 - IO_L1P_25
NET  U1_USER_LED5               LOC =  B36; # Bank  25 - IO_L1N_25
NET  U1_USER_LED4               LOC =  B37; # Bank  25 - IO_L2P_SM8P_25
NET  U1_USER_LED3               LOC =  A37; # Bank  25 - IO_L2N_SM8N_25
```

```
NET  U1_USER_LED2               LOC =  L33; # Bank  25 - IO_L3P_SM9P_25
NET  U1_USER_LED1               LOC =  K33; # Bank  25 - IO_L3N_SM9N_25

##
## USER PUSHBUTTON SWITCHES:
##
NET  U1_USER_PB4                LOC =  N23; # Bank  28 - IO_L18P_28
NET  U1_USER_PB3                LOC =  N24; # Bank  28 - IO_L18N_28
NET  U1_USER_PB2                LOC =  J26; # Bank  28 - IO_L19P_28
NET  U1_USER_PB1                LOC =  H26; # Bank  28 - IO_L19N_28

##
## SLIDE SWITCH (8 POSITION):
##
NET  U1_USER_SW8                LOC =  F20; # Bank  38 - IO_L16P_38
NET  U1_USER_SW7                LOC =  E20; # Bank  38 - IO_L16N_38
NET  U1_USER_SW6                LOC =  H21; # Bank  38 - IO_L17P_38
NET  U1_USER_SW5                LOC =  G20; # Bank  38 - IO_L17N_38
NET  U1_USER_SW4                LOC =  R21; # Bank  38 - IO_L18P_38
NET  U1_USER_SW3                LOC =  P21; # Bank  38 - IO_L18N_38
NET  U1_USER_SW2                LOC =  K21; # Bank  38 - IO_L19P_38
NET  U1_USER_SW1                LOC =  J20; # Bank  38 - IO_L19N_38

##
## USER IO:
##
NET  U1_USER_IO_6               LOC =  P34; # Bank  25 - IO_L4P_25
NET  U1_USER_IO_5               LOC =  P35; # Bank  25 - IO_L4N_VREF_25
NET  U1_USER_IO_4               LOC =  E35; # Bank  25 - IO_L5P_SM10P_25
NET  U1_USER_IO_3               LOC =  D35; # Bank  25 - IO_L5N_SM10N_25
NET  U1_USER_IO_2               LOC =  K35; # Bank  25 - IO_L6P_SM11P_25
NET  U1_USER_IO_1               LOC =  J35; # Bank  25 - IO_L6N_SM11N_25

##
## CP2103 USB-TO-UART BRIDGE INTERFACE:
##
NET  U1_USB_CTS_I_B             LOC =  P11; # Bank  35 - IO_L12P_SM5P_35
NET  U1_USB_RTS_0_B             LOC =  P10; # Bank  35 - IO_L12N_SM5N_35
NET  U1_USB_RXD_I               LOC =  F10; # Bank  35 - IO_L13P_SM6P_35
NET  U1_USB_TXD_0               LOC =  E10; # Bank  35 - IO_L13N_SM6N_35
NET  U1_USB_GPIO_3              LOC =  E11; # Bank  35 - IO_L14P_35
NET  U1_USB_GPIO_2              LOC =  D10; # Bank  35 - IO_L14N_VREF_35
NET  U1_USB_GPIO_1              LOC =  M11; # Bank  35 - IO_L15P_SM7P_35
NET  U1_USB_GPIO_0              LOC =  L10; # Bank  35 - IO_L15N_SM7N_35

##
## VGA DEBUG HEADER:
##
NET  U1_VGA_R_3                 LOC =  C34; # Bank  25 - IO_L7P_SM12P_25
NET  U1_VGA_R_2                 LOC =  B34; # Bank  25 - IO_L7N_SM12N_25
NET  U1_VGA_R_1                 LOC =  D33; # Bank  25 - IO_L8P_SRCC_25
NET  U1_VGA_R_0                 LOC =  D34; # Bank  25 - IO_L8N_SRCC_25
NET  U1_VGA_G_3                 LOC =  N33; # Bank  25 - IO_L9P_MRCC_25
NET  U1_VGA_G_2                 LOC =  N34; # Bank  25 - IO_L9N_MRCC_25
NET  U1_VGA_G_1                 LOC =  M35; # Bank  25 - IO_L10P_MRCC_25
NET  U1_VGA_G_0                 LOC =  L35; # Bank  25 - IO_L10N_MRCC_25
NET  U1_VGA_B_3                 LOC =  G35; # Bank  25 - IO_L11P_SRCC_25
NET  U1_VGA_B_2                 LOC =  F35; # Bank  25 - IO_L11N_SRCC_25
NET  U1_VGA_B_1                 LOC =  P31; # Bank  25 - IO_L12P_SM13P_25
```

```
NET  U1_VGA_B_0                LOC =  N32; # Bank  25 - IO_L12N_SM13N_25
NET  U1_VGA_HSYNC              LOC =  F33; # Bank  25 - IO_L13P_SM14P_25
NET  U1_VGA_VSYNC              LOC =  E33; # Bank  25 - IO_L13N_SM14N_25

##
## COLUMN DCI:
##
NET  U1_VRN_25                  LOC =  M34; # Bank  25 - IO_L16P_VRN_25
NET  U1_VRP_25                  LOC =  L34; # Bank  25 - IO_L16N_VRP_25
NET  U1_VRN_32                  LOC = AM20; # Bank  32 - IO_L12P_VRN_32
NET  U1_VRP_32                  LOC = AM19; # Bank  32 - IO_L12N_VRP_32

##
## FMC 1:
##
NET  FMC1_PRSNT_M2C_L           LOC = BD15; # Bank  33 - IO_L19P_33

NET  FMC1_CLK1_M2C_P            LOC = AK15; # Bank  33 - IO_L9P_MRCC_33
NET  FMC1_CLK1_M2C_N            LOC = AL14; # Bank  33 - IO_L9N_MRCC_33
NET  FMC1_CLK0_M2C_P            LOC = AL12; # Bank  34 - IO_L9P_MRCC_34
NET  FMC1_CLK0_M2C_N            LOC = AM12; # Bank  34 - IO_L9N_MRCC_34

NET  FMC1_LA33_P                LOC = AR18; # Bank  32 - IO_L2P_32
NET  FMC1_LA33_N                LOC = AR17; # Bank  32 - IO_L2N_32
NET  FMC1_LA32_P                LOC = AN18; # Bank  32 - IO_L1P_32
NET  FMC1_LA32_N                LOC = AP18; # Bank  32 - IO_L1N_32
NET  FMC1_LA31_P                LOC = AT17; # Bank  32 - IO_L5P_32
NET  FMC1_LA31_N                LOC = AU17; # Bank  32 - IO_L5N_32
NET  FMC1_LA30_P                LOC = AT19; # Bank  32 - IO_L7P_32
NET  FMC1_LA30_N                LOC = AT18; # Bank  32 - IO_L7N_32
NET  FMC1_LA29_P                LOC = AV17; # Bank  32 - IO_L4P_32
NET  FMC1_LA29_N                LOC = AW16; # Bank  32 - IO_L4N_VREF_32
NET  FMC1_LA28_P               LOC = AV18; # Bank  32 - IO_L11P_SRCC_32
NET  FMC1_LA28_N               LOC = AW18; # Bank  32 - IO_L11N_SRCC_32
NET  FMC1_LA27_P                LOC = BB17; # Bank  32 - IO_L8P_SRCC_32
NET  FMC1_LA27_N                LOC = BC16; # Bank  32 - IO_L8N_SRCC_32
NET  FMC1_LA26_P                LOC = AY17; # Bank  32 - IO_L13P_32
NET  FMC1_LA26_N                LOC = AY16; # Bank  32 - IO_L13N_32
NET  FMC1_LA25_P                LOC = BC18; # Bank  32 - IO_L14P_32
NET  FMC1_LA25_N               LOC = BD18; # Bank  32 - IO_L14N_VREF_32
NET  FMC1_LA24_P                LOC = AY18; # Bank  32 - IO_L16P_32
NET  FMC1_LA24_N                LOC = BA18; # Bank  32 - IO_L16N_32
NET  FMC1_LA23_P                LOC = BA17; # Bank  32 - IO_L17P_32
NET  FMC1_LA23_N                LOC = BB16; # Bank  32 - IO_L17N_32
NET  FMC1_LA22_P                LOC = AJ18; # Bank  32 - IO_L6P_32
NET  FMC1_LA22_N                LOC = AK18; # Bank  32 - IO_L6N_32
NET  FMC1_LA21_P                LOC = AJ20; # Bank  32 - IO_L15P_32
NET  FMC1_LA21_N                LOC = AJ19; # Bank  32 - IO_L15N_32
NET  FMC1_LA20_P                LOC = AK17; # Bank  32 - IO_L3P_32
NET  FMC1_LA20_N                LOC = AL17; # Bank  32 - IO_L3N_32
NET  FMC1_LA19_P                LOC = AM17; # Bank  32 - IO_L0P_32
NET  FMC1_LA19_N                LOC = AN17; # Bank  32 - IO_L0N_32
NET  FMC1_LA18_CC_P            LOC = AN19; # Bank  32 - IO_L10P_MRCC_32
NET  FMC1_LA18_CC_N            LOC = AP19; # Bank  32 - IO_L10N_MRCC_32
NET  FMC1_LA17_CC_P             LOC = AL19; # Bank  32 - IO_L9P_MRCC_32
NET  FMC1_LA17_CC_N             LOC = AL18; # Bank  32 - IO_L9N_MRCC_32
NET  FMC1_LA16_P                LOC = BB14; # Bank  33 - IO_L13P_33
NET  FMC1_LA16_N                LOC = BC13; # Bank  33 - IO_L13N_33
NET  FMC1_LA15_P                LOC = BA15; # Bank  33 - IO_L16P_33
```

```
NET  FMC1_LA15_N              LOC = BB15; # Bank  33 - IO_L16N_33
NET  FMC1_LA14_P              LOC = BA14; # Bank  33 - IO_L8P_SRCC_33
NET  FMC1_LA14_N              LOC = BA13; # Bank  33 - IO_L8N_SRCC_33
NET  FMC1_LA13_P              LOC = AU16; # Bank  33 - IO_L14P_33
NET  FMC1_LA13_N             LOC = AV16; # Bank  33 - IO_L14N_VREF_33
NET  FMC1_LA12_P              LOC = AV14; # Bank  33 - IO_L2P_33
NET  FMC1_LA12_N              LOC = AW14; # Bank  33 - IO_L2N_33
NET  FMC1_LA11_P              LOC = AW15; # Bank  33 - IO_L17P_33
NET  FMC1_LA11_N              LOC = AY15; # Bank  33 - IO_L17N_33
NET  FMC1_LA10_P              LOC = AU14; # Bank  33 - IO_L5P_33
NET  FMC1_LA10_N              LOC = AV13; # Bank  33 - IO_L5N_33
NET  FMC1_LA09_P              LOC = AT15; # Bank  33 - IO_L7P_33
NET  FMC1_LA09_N              LOC = AU15; # Bank  33 - IO_L7N_33
NET  FMC1_LA08_P              LOC = AM14; # Bank  33 - IO_L15P_33
NET  FMC1_LA08_N              LOC = AN14; # Bank  33 - IO_L15N_33
NET  FMC1_LA07_P              LOC = AR15; # Bank  33 - IO_L0P_33
NET  FMC1_LA07_N              LOC = AT14; # Bank  33 - IO_L0N_33
NET  FMC1_LA06_P              LOC = AP15; # Bank  33 - IO_L1P_33
NET  FMC1_LA06_N              LOC = AP14; # Bank  33 - IO_L1N_33
NET  FMC1_LA05_P              LOC = AP16; # Bank  33 - IO_L4P_33
NET  FMC1_LA05_N              LOC = AR16; # Bank  33 - IO_L4N_VREF_33
NET  FMC1_LA04_P              LOC = AJ16; # Bank  33 - IO_L6P_33
NET  FMC1_LA04_N              LOC = AK16; # Bank  33 - IO_L6N_33
NET  FMC1_LA03_P              LOC = AM16; # Bank  33 - IO_L18P_33
NET  FMC1_LA03_N              LOC = AN16; # Bank  33 - IO_L18N_33
NET  FMC1_LA02_P              LOC = AJ15; # Bank  33 - IO_L3P_33
NET  FMC1_LA02_N              LOC = AJ14; # Bank  33 - IO_L3N_33
NET  FMC1_LA01_CC_P           LOC = AW13; # Bank  33 - IO_L11P_SRCC_33
NET  FMC1_LA01_CC_N           LOC = AY13; # Bank  33 - IO_L11N_SRCC_33
NET  FMC1_LA00_CC_P           LOC = BC14; # Bank  33 - IO_L10P_MRCC_33
NET  FMC1_LA00_CC_N           LOC = BD13; # Bank  33 - IO_L10N_MRCC_33

NET  FMC1_HA23_P              LOC = AL24; # Bank  21 - IO_L15P_21
NET  FMC1_HA23_N              LOC = AM24; # Bank  21 - IO_L15N_21
NET  FMC1_HA22_P              LOC = AP25; # Bank  21 - IO_L12P_VRN_21
NET  FMC1_HA22_N              LOC = AR25; # Bank  21 - IO_L12N_VRP_21
NET  FMC1_HA21_P              LOC = AV24; # Bank  21 - IO_L13P_21
NET  FMC1_HA21_N              LOC = AW24; # Bank  21 - IO_L13N_21
NET  FMC1_HA20_P              LOC = BC23; # Bank  21 - IO_L16P_21
NET  FMC1_HA20_N              LOC = BD23; # Bank  21 - IO_L16N_21
NET  FMC1_HA19_P              LOC = AT24; # Bank  21 - IO_L14P_21
NET  FMC1_HA19_N             LOC = AU24; # Bank  21 - IO_L14N_VREF_21
NET  FMC1_HA18_P              LOC = BC24; # Bank  21 - IO_L17P_21
NET  FMC1_HA18_N              LOC = BD24; # Bank  21 - IO_L17N_21
NET  FMC1_HA17_CC_P           LOC = AR23; # Bank  21 - IO_L9P_MRCC_21
NET  FMC1_HA17_CC_N           LOC = AT23; # Bank  21 - IO_L9N_MRCC_21
NET  FMC1_HA16_P            LOC = AN11; # Bank  34 - IO_L12P_A03_D19_34
NET  FMC1_HA16_N            LOC = AP10; # Bank  34 - IO_L12N_A02_D18_34
NET  FMC1_HA15_P             LOC = AK10; # Bank  34 - IO_L3P_A13_D29_34
NET  FMC1_HA15_N             LOC = AL10; # Bank  34 - IO_L3N_A12_D28_34
NET  FMC1_HA14_P               LOC = AK13; # Bank  34 - IO_L15P_A23_34
NET  FMC1_HA14_N               LOC = AL13; # Bank  34 - IO_L15N_A22_34
NET  FMC1_HA13_P             LOC = AW11; # Bank  34 - IO_L7P_A05_D21_34
NET  FMC1_HA13_N             LOC = AY11; # Bank  34 - IO_L7N_A04_D20_34
NET  FMC1_HA12_P            LOC = AT13; # Bank  34 - IO_L13P_A01_D17_34
NET  FMC1_HA12_N            LOC = AU12; # Bank  34 - IO_L13N_A00_D16_34
NET  FMC1_HA11_P             LOC = AM11; # Bank  34 - IO_L6P_A07_D23_34
NET  FMC1_HA11_N             LOC = AM10; # Bank  34 - IO_L6N_A06_D22_34
NET  FMC1_HA10_P               LOC = AN13; # Bank  34 - IO_L18P_A17_34
```

```
NET  FMC1_HA10_N                LOC = AN12; # Bank  34 - IO_L18N_A16_34
NET  FMC1_HA09_P                LOC = BB12; # Bank  34 - IO_L19P_VRN_34
NET  FMC1_HA09_N                LOC = BC12; # Bank  34 - IO_L19N_VRP_34
NET  FMC1_HA08_P              LOC = AV12; # Bank  34 - IO_L5P_A09_D25_34
NET  FMC1_HA08_N              LOC = AV11; # Bank  34 - IO_L5N_A08_D24_34
NET  FMC1_HA07_P              LOC = AR10; # Bank  34 - IO_L2P_A15_D31_34
NET  FMC1_HA07_N              LOC = AT10; # Bank  34 - IO_L2N_A14_D30_34
NET  FMC1_HA06_P                LOC = AR12; # Bank  34 - IO_L1P_GC_34
NET  FMC1_HA06_N                LOC = AT12; # Bank  34 - IO_L1N_GC_34
NET  FMC1_HA05_P                LOC = AY12; # Bank  34 - IO_L14P_A25_34
NET  FMC1_HA05_N              LOC = BA12; # Bank  34 - IO_L14N_VREF_A24_34
NET  FMC1_HA04_P                LOC = BD11; # Bank  34 - IO_L17P_A19_34
NET  FMC1_HA04_N                LOC = BD10; # Bank  34 - IO_L17N_A18_34
NET  FMC1_HA03_P                LOC = BB11; # Bank  34 - IO_L16P_A21_34
NET  FMC1_HA03_N                LOC = BC11; # Bank  34 - IO_L16N_A20_34
NET  FMC1_HA02_P              LOC = AU11; # Bank  34 - IO_L4P_A11_D27_34
NET  FMC1_HA02_N                LOC = AU10; # Bank  34 -
IO_L4N_VREF_A10_D26_34
NET  FMC1_HA01_CC_P             LOC = AW10; # Bank  34 - IO_L10P_MRCC_34
NET  FMC1_HA01_CC_N             LOC = AY10; # Bank  34 - IO_L10N_MRCC_34
NET  FMC1_HA00_CC_P             LOC = BA10; # Bank  34 - IO_L11P_SRCC_34
NET  FMC1_HA00_CC_N             LOC = BB10; # Bank  34 - IO_L11N_SRCC_34

NET  FMC1_HB21_P                LOC = AN24; # Bank  21 - IO_L18P_21
NET  FMC1_HB21_N                LOC = AP24; # Bank  21 - IO_L18N_21
NET  FMC1_HB20_P                LOC = BA25; # Bank  21 - IO_L19P_21
NET  FMC1_HB20_N                LOC = BB25; # Bank  21 - IO_L19N_21
NET  FMC1_HB19_P                LOC = AU21; # Bank  31 - IO_L14P_31
NET  FMC1_HB19_N              LOC = AV21; # Bank  31 - IO_L14N_VREF_31
NET  FMC1_HB18_P                LOC = AR22; # Bank  31 - IO_L12P_VRN_31
NET  FMC1_HB18_N                LOC = AR21; # Bank  31 - IO_L12N_VRP_31
NET  FMC1_HB17_CC_P             LOC = AP21; # Bank  31 - IO_L9P_MRCC_31
NET  FMC1_HB17_CC_N             LOC = AR20; # Bank  31 - IO_L9N_MRCC_31
NET  FMC1_HB16_P                LOC = AK22; # Bank  31 - IO_L3P_31
NET  FMC1_HB16_N                LOC = AK21; # Bank  31 - IO_L3N_31
NET  FMC1_HB15_P                LOC = AN21; # Bank  31 - IO_L6P_31
NET  FMC1_HB15_N                LOC = AP20; # Bank  31 - IO_L6N_31
NET  FMC1_HB14_P                LOC = AM22; # Bank  31 - IO_L18P_31
NET  FMC1_HB14_N                LOC = AN22; # Bank  31 - IO_L18N_31
NET  FMC1_HB13_P                LOC = AT22; # Bank  31 - IO_L13P_31
NET  FMC1_HB13_N                LOC = AU22; # Bank  31 - IO_L13N_31
NET  FMC1_HB12_P                LOC = AL22; # Bank  31 - IO_L15P_31
NET  FMC1_HB12_N                LOC = AM21; # Bank  31 - IO_L15N_31
NET  FMC1_HB11_P                LOC = AU19; # Bank  31 - IO_L0P_31
NET  FMC1_HB11_N                LOC = AV19; # Bank  31 - IO_L0N_31
NET  FMC1_HB10_P                LOC = AT20; # Bank  31 - IO_L1P_31
NET  FMC1_HB10_N                LOC = AU20; # Bank  31 - IO_L1N_31
NET  FMC1_HB09_P                LOC = AW20; # Bank  31 - IO_L2P_31
NET  FMC1_HB09_N                LOC = AW19; # Bank  31 - IO_L2N_31
NET  FMC1_HB08_P                LOC = AY20; # Bank  31 - IO_L4P_31
NET  FMC1_HB08_N                LOC = BA19; # Bank  31 - IO_L4N_VREF_31
NET  FMC1_HB07_P                LOC = BA20; # Bank  31 - IO_L5P_31
NET  FMC1_HB07_N                LOC = BB20; # Bank  31 - IO_L5N_31
NET  FMC1_HB06_CC_P             LOC = AV22; # Bank  31 - IO_L10P_MRCC_31
NET  FMC1_HB06_CC_N             LOC = AW21; # Bank  31 - IO_L10N_MRCC_31
NET  FMC1_HB05_P                LOC = BC21; # Bank  31 - IO_L17P_31
NET  FMC1_HB05_N                LOC = BD21; # Bank  31 - IO_L17N_31
NET  FMC1_HB04_P                LOC = BB19; # Bank  31 - IO_L7P_31
NET  FMC1_HB04_N                LOC = BC19; # Bank  31 - IO_L7N_31
```

```
NET  FMC1_HB03_P                LOC = AY22; # Bank  31 - IO_L19P_31
NET  FMC1_HB03_N                LOC = AY21; # Bank  31 - IO_L19N_31
NET  FMC1_HB02_P                LOC = BB22; # Bank  31 - IO_L16P_31
NET  FMC1_HB02_N                LOC = BC22; # Bank  31 - IO_L16N_31
NET  FMC1_HB01_P                LOC = BD20; # Bank  31 - IO_L8P_SRCC_31
NET  FMC1_HB01_N                LOC = BD19; # Bank  31 - IO_L8N_SRCC_31
NET  FMC1_HB00_CC_P             LOC = BA22; # Bank  31 - IO_L11P_SRCC_31
NET  FMC1_HB00_CC_N             LOC = BB21; # Bank  31 - IO_L11N_SRCC_31

##
## FPGA TO FPGA LVDS CHANNELS (4 BANKS, 20 PAIR PER BANK):
##
NET  U1_B34_LVDS_00_P           LOC = AM27; # Bank  22 - IO_L0P_22
NET  U1_B34_LVDS_00_N           LOC = AN28; # Bank  22 - IO_L0N_22
NET  U1_B34_LVDS_01_P           LOC = AN27; # Bank  22 - IO_L1P_22
NET  U1_B34_LVDS_01_N           LOC = AP28; # Bank  22 - IO_L1N_22
NET  U1_B34_LVDS_02_P           LOC = AR28; # Bank  22 - IO_L2P_22
NET  U1_B34_LVDS_02_N           LOC = AT28; # Bank  22 - IO_L2N_22
NET  U1_B34_LVDS_03_P           LOC = AJ28; # Bank  22 - IO_L3P_22
NET  U1_B34_LVDS_03_N           LOC = AK28; # Bank  22 - IO_L3N_22
NET  U1_B34_LVDS_04_P           LOC = AV28; # Bank  22 - IO_L4P_22
NET  U1_B34_LVDS_04_N           LOC = AW29; # Bank  22 - IO_L4N_VREF_22
NET  U1_B34_LVDS_05_P           LOC = AR26; # Bank  22 - IO_L5P_22
NET  U1_B34_LVDS_05_N           LOC = AR27; # Bank  22 - IO_L5N_22
NET  U1_B34_LVDS_06_P           LOC = AL27; # Bank  22 - IO_L6P_22
NET  U1_B34_LVDS_06_N           LOC = AL28; # Bank  22 - IO_L6N_22
NET  U1_B34_LVDS_07_P           LOC = AT27; # Bank  22 - IO_L7P_22
NET  U1_B34_LVDS_07_N           LOC = AU27; # Bank  22 - IO_L7N_22
NET  U1_B34_LVDS_08_P           LOC = AY28; # Bank  22 - IO_L8P_SRCC_22
NET  U1_B34_LVDS_08_N           LOC = BA29; # Bank  22 - IO_L8N_SRCC_22
NET  U1_B34_LVDS_09_P           LOC = AJ26; # Bank  22 - IO_L9P_MRCC_22
NET  U1_B34_LVDS_09_N           LOC = AK27; # Bank  22 - IO_L9N_MRCC_22
NET  U1_B34_LVDS_10_P           LOC = AN26; # Bank  22 - IO_L10P_MRCC_22
NET  U1_B34_LVDS_10_N           LOC = AP26; # Bank  22 - IO_L10N_MRCC_22
NET  U1_B34_LVDS_11_P           LOC = AV27; # Bank  22 - IO_L11P_SRCC_22
NET  U1_B34_LVDS_11_N           LOC = AW28; # Bank  22 - IO_L11N_SRCC_22
NET  U1_B34_LVDS_12_P           LOC = AJ25; # Bank  22 - IO_L12P_VRN_22
NET  U1_B34_LVDS_12_N           LOC = AK26; # Bank  22 - IO_L12N_VRP_22
NET  U1_B34_LVDS_13_P           LOC = AY27; # Bank  22 - IO_L13P_22
NET  U1_B34_LVDS_13_N           LOC = BA28; # Bank  22 - IO_L13N_22
NET  U1_B34_LVDS_14_P           LOC = BC27; # Bank  22 - IO_L14P_22
NET  U1_B34_LVDS_14_N           LOC = BD28; # Bank  22 - IO_L14N_VREF_22
NET  U1_B34_LVDS_15_P           LOC = AM25; # Bank  22 - IO_L15P_22
NET  U1_B34_LVDS_15_N           LOC = AM26; # Bank  22 - IO_L15N_22
NET  U1_B34_LVDS_16_P           LOC = BA27; # Bank  22 - IO_L16P_22
NET  U1_B34_LVDS_16_N           LOC = BB27; # Bank  22 - IO_L16N_22
NET  U1_B34_LVDS_17_P           LOC = BB29; # Bank  22 - IO_L17P_22
NET  U1_B34_LVDS_17_N           LOC = BC29; # Bank  22 - IO_L17N_22
NET  U1_B34_LVDS_18_P           LOC = AK25; # Bank  22 - IO_L18P_22
NET  U1_B34_LVDS_18_N           LOC = AL25; # Bank  22 - IO_L18N_22
NET  U1_B34_LVDS_19_P           LOC = BC28; # Bank  22 - IO_L19P_22
NET  U1_B34_LVDS_19_N           LOC = BD29; # Bank  22 - IO_L19N_22

NET  U1_B33_LVDS_00_P           LOC = AP31; # Bank  23 - IO_L0P_23
NET  U1_B33_LVDS_00_N           LOC = AR31; # Bank  23 - IO_L0N_23
NET  U1_B33_LVDS_01_P           LOC = AP29; # Bank  23 - IO_L1P_23
NET  U1_B33_LVDS_01_N           LOC = AP30; # Bank  23 - IO_L1N_23
NET  U1_B33_LVDS_02_P           LOC = AU31; # Bank  23 - IO_L2P_23
NET  U1_B33_LVDS_02_N           LOC = AV31; # Bank  23 - IO_L2N_23
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```
NET  U1_B33_LVDS_03_P          LOC = AJ31; # Bank  23 - IO_L3P_23
NET  U1_B33_LVDS_03_N          LOC = AK31; # Bank  23 - IO_L3N_23
NET  U1_B33_LVDS_04_P          LOC = AR30; # Bank  23 - IO_L4P_23
NET  U1_B33_LVDS_04_N          LOC = AT30; # Bank  23 - IO_L4N_VREF_23
NET  U1_B33_LVDS_05_P          LOC = AU32; # Bank  23 - IO_L5P_23
NET  U1_B33_LVDS_05_N          LOC = AV32; # Bank  23 - IO_L5N_23
NET  U1_B33_LVDS_06_P          LOC = AK30; # Bank  23 - IO_L6P_23
NET  U1_B33_LVDS_06_N          LOC = AL30; # Bank  23 - IO_L6N_23
NET  U1_B33_LVDS_07_P          LOC = AT29; # Bank  23 - IO_L7P_23
NET  U1_B33_LVDS_07_N          LOC = AU30; # Bank  23 - IO_L7N_23
NET  U1_B33_LVDS_08_P          LOC = AY32; # Bank  23 - IO_L8P_SRCC_23
NET  U1_B33_LVDS_08_N          LOC = BA32; # Bank  23 - IO_L8N_SRCC_23
NET  U1_B33_LVDS_09_P          LOC = AJ29; # Bank  23 - IO_L9P_MRCC_23
NET  U1_B33_LVDS_09_N          LOC = AJ30; # Bank  23 - IO_L9N_MRCC_23
NET  U1_B33_LVDS_10_P         LOC = BB31; # Bank  23 - IO_L10P_MRCC_23
NET  U1_B33_LVDS_10_N         LOC = BC31; # Bank  23 - IO_L10N_MRCC_23
NET  U1_B33_LVDS_11_P         LOC = AW31; # Bank  23 - IO_L11P_SRCC_23
NET  U1_B33_LVDS_11_N         LOC = AY31; # Bank  23 - IO_L11N_SRCC_23
NET  U1_B33_LVDS_12_P          LOC = AL29; # Bank  23 - IO_L12P_VRN_23
NET  U1_B33_LVDS_12_N          LOC = AM30; # Bank  23 - IO_L12N_VRP_23
NET  U1_B33_LVDS_13_P          LOC = BB32; # Bank  23 - IO_L13P_23
NET  U1_B33_LVDS_13_N          LOC = BC32; # Bank  23 - IO_L13N_23
NET  U1_B33_LVDS_14_P          LOC = AU29; # Bank  23 - IO_L14P_23
NET  U1_B33_LVDS_14_N         LOC = AV29; # Bank  23 - IO_L14N_VREF_23
NET  U1_B33_LVDS_15_P          LOC = AM31; # Bank  23 - IO_L15P_23
NET  U1_B33_LVDS_15_N          LOC = AN31; # Bank  23 - IO_L15N_23
NET  U1_B33_LVDS_16_P          LOC = AW30; # Bank  23 - IO_L16P_23
NET  U1_B33_LVDS_16_N          LOC = AY30; # Bank  23 - IO_L16N_23
NET  U1_B33_LVDS_17_P          LOC = BA30; # Bank  23 - IO_L17P_23
NET  U1_B33_LVDS_17_N          LOC = BB30; # Bank  23 - IO_L17N_23
NET  U1_B33_LVDS_18_P          LOC = AM29; # Bank  23 - IO_L18P_23
NET  U1_B33_LVDS_18_N          LOC = AN29; # Bank  23 - IO_L18N_23
NET  U1_B33_LVDS_19_P          LOC = BD30; # Bank  23 - IO_L19P_23
NET  U1_B33_LVDS_19_N          LOC = BD31; # Bank  23 - IO_L19N_23

NET  U1_B32_LVDS_00_P          LOC = AP33; # Bank  24 - IO_L0P_GC_24
NET  U1_B32_LVDS_00_N          LOC = AP34; # Bank  24 - IO_L0N_GC_24
NET  U1_B32_LVDS_01_P          LOC = AR33; # Bank  24 - IO_L1P_GC_24
NET  U1_B32_LVDS_01_N          LOC = AT33; # Bank  24 - IO_L1N_GC_24
NET  U1_B32_LVDS_02_P          LOC = AR35; # Bank  24 - IO_L2P_D15_24
NET  U1_B32_LVDS_02_N          LOC = AT35; # Bank  24 - IO_L2N_D14_24
NET  U1_B32_LVDS_03_P          LOC = AK35; # Bank  24 - IO_L3P_D13_24
NET  U1_B32_LVDS_03_N          LOC = AL35; # Bank  24 - IO_L3N_D12_24
NET  U1_B32_LVDS_04_P          LOC = AU34; # Bank  24 - IO_L4P_D11_24
NET  U1_B32_LVDS_04_N         LOC = AV34; # Bank  24 - IO_L4N_VREF_D10_24
NET  U1_B32_LVDS_05_P          LOC = AT34; # Bank  24 - IO_L5P_D9_24
NET  U1_B32_LVDS_05_N          LOC = AU35; # Bank  24 - IO_L5N_D8_24
NET  U1_B32_LVDS_06_P          LOC = AL34; # Bank  24 - IO_L6P_D7_24
NET  U1_B32_LVDS_06_N          LOC = AM35; # Bank  24 - IO_L6N_D6_24
NET  U1_B32_LVDS_07_P          LOC = AV33; # Bank  24 - IO_L7P_D5_24
NET  U1_B32_LVDS_07_N          LOC = AW34; # Bank  24 - IO_L7N_D4_24
NET  U1_B32_LVDS_08_P          LOC = AR32; # Bank  24 - IO_L8P_SRCC_24
NET  U1_B32_LVDS_08_N          LOC = AT32; # Bank  24 - IO_L8N_SRCC_24
NET  U1_B32_LVDS_09_P          LOC = AL33; # Bank  24 - IO_L9P_MRCC_24
NET  U1_B32_LVDS_09_N          LOC = AM34; # Bank  24 - IO_L9N_MRCC_24
NET  U1_B32_LVDS_10_P         LOC = AW35; # Bank  24 - IO_L10P_MRCC_24
NET  U1_B32_LVDS_10_N         LOC = AY35; # Bank  24 - IO_L10N_MRCC_24
NET  U1_B32_LVDS_11_P         LOC = BA35; # Bank  24 - IO_L11P_SRCC_24
NET  U1_B32_LVDS_11_N         LOC = BB35; # Bank  24 - IO_L11N_SRCC_24
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NET  U1_B32_LVDS_12_P          LOC = AN34; # Bank  24 - IO_L12P_D3_24
NET  U1_B32_LVDS_12_N         LOC = AP35; # Bank  24 - IO_L12N_D2_FS2_24
NET  U1_B32_LVDS_13_P         LOC = BA33; # Bank  24 - IO_L13P_D1_FS1_24
NET  U1_B32_LVDS_13_N         LOC = BA34; # Bank  24 - IO_L13N_D0_FS0_24
NET  U1_B32_LVDS_14_P          LOC = AW33; # Bank  24 - IO_L14P_FCS_B_24
NET  U1_B32_LVDS_14_N          LOC = AY33; # Bank  24 -
IO_L14N_VREF_FOE_B_MOSI
NET  U1_B32_LVDS_15_P         LOC = AN32; # Bank  24 - IO_L15P_FWE_B_24
NET  U1_B32_LVDS_15_N          LOC = AN33; # Bank  24 - IO_L15N_RS1_24
NET  U1_B32_LVDS_16_P          LOC = BB34; # Bank  24 - IO_L16P_RS0_24
NET  U1_B32_LVDS_16_N         LOC = BC34; # Bank  24 - IO_L16N_CSO_B_24
NET  U1_B32_LVDS_17_P          LOC = BD34; # Bank  24 - IO_L17P_VRN_24
NET  U1_B32_LVDS_17_N          LOC = BD35; # Bank  24 - IO_L17N_VRP_24
NET  U1_B32_LVDS_18_P          LOC = AL32; # Bank  24 - IO_L18P_24
NET  U1_B32_LVDS_18_N          LOC = AM32; # Bank  24 - IO_L18N_24
NET  U1_B32_LVDS_19_P          LOC = BC33; # Bank  24 - IO_L19P_24
NET  U1_B32_LVDS_19_N          LOC = BD33; # Bank  24 - IO_L19N_24

NET  U1_B26_LVDS_00_P          LOC =  B31; # Bank  26 - IO_L0P_26
NET  U1_B26_LVDS_00_N          LOC =  A32; # Bank  26 - IO_L0N_26
NET  U1_B26_LVDS_01_P          LOC =  B30; # Bank  26 - IO_L1P_26
NET  U1_B26_LVDS_01_N          LOC =  A30; # Bank  26 - IO_L1N_26
NET  U1_B26_LVDS_02_P          LOC =  C32; # Bank  26 - IO_L2P_26
NET  U1_B26_LVDS_02_N          LOC =  C33; # Bank  26 - IO_L2N_26
NET  U1_B26_LVDS_03_P          LOC =  M30; # Bank  26 - IO_L3P_26
NET  U1_B26_LVDS_03_N          LOC =  M31; # Bank  26 - IO_L3N_26
NET  U1_B26_LVDS_04_P          LOC =  E30; # Bank  26 - IO_L4P_26
NET  U1_B26_LVDS_04_N          LOC =  D30; # Bank  26 - IO_L4N_VREF_26
NET  U1_B26_LVDS_05_P          LOC =  B32; # Bank  26 - IO_L5P_26
NET  U1_B26_LVDS_05_N          LOC =  A33; # Bank  26 - IO_L5N_26
NET  U1_B26_LVDS_06_P          LOC =  N29; # Bank  26 - IO_L6P_26
NET  U1_B26_LVDS_06_N          LOC =  M29; # Bank  26 - IO_L6N_26
NET  U1_B26_LVDS_07_P          LOC =  D31; # Bank  26 - IO_L7P_26
NET  U1_B26_LVDS_07_N          LOC =  C31; # Bank  26 - IO_L7N_26
NET  U1_B26_LVDS_08_P          LOC =  G31; # Bank  26 - IO_L8P_SRCC_26
NET  U1_B26_LVDS_08_N          LOC =  F32; # Bank  26 - IO_L8N_SRCC_26
NET  U1_B26_LVDS_09_P          LOC =  R28; # Bank  26 - IO_L9P_MRCC_26
NET  U1_B26_LVDS_09_N          LOC =  P29; # Bank  26 - IO_L9N_MRCC_26
NET  U1_B26_LVDS_10_P         LOC =  J31; # Bank  26 - IO_L10P_MRCC_26
NET  U1_B26_LVDS_10_N         LOC =  H32; # Bank  26 - IO_L10N_MRCC_26
NET  U1_B26_LVDS_11_P         LOC =  E31; # Bank  26 - IO_L11P_SRCC_26
NET  U1_B26_LVDS_11_N         LOC =  E32; # Bank  26 - IO_L11N_SRCC_26
NET  U1_B26_LVDS_12_P          LOC =  N31; # Bank  26 - IO_L12P_VRN_26
NET  U1_B26_LVDS_12_N          LOC =  M32; # Bank  26 - IO_L12N_VRP_26
NET  U1_B26_LVDS_13_P          LOC =  G30; # Bank  26 - IO_L13P_26
NET  U1_B26_LVDS_13_N          LOC =  F30; # Bank  26 - IO_L13N_26
NET  U1_B26_LVDS_14_P          LOC =  L30; # Bank  26 - IO_L14P_26
NET  U1_B26_LVDS_14_N         LOC =  K31; # Bank  26 - IO_L14N_VREF_26
NET  U1_B26_LVDS_15_P          LOC =  R30; # Bank  26 - IO_L15P_26
NET  U1_B26_LVDS_15_N          LOC =  P30; # Bank  26 - IO_L15N_26
NET  U1_B26_LVDS_16_P          LOC =  L32; # Bank  26 - IO_L16P_26
NET  U1_B26_LVDS_16_N          LOC =  K32; # Bank  26 - IO_L16N_26
NET  U1_B26_LVDS_17_P          LOC =  H31; # Bank  26 - IO_L17P_26
NET  U1_B26_LVDS_17_N          LOC =  G32; # Bank  26 - IO_L17N_26
NET  U1_B26_LVDS_18_P          LOC =  T29; # Bank  26 - IO_L18P_26
NET  U1_B26_LVDS_18_N          LOC =  T30; # Bank  26 - IO_L18N_26
NET  U1_B26_LVDS_19_P          LOC =  K30; # Bank  26 - IO_L19P_26
NET  U1_B26_LVDS_19_N          LOC =  J30; # Bank  26 - IO_L19N_26
```

```
##
## GTX REFCLKS
##
NET  U1_MGTREFCLK0_101_C_P     LOC = AU37; # Bank 101 - MGTREFCLK0P_101
NET  U1_MGTREFCLK0_101_C_N     LOC = AU38; # Bank 101 - MGTREFCLK0N_101
NET  U1_MGTREFCLK1_101_C_P     LOC = AR37; # Bank 101 - MGTREFCLK1P_101
NET  U1_MGTREFCLK1_101_C_N     LOC = AR38; # Bank 101 - MGTREFCLK1N_101
NET  U1_MGTREFCLK0_104_C_P     LOC = AB35; # Bank 104 - MGTREFCLK0P_104
NET  U1_MGTREFCLK0_104_C_N     LOC = AB36; # Bank 104 - MGTREFCLK0N_104
NET  U1_MGTREFCLK1_104_C_P     LOC =  Y35; # Bank 104 - MGTREFCLK1P_104
NET  U1_MGTREFCLK1_104_C_N     LOC =  Y36; # Bank 104 - MGTREFCLK1N_104
NET  U1_MGTREFCLK1_111_P       LOC =  AR8; # Bank 111 - MGTREFCLK1P_111
NET  U1_MGTREFCLK1_111_N       LOC =  AR7; # Bank 111 - MGTREFCLK1N_111
NET  U1_MGTREFCLK0_111_P       LOC =  AU8; # Bank 111 - MGTREFCLK0P_111
NET  U1_MGTREFCLK0_111_N       LOC =  AU7; # Bank 111 - MGTREFCLK0N_111
NET  U1_MGTREFCLK1_114_P       LOC =  Y10; # Bank 114 - MGTREFCLK1P_114
NET  U1_MGTREFCLK1_114_N       LOC =   Y9; # Bank 114 - MGTREFCLK1N_114
NET  U1_MGTREFCLK0_114_P       LOC = AB10; # Bank 114 - MGTREFCLK0P_114
NET  U1_MGTREFCLK0_114_N       LOC =  AB9; # Bank 114 - MGTREFCLK0N_114

##
## GTH REFCLKS (1 PER QUAD):
##
NET  U1_MGTREFCLK_106_P        LOC =  R41; # Bank 106 - MGTREFCLKP_106
NET  U1_MGTREFCLK_106_N        LOC =  R42; # Bank 106 - MGTREFCLKN_106
NET  U1_MGTREFCLK_107_P        LOC =  J41; # Bank 107 - MGTREFCLKP_107
NET  U1_MGTREFCLK_107_N        LOC =  J42; # Bank 107 - MGTREFCLKN_107
NET  U1_MGTREFCLK_108_P        LOC =  E41; # Bank 108 - MGTREFCLKP_108
NET  U1_MGTREFCLK_108_N        LOC =  E42; # Bank 108 - MGTREFCLKN_108
NET  U1_MGTREFCLK_116_P        LOC =   R4; # Bank 116 - MGTREFCLKP_116
NET  U1_MGTREFCLK_116_N        LOC =   R3; # Bank 116 - MGTREFCLKN_116
NET  U1_MGTREFCLK_117_P        LOC =   J4; # Bank 117 - MGTREFCLKP_117
NET  U1_MGTREFCLK_117_N        LOC =   J3; # Bank 117 - MGTREFCLKN_117
NET  U1_MGTREFCLK_118_P        LOC =   E4; # Bank 118 - MGTREFCLKP_118
NET  U1_MGTREFCLK_118_N        LOC =   E3; # Bank 118 - MGTREFCLKN_118

##
## INTERLOCKEN INTERFACE (AIRMAX CONNECTORS) FLOW CONTROL SIGNALS:
##
NET  U1_AMR1_FC_LS_SYNC        LOC =  C12; # Bank  35 - IO_L0P_35
NET  U1_AMR1_FC_LS_DATA        LOC =  C11; # Bank  35 - IO_L0N_35
NET  U1_AMR1_FC_LS_CK          LOC =  A13; # Bank  35 - IO_L1P_35
NET  U1_AMH1_FC_LS_SYNC        LOC =  A12; # Bank  35 - IO_L1N_35
NET  U1_AMH1_FC_LS_DATA        LOC =  B11; # Bank  35 - IO_L2P_SM0P_35
NET  U1_AMH1_FC_LS_CK          LOC =  A10; # Bank  35 - IO_L2N_SM0N_35

NET  U1_AMR2_FC_LS_SYNC        LOC =  R13; # Bank  35 - IO_L3P_SM1P_35
NET  U1_AMR2_FC_LS_DATA        LOC =  R12; # Bank  35 - IO_L3N_SM1N_35
NET  U1_AMR2_FC_LS_CK          LOC =   B9; # Bank  35 - IO_L4P_35
NET  U1_AMH2_FC_LS_SYNC        LOC =   A8; # Bank  35 - IO_L4N_VREF_35
NET  U1_AMH2_FC_LS_DATA        LOC =  C13; # Bank  35 - IO_L5P_SM2P_35
NET  U1_AMH2_FC_LS_CK          LOC =  B12; # Bank  35 - IO_L5N_SM2N_35

NET  U1_AMR3_FC_LS_SYNC        LOC =  H11; # Bank  35 - IO_L6P_SM3P_35
NET  U1_AMR3_FC_LS_DATA        LOC =  G10; # Bank  35 - IO_L6N_SM3N_35
NET  U1_AMR3_FC_LS_CK          LOC =  B10; # Bank  35 - IO_L7P_SM4P_35
NET  U1_AMH3_FC_LS_SYNC        LOC =   A9; # Bank  35 - IO_L7N_SM4N_35
NET  U1_AMH3_FC_LS_DATA        LOC =  E12; # Bank  35 - IO_L8P_SRCC_35
NET  U1_AMH3_FC_LS_CK          LOC =  D11; # Bank  35 - IO_L8N_SRCC_35
```

```
##
## INTERLOCKEN INTERFACE (AIRMAX CONNECTORS) I/O CONTROL SIGNALS:
##
NET  U1_AMH3_IO7               LOC =  G34; # Bank  25 - IO_L14P_25
NET  U1_AMH3_IO6              LOC =  F34; # Bank  25 - IO_L14N_VREF_25
NET  U1_AMH3_IO5             LOC =  R33; # Bank  25 - IO_L15P_SM15P_25
NET  U1_AMH3_IO4             LOC =  P33; # Bank  25 - IO_L15N_SM15N_25
NET  U1_AMH3_IO3               LOC =  J34; # Bank  25 - IO_L17P_25
NET  U1_AMH3_IO2               LOC =  H34; # Bank  25 - IO_L17N_25
NET  U1_AMH3_IO1               LOC =  R31; # Bank  25 - IO_L18P_GC_25
NET  U1_AMH3_IO0               LOC =  R32; # Bank  25 - IO_L18N_GC_25

NET  U1_AMH2_IO7               LOC = AU26; # Bank  21 - IO_L0P_21
NET  U1_AMH2_IO6               LOC = AV26; # Bank  21 - IO_L0N_21
NET  U1_AMH2_IO5               LOC = AW25; # Bank  21 - IO_L2P_21
NET  U1_AMH2_IO4               LOC = AY25; # Bank  21 - IO_L2N_21
NET  U1_AMH2_IO3               LOC = AK23; # Bank  21 - IO_L3P_21
NET  U1_AMH2_IO2               LOC = AL23; # Bank  21 - IO_L3N_21
NET  U1_AMH2_IO1               LOC = BD25; # Bank  21 - IO_L4P_21
NET  U1_AMH2_IO0               LOC = BD26; # Bank  21 - IO_L4N_VREF_21

NET  U1_AMH1_IO7               LOC = AW26; # Bank  21 - IO_L5P_21
NET  U1_AMH1_IO6               LOC = AY26; # Bank  21 - IO_L5N_21
NET  U1_AMH1_IO5               LOC = AN23; # Bank  21 - IO_L6P_21
NET  U1_AMH1_IO4               LOC = AP23; # Bank  21 - IO_L6N_21
NET  U1_AMH1_IO3               LOC = BB26; # Bank  21 - IO_L7P_21
NET  U1_AMH1_IO2               LOC = BC26; # Bank  21 - IO_L7N_21
NET  U1_AMH1_IO1               LOC = BA24; # Bank  21 - IO_L8P_SRCC_21
NET  U1_AMH1_IO0               LOC = BB24; # Bank  21 - IO_L8N_SRCC_21
```

Appendix D

ML630 Master UCF Listing for U2

The ML630 master user constraints file (UCF) template provides for designs targeting the ML630 board. Net names in the constraints listed below correlate with net names on the ML630 board schematic. Users must identify the appropriate pins and replace the net names below with net names in the user RTL. See the Constraints Guide for more information.

```
############################################################
##
##  ML630 FPGA U2 PIN LOCS: INITIAL RELEASE
##
##  FPGA = HX380T-2FFG1924 OR HX565T-2FFG1924
##
############################################################

##
## GLOBAL LVDS CLOCK INPUTS:
## ALL SI570 @I2C 0X5D, DEFAULT STARTUP = 156.25MHZ
##
NET  U2_LVDS_OSC_P              LOC = AR33; # Bank  24 - 200MHz
NET  U2_LVDS_OSC_N              LOC = AT33; # Bank  24 - 200MHz
NET  U2_SI570_4_P               LOC =  N11; # Bank  35 - 156.25MHz
NET  U2_SI570_4_N               LOC =  M10; # Bank  35 - 156.25MHz
NET  U2_SI570_5_P               LOC =  N12; # Bank  35 - 156.25MHz
NET  U2_SI570_5_N               LOC =  M12; # Bank  35 - 156.25MHz

##
## FPGA CONTROL FOR 2:1 GTH REFCLK MUX:
##
NET  U2_GTHREFCLK_LS_SEL0       LOC =  G12; # Bank  35 - IO_L10P_MRCC_35
NET  U2_GTHREFCLK_LS_SEL1       LOC =  F12; # Bank  35 - IO_L10N_MRCC_35

##
## FPGA I2C INTERFACE:
##
NET  U2_SCL_MAIN                LOC =  H12; # Bank  35 - CLOCKS, EEPROM
NET  U2_SDA_MAIN                LOC =  G11; # Bank  35 - SHARED WITH U1
NET  U2_SDA_LS                  LOC =  K10; # Bank  35 - FMC2
NET  U2_SCL_LS                  LOC =  J10; # Bank  35 - FMC2

##
## CP2103 USB-TO-UART BRIDGE INTERFACE:
##
NET  U2_USB_CTS_I_B             LOC =  P11; # Bank  35 - IO_L12P_SM5P_35
NET  U2_USB_RTS_0_B             LOC =  P10; # Bank  35 - IO_L12N_SM5N_35
NET  U2_USB_RXD_I               LOC =  F10; # Bank  35 - IO_L13P_SM6P_35
NET  U2_USB_TXD_0               LOC =  E10; # Bank  35 - IO_L13N_SM6N_35
```

```
NET  U2_USB_GPIO_3              LOC =  E11; # Bank  35 - IO_L14P_35
NET  U2_USB_GPIO_2              LOC =  D10; # Bank  35 - IO_L14N_VREF_35
NET  U2_USB_GPIO_1              LOC =  M11; # Bank  35 - IO_L15P_SM7P_35
NET  U2_USB_GPIO_0              LOC =  L10; # Bank  35 - IO_L15N_SM7N_35

##
## USER PUSHBUTTON SWITCHES:
##
NET  U2_USER_PB4                LOC =  N23; # Bank  28 - IO_L18P_28
NET  U2_USER_PB3                LOC =  N24; # Bank  28 - IO_L18N_28
NET  U2_USER_PB2                LOC =  J26; # Bank  28 - IO_L19P_28
NET  U2_USER_PB1                LOC =  H26; # Bank  28 - IO_L19N_28

##
## USER LEDS:
##
NET  U2_USER_LED8               LOC =  A34; # Bank  25 - IO_L0P_25
NET  U2_USER_LED7               LOC =  A35; # Bank  25 - IO_L0N_25
NET  U2_USER_LED6               LOC =  B35; # Bank  25 - IO_L1P_25
NET  U2_USER_LED5               LOC =  B36; # Bank  25 - IO_L1N_25
NET  U2_USER_LED4               LOC =  B37; # Bank  25 - IO_L2P_SM8P_25
NET  U2_USER_LED3               LOC =  A37; # Bank  25 - IO_L2N_SM8N_25
NET  U2_USER_LED2               LOC =  L33; # Bank  25 - IO_L3P_SM9P_25
NET  U2_USER_LED1               LOC =  K33; # Bank  25 - IO_L3N_SM9N_25

##
## SLIDE SWITCH (8 POSITION):]
##
NET  U2_USER_SW8                LOC =  F20; # Bank  38 - IO_L16P_38
NET  U2_USER_SW7                LOC =  E20; # Bank  38 - IO_L16N_38
NET  U2_USER_SW6                LOC =  H21; # Bank  38 - IO_L17P_38
NET  U2_USER_SW5                LOC =  G20; # Bank  38 - IO_L17N_38
NET  U2_USER_SW4                LOC =  R21; # Bank  38 - IO_L18P_38
NET  U2_USER_SW3                LOC =  P21; # Bank  38 - IO_L18N_38
NET  U2_USER_SW2                LOC =  K21; # Bank  38 - IO_L19P_38
NET  U2_USER_SW1                LOC =  J20; # Bank  38 - IO_L19N_38
##
## USER I/O HEADER:
##
NET  U2_USER_IO_6               LOC =  P34; # Bank  25 - IO_L4P_25
NET  U2_USER_IO_5               LOC =  P35; # Bank  25 - IO_L4N_VREF_25
NET  U2_USER_IO_4               LOC =  E35; # Bank  25 - IO_L5P_SM10P_25
NET  U2_USER_IO_3               LOC =  D35; # Bank  25 - IO_L5N_SM10N_25
NET  U2_USER_IO_2               LOC =  K35; # Bank  25 - IO_L6P_SM11P_25
NET  U2_USER_IO_1               LOC =  J35; # Bank  25 - IO_L6N_SM11N_25

##
## VGA2 DEBUG HEADER:
##
NET  U2_VGA_R_3                 LOC =  C34; # Bank  25 - IO_L7P_SM12P_25
NET  U2_VGA_R_2                 LOC =  B34; # Bank  25 - IO_L7N_SM12N_25
NET  U2_VGA_R_1                 LOC =  D33; # Bank  25 - IO_L8P_SRCC_25
NET  U2_VGA_R_0                 LOC =  D34; # Bank  25 - IO_L8N_SRCC_25
NET  U2_VGA_G_3                 LOC =  N33; # Bank  25 - IO_L9P_MRCC_25
NET  U2_VGA_G_2                 LOC =  N34; # Bank  25 - IO_L9N_MRCC_25
NET  U2_VGA_G_1                 LOC =  M35; # Bank  25 - IO_L10P_MRCC_25
NET  U2_VGA_G_0                 LOC =  L35; # Bank  25 - IO_L10N_MRCC_25
NET  U2_VGA_B_3                 LOC =  G35; # Bank  25 - IO_L11P_SRCC_25
NET  U2_VGA_B_2                 LOC =  F35; # Bank  25 - IO_L11N_SRCC_25
```

```
NET  U2_VGA_B_1                LOC =  P31; # Bank  25 - IO_L12P_SM13P_25
NET  U2_VGA_B_0                LOC =  N32; # Bank  25 - IO_L12N_SM13N_25
NET  U2_VGA_HSYNC              LOC =  F33; # Bank  25 - IO_L13P_SM14P_25
NET  U2_VGA_VSYNC              LOC =  E33; # Bank  25 - IO_L13N_SM14N_25

##
## DCI:
##
NET  U2_VRN_21                  LOC = AP25; # Bank  21 - IO_L12P_VRN_21
NET  U2_VRP_21                  LOC = AR25; # Bank  21 - IO_L12N_VRP_21
NET  U2_VRN_22                  LOC = AJ25; # Bank  22 - IO_L12P_VRN_22
NET  U2_VRP_22                  LOC = AK26; # Bank  22 - IO_L12N_VRP_22
NET  U2_VRN_25                  LOC =  M34; # Bank  25 - IO_L16P_VRN_25
NET  U2_VRP_25                  LOC =  L34; # Bank  25 - IO_L16N_VRP_25
NET  U2_VRN_35                  LOC =  L12; # Bank  35 - IO_L16P_VRN_35
NET  U2_VRP_35                  LOC =  K12; # Bank  35 - IO_L16N_VRP_35
NET  U2_VRN_36                  LOC =  N14; # Bank  36 - IO_L12P_VRN_36
NET  U2_VRP_36                  LOC =  M14; # Bank  36 - IO_L12N_VRP_36


##
## FMC2:
##
NET  FMC2_PRSNT_M2C_L           LOC = BA25; # Bank  21 - IO_L19P_21

NET  FMC2_CLK0_M2C_P            LOC = AP21; # Bank  31 - IO_L9P_MRCC_31
NET  FMC2_CLK0_M2C_N            LOC = AR20; # Bank  31 - IO_L9N_MRCC_31
NET  FMC2_CLK1_M2C_P            LOC = AR23; # Bank  21 - IO_L9P_MRCC_21
NET  FMC2_CLK1_M2C_N            LOC = AT23; # Bank  21 - IO_L9N_MRCC_21

NET  FMC2_LA33_P                LOC = AJ28; # Bank  22 - IO_L3P_22
NET  FMC2_LA33_N                LOC = AK28; # Bank  22 - IO_L3N_22
NET  FMC2_LA32_P                LOC = AM25; # Bank  22 - IO_L15P_22
NET  FMC2_LA32_N                LOC = AM26; # Bank  22 - IO_L15N_22
NET  FMC2_LA31_P                LOC = AM27; # Bank  22 - IO_L0P_22
NET  FMC2_LA31_N                LOC = AN28; # Bank  22 - IO_L0N_22
NET  FMC2_LA30_P                LOC = AL27; # Bank  22 - IO_L6P_22
NET  FMC2_LA30_N                LOC = AL28; # Bank  22 - IO_L6N_22
NET  FMC2_LA29_P                LOC = AR26; # Bank  22 - IO_L5P_22
NET  FMC2_LA29_N                LOC = AR27; # Bank  22 - IO_L5N_22
NET  FMC2_LA28_P                LOC = AR28; # Bank  22 - IO_L2P_22
NET  FMC2_LA28_N                LOC = AT28; # Bank  22 - IO_L2N_22
NET  FMC2_LA27_P                LOC = AY28; # Bank  22 - IO_L8P_SRCC_22
NET  FMC2_LA27_N                LOC = BA29; # Bank  22 - IO_L8N_SRCC_22
NET  FMC2_LA26_P                LOC = AY27; # Bank  22 - IO_L13P_22
NET  FMC2_LA26_N                LOC = BA28; # Bank  22 - IO_L13N_22
NET  FMC2_LA25_P                LOC = AV27; # Bank  22 - IO_L11P_SRCC_22
NET  FMC2_LA25_N                LOC = AW28; # Bank  22 - IO_L11N_SRCC_22
NET  FMC2_LA24_P                LOC = AV28; # Bank  22 - IO_L4P_22
NET  FMC2_LA24_N                LOC = AW29; # Bank  22 - IO_L4N_VREF_22
NET  FMC2_LA23_P                LOC = BA27; # Bank  22 - IO_L16P_22
NET  FMC2_LA23_N                LOC = BB27; # Bank  22 - IO_L16N_22
NET  FMC2_LA22_P                LOC = AT27; # Bank  22 - IO_L7P_22
NET  FMC2_LA22_N                LOC = AU27; # Bank  22 - IO_L7N_22
NET  FMC2_LA21_P                LOC = BB29; # Bank  22 - IO_L17P_22
NET  FMC2_LA21_N                LOC = BC29; # Bank  22 - IO_L17N_22
NET  FMC2_LA20_P                LOC = BC27; # Bank  22 - IO_L14P_22
NET  FMC2_LA20_N                LOC = BD28; # Bank  22 - IO_L14N_VREF_22
NET  FMC2_LA19_P                LOC = AN27; # Bank  22 - IO_L1P_22
```

```
NET  FMC2_LA19_N                LOC = AP28; # Bank  22 - IO_L1N_22
NET  FMC2_LA18_CC_P             LOC = AJ26; # Bank  22 - IO_L9P_MRCC_22
NET  FMC2_LA18_CC_N             LOC = AK27; # Bank  22 - IO_L9N_MRCC_22
NET  FMC2_LA17_CC_P            LOC = AN26; # Bank  22 - IO_L10P_MRCC_22
NET  FMC2_LA17_CC_N            LOC = AP26; # Bank  22 - IO_L10N_MRCC_22
NET  FMC2_LA16_P                LOC = BD25; # Bank  21 - IO_L4P_21
NET  FMC2_LA16_N                LOC = BD26; # Bank  21 - IO_L4N_VREF_21
NET  FMC2_LA15_P                LOC = BB26; # Bank  21 - IO_L7P_21
NET  FMC2_LA15_N                LOC = BC26; # Bank  21 - IO_L7N_21
NET  FMC2_LA14_P                LOC = BC24; # Bank  21 - IO_L17P_21
NET  FMC2_LA14_N                LOC = BD24; # Bank  21 - IO_L17N_21
NET  FMC2_LA13_P                LOC = BC23; # Bank  21 - IO_L16P_21
NET  FMC2_LA13_N                LOC = BD23; # Bank  21 - IO_L16N_21
NET  FMC2_LA12_P                LOC = AK23; # Bank  21 - IO_L3P_21
NET  FMC2_LA12_N                LOC = AL23; # Bank  21 - IO_L3N_21
NET  FMC2_LA11_P                LOC = AW26; # Bank  21 - IO_L5P_21
NET  FMC2_LA11_N                LOC = AY26; # Bank  21 - IO_L5N_21
NET  FMC2_LA10_P                LOC = AW25; # Bank  21 - IO_L2P_21
NET  FMC2_LA10_N                LOC = AY25; # Bank  21 - IO_L2N_21
NET  FMC2_LA09_P                LOC = BA24; # Bank  21 - IO_L8P_SRCC_21
NET  FMC2_LA09_N                LOC = BB24; # Bank  21 - IO_L8N_SRCC_21
NET  FMC2_LA08_P                LOC = AT24; # Bank  21 - IO_L14P_21
NET  FMC2_LA08_N               LOC = AU24; # Bank  21 - IO_L14N_VREF_21
NET  FMC2_LA07_P                LOC = AV24; # Bank  21 - IO_L13P_21
NET  FMC2_LA07_N                LOC = AW24; # Bank  21 - IO_L13N_21
NET  FMC2_LA06_P                LOC = AU26; # Bank  21 - IO_L0P_21
NET  FMC2_LA06_N                LOC = AV26; # Bank  21 - IO_L0N_21
NET  FMC2_LA05_P                LOC = AT25; # Bank  21 - IO_L1P_21
NET  FMC2_LA05_N                LOC = AU25; # Bank  21 - IO_L1N_21
NET  FMC2_LA04_P                LOC = AN23; # Bank  21 - IO_L6P_21
NET  FMC2_LA04_N                LOC = AP23; # Bank  21 - IO_L6N_21
NET  FMC2_LA03_P                LOC = AN24; # Bank  21 - IO_L18P_21
NET  FMC2_LA03_N                LOC = AP24; # Bank  21 - IO_L18N_21
NET  FMC2_LA02_P                LOC = AL24; # Bank  21 - IO_L15P_21
NET  FMC2_LA02_N                LOC = AM24; # Bank  21 - IO_L15N_21
NET  FMC2_LA01_CC_P            LOC = AY23; # Bank  21 - IO_L11P_SRCC_21
NET  FMC2_LA01_CC_N            LOC = BA23; # Bank  21 - IO_L11N_SRCC_21
NET  FMC2_LA00_CC_P            LOC = AV23; # Bank  21 - IO_L10P_MRCC_21
NET  FMC2_LA00_CC_N            LOC = AW23; # Bank  21 - IO_L10N_MRCC_21


NET  FMC2_HA23_P                LOC = BD34; # Bank  24 - IO_L17P_VRN_24
NET  FMC2_HA23_N                LOC = BD35; # Bank  24 - IO_L17N_VRP_24
NET  FMC2_HA22_P                LOC = BB34; # Bank  24 - IO_L16P_RS0_24
NET  FMC2_HA22_N               LOC = BC34; # Bank  24 - IO_L16N_CSO_B_24
NET  FMC2_HA21_P               LOC = AW33; # Bank  24 - IO_L14P_FCS_B_24
NET  FMC2_HA21_N                LOC = AY33; # Bank  24 -
IO_L14N_VREF_FOE_B_MOSI
NET  FMC2_HA20_P               LOC = AN32; # Bank  24 - IO_L15P_FWE_B_24
NET  FMC2_HA20_N                LOC = AN33; # Bank  24 - IO_L15N_RS1_24
NET  FMC2_HA19_P               LOC = BA33; # Bank  24 - IO_L13P_D1_FS1_24
NET  FMC2_HA19_N               LOC = BA34; # Bank  24 - IO_L13N_D0_FS0_24
NET  FMC2_HA18_P                LOC = AN34; # Bank  24 - IO_L12P_D3_24
NET  FMC2_HA18_N               LOC = AP35; # Bank  24 - IO_L12N_D2_FS2_24
NET  FMC2_HA17_CC_P             LOC = AL33; # Bank  24 - IO_L9P_MRCC_24
NET  FMC2_HA17_CC_N             LOC = AM34; # Bank  24 - IO_L9N_MRCC_24
NET  FMC2_HA16_P                LOC = BB22; # Bank  31 - IO_L16P_31
NET  FMC2_HA16_N                LOC = BC22; # Bank  31 - IO_L16N_31
NET  FMC2_HA15_P                LOC = BA20; # Bank  31 - IO_L5P_31
```

```
NET  FMC2_HA15_N              LOC = BB20; # Bank  31 - IO_L5N_31
NET  FMC2_HA14_P              LOC = AY22; # Bank  31 - IO_L19P_31
NET  FMC2_HA14_N              LOC = AY21; # Bank  31 - IO_L19N_31
NET  FMC2_HA13_P              LOC = BC21; # Bank  31 - IO_L17P_31
NET  FMC2_HA13_N              LOC = BD21; # Bank  31 - IO_L17N_31
NET  FMC2_HA12_P              LOC = BB19; # Bank  31 - IO_L7P_31
NET  FMC2_HA12_N              LOC = BC19; # Bank  31 - IO_L7N_31
NET  FMC2_HA11_P              LOC = AT22; # Bank  31 - IO_L13P_31
NET  FMC2_HA11_N              LOC = AU22; # Bank  31 - IO_L13N_31
NET  FMC2_HA10_P              LOC = AU21; # Bank  31 - IO_L14P_31
NET  FMC2_HA10_N             LOC = AV21; # Bank  31 - IO_L14N_VREF_31
NET  FMC2_HA09_P              LOC = AL22; # Bank  31 - IO_L15P_31
NET  FMC2_HA09_N              LOC = AM21; # Bank  31 - IO_L15N_31
NET  FMC2_HA08_P              LOC = AT20; # Bank  31 - IO_L1P_31
NET  FMC2_HA08_N              LOC = AU20; # Bank  31 - IO_L1N_31
NET  FMC2_HA07_P              LOC = AM22; # Bank  31 - IO_L18P_31
NET  FMC2_HA07_N              LOC = AN22; # Bank  31 - IO_L18N_31
NET  FMC2_HA06_P              LOC = AR22; # Bank  31 - IO_L12P_VRN_31
NET  FMC2_HA06_N              LOC = AR21; # Bank  31 - IO_L12N_VRP_31
NET  FMC2_HA05_P              LOC = AY20; # Bank  31 - IO_L4P_31
NET  FMC2_HA05_N              LOC = BA19; # Bank  31 - IO_L4N_VREF_31
NET  FMC2_HA04_P              LOC = AW20; # Bank  31 - IO_L2P_31
NET  FMC2_HA04_N              LOC = AW19; # Bank  31 - IO_L2N_31
NET  FMC2_HA03_P              LOC = AN21; # Bank  31 - IO_L6P_31
NET  FMC2_HA03_N              LOC = AP20; # Bank  31 - IO_L6N_31
NET  FMC2_HA02_P              LOC = AK22; # Bank  31 - IO_L3P_31
NET  FMC2_HA02_N              LOC = AK21; # Bank  31 - IO_L3N_31
NET  FMC2_HA01_CC_P           LOC = AV22; # Bank  31 - IO_L10P_MRCC_31
NET  FMC2_HA01_CC_N           LOC = AW21; # Bank  31 - IO_L10N_MRCC_31
NET  FMC2_HA00_CC_P           LOC = BA22; # Bank  31 - IO_L11P_SRCC_31
NET  FMC2_HA00_CC_N           LOC = BB21; # Bank  31 - IO_L11N_SRCC_31


NET  FMC2_HB21_P              LOC = AL32; # Bank  24 - IO_L18P_24
NET  FMC2_HB21_N              LOC = AM32; # Bank  24 - IO_L18N_24
NET  FMC2_HB20_P              LOC = BC33; # Bank  24 - IO_L19P_24
NET  FMC2_HB20_N              LOC = BD33; # Bank  24 - IO_L19N_24
NET  FMC2_HB19_P              LOC = AM31; # Bank  23 - IO_L15P_23
NET  FMC2_HB19_N              LOC = AN31; # Bank  23 - IO_L15N_23
NET  FMC2_HB18_P              LOC = AM29; # Bank  23 - IO_L18P_23
NET  FMC2_HB18_N              LOC = AN29; # Bank  23 - IO_L18N_23
NET  FMC2_HB17_CC_P           LOC = AJ29; # Bank  23 - IO_L9P_MRCC_23
NET  FMC2_HB17_CC_N           LOC = AJ30; # Bank  23 - IO_L9N_MRCC_23
NET  FMC2_HB16_P              LOC = AL29; # Bank  23 - IO_L12P_VRN_23
NET  FMC2_HB16_N              LOC = AM30; # Bank  23 - IO_L12N_VRP_23
NET  FMC2_HB15_P              LOC = AK30; # Bank  23 - IO_L6P_23
NET  FMC2_HB15_N              LOC = AL30; # Bank  23 - IO_L6N_23
NET  FMC2_HB14_P              LOC = AJ31; # Bank  23 - IO_L3P_23
NET  FMC2_HB14_N              LOC = AK31; # Bank  23 - IO_L3N_23
NET  FMC2_HB13_P              LOC = AR30; # Bank  23 - IO_L4P_23
NET  FMC2_HB13_N              LOC = AT30; # Bank  23 - IO_L4N_VREF_23
NET  FMC2_HB12_P              LOC = AP31; # Bank  23 - IO_L0P_23
NET  FMC2_HB12_N              LOC = AR31; # Bank  23 - IO_L0N_23
NET  FMC2_HB11_P              LOC = AT29; # Bank  23 - IO_L7P_23
NET  FMC2_HB11_N              LOC = AU30; # Bank  23 - IO_L7N_23
NET  FMC2_HB10_P              LOC = AP29; # Bank  23 - IO_L1P_23
NET  FMC2_HB10_N              LOC = AP30; # Bank  23 - IO_L1N_23
NET  FMC2_HB09_P              LOC = AU31; # Bank  23 - IO_L2P_23
NET  FMC2_HB09_N              LOC = AV31; # Bank  23 - IO_L2N_23
```

```
NET  FMC2_HB08_P                LOC = AU32; # Bank  23 - IO_L5P_23
NET  FMC2_HB08_N                LOC = AV32; # Bank  23 - IO_L5N_23
NET  FMC2_HB07_P                LOC = AU29; # Bank  23 - IO_L14P_23
NET  FMC2_HB07_N               LOC = AV29; # Bank  23 - IO_L14N_VREF_23
NET  FMC2_HB06_CC_P            LOC = AW31; # Bank  23 - IO_L11P_SRCC_23
NET  FMC2_HB06_CC_N            LOC = AY31; # Bank  23 - IO_L11N_SRCC_23
NET  FMC2_HB05_P                LOC = AW30; # Bank  23 - IO_L16P_23
NET  FMC2_HB05_N                LOC = AY30; # Bank  23 - IO_L16N_23
NET  FMC2_HB04_P                LOC = AY32; # Bank  23 - IO_L8P_SRCC_23
NET  FMC2_HB04_N                LOC = BA32; # Bank  23 - IO_L8N_SRCC_23
NET  FMC2_HB03_P                LOC = BD30; # Bank  23 - IO_L19P_23
NET  FMC2_HB03_N                LOC = BD31; # Bank  23 - IO_L19N_23
NET  FMC2_HB02_P                LOC = BA30; # Bank  23 - IO_L17P_23
NET  FMC2_HB02_N                LOC = BB30; # Bank  23 - IO_L17N_23
NET  FMC2_HB01_P                LOC = BB32; # Bank  23 - IO_L13P_23
NET  FMC2_HB01_N                LOC = BC32; # Bank  23 - IO_L13N_23
NET  FMC2_HB00_CC_P            LOC = BB31; # Bank  23 - IO_L10P_MRCC_23
NET  FMC2_HB00_CC_N            LOC = BC31; # Bank  23 - IO_L10N_MRCC_23


##
## FPGA TO FPGA LVDS (4 BANKS, 20 PAIRS PER BANK):
##
NET  U1_B26_LVDS_00_P           LOC =  B31; # Bank  26 - IO_L0P_26
NET  U1_B26_LVDS_00_N           LOC =  A32; # Bank  26 - IO_L0N_26
NET  U1_B26_LVDS_01_P           LOC =  B30; # Bank  26 - IO_L1P_26
NET  U1_B26_LVDS_01_N           LOC =  A30; # Bank  26 - IO_L1N_26
NET  U1_B26_LVDS_02_P           LOC =  C32; # Bank  26 - IO_L2P_26
NET  U1_B26_LVDS_02_N           LOC =  C33; # Bank  26 - IO_L2N_26
NET  U1_B26_LVDS_03_P           LOC =  M30; # Bank  26 - IO_L3P_26
NET  U1_B26_LVDS_03_N           LOC =  M31; # Bank  26 - IO_L3N_26
NET  U1_B26_LVDS_04_P           LOC =  E30; # Bank  26 - IO_L4P_26
NET  U1_B26_LVDS_04_N           LOC =  D30; # Bank  26 - IO_L4N_VREF_26
NET  U1_B26_LVDS_05_P           LOC =  B32; # Bank  26 - IO_L5P_26
NET  U1_B26_LVDS_05_N           LOC =  A33; # Bank  26 - IO_L5N_26
NET  U1_B26_LVDS_06_P           LOC =  N29; # Bank  26 - IO_L6P_26
NET  U1_B26_LVDS_06_N           LOC =  M29; # Bank  26 - IO_L6N_26
NET  U1_B26_LVDS_07_P           LOC =  D31; # Bank  26 - IO_L7P_26
NET  U1_B26_LVDS_07_N           LOC =  C31; # Bank  26 - IO_L7N_26
NET  U1_B26_LVDS_08_P           LOC =  G31; # Bank  26 - IO_L8P_SRCC_26
NET  U1_B26_LVDS_08_N           LOC =  F32; # Bank  26 - IO_L8N_SRCC_26
NET  U1_B26_LVDS_09_P           LOC =  R28; # Bank  26 - IO_L9P_MRCC_26
NET  U1_B26_LVDS_09_N           LOC =  P29; # Bank  26 - IO_L9N_MRCC_26
NET  U1_B26_LVDS_10_P          LOC =  J31; # Bank  26 - IO_L10P_MRCC_26
NET  U1_B26_LVDS_10_N          LOC =  H32; # Bank  26 - IO_L10N_MRCC_26
NET  U1_B26_LVDS_11_P          LOC =  E31; # Bank  26 - IO_L11P_SRCC_26
NET  U1_B26_LVDS_11_N          LOC =  E32; # Bank  26 - IO_L11N_SRCC_26
NET  U1_B26_LVDS_12_P           LOC =  N31; # Bank  26 - IO_L12P_VRN_26
NET  U1_B26_LVDS_12_N           LOC =  M32; # Bank  26 - IO_L12N_VRP_26
NET  U1_B26_LVDS_13_P           LOC =  G30; # Bank  26 - IO_L13P_26
NET  U1_B26_LVDS_13_N           LOC =  F30; # Bank  26 - IO_L13N_26
NET  U1_B26_LVDS_14_P           LOC =  L30; # Bank  26 - IO_L14P_26
NET  U1_B26_LVDS_14_N          LOC =  K31; # Bank  26 - IO_L14N_VREF_26
NET  U1_B26_LVDS_15_P           LOC =  R30; # Bank  26 - IO_L15P_26
NET  U1_B26_LVDS_15_N           LOC =  P30; # Bank  26 - IO_L15N_26
NET  U1_B26_LVDS_16_P           LOC =  L32; # Bank  26 - IO_L16P_26
NET  U1_B26_LVDS_16_N           LOC =  K32; # Bank  26 - IO_L16N_26
NET  U1_B26_LVDS_17_P           LOC =  H31; # Bank  26 - IO_L17P_26
NET  U1_B26_LVDS_17_N           LOC =  G32; # Bank  26 - IO_L17N_26
```

```
NET  U1_B26_LVDS_18_P          LOC =  T29; # Bank  26 - IO_L18P_26
NET  U1_B26_LVDS_18_N          LOC =  T30; # Bank  26 - IO_L18N_26
NET  U1_B26_LVDS_19_P          LOC =  K30; # Bank  26 - IO_L19P_26
NET  U1_B26_LVDS_19_N          LOC =  J30; # Bank  26 - IO_L19N_26


NET  U1_B32_LVDS_13_P          LOC = AM17; # Bank  32 - IO_L0P_32
NET  U1_B32_LVDS_13_N          LOC = AN17; # Bank  32 - IO_L0N_32
NET  U1_B32_LVDS_09_P          LOC = AN18; # Bank  32 - IO_L1P_32
NET  U1_B32_LVDS_09_N          LOC = AP18; # Bank  32 - IO_L1N_32
NET  U1_B32_LVDS_18_P          LOC = AR18; # Bank  32 - IO_L2P_32
NET  U1_B32_LVDS_18_N          LOC = AR17; # Bank  32 - IO_L2N_32
NET  U1_B32_LVDS_12_P          LOC = AK17; # Bank  32 - IO_L3P_32
NET  U1_B32_LVDS_12_N          LOC = AL17; # Bank  32 - IO_L3N_32
NET  U1_B32_LVDS_10_P          LOC = AV17; # Bank  32 - IO_L4P_32
NET  U1_B32_LVDS_10_N          LOC = AW16; # Bank  32 - IO_L4N_VREF_32
NET  U1_B32_LVDS_05_P          LOC = AT17; # Bank  32 - IO_L5P_32
NET  U1_B32_LVDS_05_N          LOC = AU17; # Bank  32 - IO_L5N_32
NET  U1_B32_LVDS_03_P          LOC = AJ18; # Bank  32 - IO_L6P_32
NET  U1_B32_LVDS_03_N          LOC = AK18; # Bank  32 - IO_L6N_32
NET  U1_B32_LVDS_17_P          LOC = AT19; # Bank  32 - IO_L7P_32
NET  U1_B32_LVDS_17_N          LOC = AT18; # Bank  32 - IO_L7N_32
NET  U1_B32_LVDS_14_P          LOC = BB17; # Bank  32 - IO_L8P_SRCC_32
NET  U1_B32_LVDS_14_N          LOC = BC16; # Bank  32 - IO_L8N_SRCC_32
NET  U1_B32_LVDS_00_P          LOC = AL19; # Bank  32 - IO_L9P_MRCC_32
NET  U1_B32_LVDS_00_N          LOC = AL18; # Bank  32 - IO_L9N_MRCC_32
NET  U1_B32_LVDS_08_P         LOC = AN19; # Bank  32 - IO_L10P_MRCC_32
NET  U1_B32_LVDS_08_N         LOC = AP19; # Bank  32 - IO_L10N_MRCC_32
NET  U1_B32_LVDS_01_P         LOC = AV18; # Bank  32 - IO_L11P_SRCC_32
NET  U1_B32_LVDS_01_N         LOC = AW18; # Bank  32 - IO_L11N_SRCC_32
NET  U1_B32_LVDS_06_P          LOC = AM20; # Bank  32 - IO_L12P_VRN_32
NET  U1_B32_LVDS_06_N          LOC = AM19; # Bank  32 - IO_L12N_VRP_32
NET  U1_B32_LVDS_11_P          LOC = AY17; # Bank  32 - IO_L13P_32
NET  U1_B32_LVDS_11_N          LOC = AY16; # Bank  32 - IO_L13N_32
NET  U1_B32_LVDS_07_P          LOC = BC18; # Bank  32 - IO_L14P_32
NET  U1_B32_LVDS_07_N         LOC = BD18; # Bank  32 - IO_L14N_VREF_32
NET  U1_B32_LVDS_15_P          LOC = AJ20; # Bank  32 - IO_L15P_32
NET  U1_B32_LVDS_15_N          LOC = AJ19; # Bank  32 - IO_L15N_32
NET  U1_B32_LVDS_19_P          LOC = AY18; # Bank  32 - IO_L16P_32
NET  U1_B32_LVDS_19_N          LOC = BA18; # Bank  32 - IO_L16N_32
NET  U1_B32_LVDS_16_P          LOC = BA17; # Bank  32 - IO_L17P_32
NET  U1_B32_LVDS_16_N          LOC = BB16; # Bank  32 - IO_L17N_32
NET  U1_B32_LVDS_02_P          LOC = AK20; # Bank  32 - IO_L18P_32
NET  U1_B32_LVDS_02_N          LOC = AL20; # Bank  32 - IO_L18N_32
NET  U1_B32_LVDS_04_P          LOC = BC17; # Bank  32 - IO_L19P_32
NET  U1_B32_LVDS_04_N          LOC = BD16; # Bank  32 - IO_L19N_32


NET  U1_B33_LVDS_00_P          LOC = AR15; # Bank  33 - IO_L0P_33
NET  U1_B33_LVDS_00_N          LOC = AT14; # Bank  33 - IO_L0N_33
NET  U1_B33_LVDS_18_P          LOC = AP15; # Bank  33 - IO_L1P_33
NET  U1_B33_LVDS_18_N          LOC = AP14; # Bank  33 - IO_L1N_33
NET  U1_B33_LVDS_17_P          LOC = AV14; # Bank  33 - IO_L2P_33
NET  U1_B33_LVDS_17_N          LOC = AW14; # Bank  33 - IO_L2N_33
NET  U1_B33_LVDS_09_P          LOC = AJ15; # Bank  33 - IO_L3P_33
NET  U1_B33_LVDS_09_N          LOC = AJ14; # Bank  33 - IO_L3N_33
NET  U1_B33_LVDS_02_P          LOC = AP16; # Bank  33 - IO_L4P_33
NET  U1_B33_LVDS_02_N          LOC = AR16; # Bank  33 - IO_L4N_VREF_33
NET  U1_B33_LVDS_04_P          LOC = AU14; # Bank  33 - IO_L5P_33
```

```
NET  U1_B33_LVDS_04_N          LOC = AV13; # Bank  33 - IO_L5N_33
NET  U1_B33_LVDS_06_P          LOC = AJ16; # Bank  33 - IO_L6P_33
NET  U1_B33_LVDS_06_N          LOC = AK16; # Bank  33 - IO_L6N_33
NET  U1_B33_LVDS_11_P          LOC = AT15; # Bank  33 - IO_L7P_33
NET  U1_B33_LVDS_11_N          LOC = AU15; # Bank  33 - IO_L7N_33
NET  U1_B33_LVDS_16_P          LOC = BA14; # Bank  33 - IO_L8P_SRCC_33
NET  U1_B33_LVDS_16_N          LOC = BA13; # Bank  33 - IO_L8N_SRCC_33
NET  U1_B33_LVDS_03_P          LOC = AK15; # Bank  33 - IO_L9P_MRCC_33
NET  U1_B33_LVDS_03_N          LOC = AL14; # Bank  33 - IO_L9N_MRCC_33
NET  U1_B33_LVDS_08_P         LOC = BC14; # Bank  33 - IO_L10P_MRCC_33
NET  U1_B33_LVDS_08_N         LOC = BD13; # Bank  33 - IO_L10N_MRCC_33
NET  U1_B33_LVDS_14_P         LOC = AW13; # Bank  33 - IO_L11P_SRCC_33
NET  U1_B33_LVDS_14_N         LOC = AY13; # Bank  33 - IO_L11N_SRCC_33
NET  U1_B33_LVDS_12_P          LOC = AL15; # Bank  33 - IO_L12P_VRN_33
NET  U1_B33_LVDS_12_N          LOC = AM15; # Bank  33 - IO_L12N_VRP_33
NET  U1_B33_LVDS_10_P          LOC = BB14; # Bank  33 - IO_L13P_33
NET  U1_B33_LVDS_10_N          LOC = BC13; # Bank  33 - IO_L13N_33
NET  U1_B33_LVDS_01_P          LOC = AU16; # Bank  33 - IO_L14P_33
NET  U1_B33_LVDS_01_N         LOC = AV16; # Bank  33 - IO_L14N_VREF_33
NET  U1_B33_LVDS_15_P          LOC = AM14; # Bank  33 - IO_L15P_33
NET  U1_B33_LVDS_15_N          LOC = AN14; # Bank  33 - IO_L15N_33
NET  U1_B33_LVDS_13_P          LOC = BA15; # Bank  33 - IO_L16P_33
NET  U1_B33_LVDS_13_N          LOC = BB15; # Bank  33 - IO_L16N_33
NET  U1_B33_LVDS_19_P          LOC = AW15; # Bank  33 - IO_L17P_33
NET  U1_B33_LVDS_19_N          LOC = AY15; # Bank  33 - IO_L17N_33
NET  U1_B33_LVDS_07_P          LOC = AM16; # Bank  33 - IO_L18P_33
NET  U1_B33_LVDS_07_N          LOC = AN16; # Bank  33 - IO_L18N_33
NET  U1_B33_LVDS_05_P          LOC = BD15; # Bank  33 - IO_L19P_33
NET  U1_B33_LVDS_05_N          LOC = BD14; # Bank  33 - IO_L19N_33


NET  U1_B34_LVDS_05_P          LOC = AP11; # Bank  34 - IO_L0P_GC_34
NET  U1_B34_LVDS_05_N          LOC = AR11; # Bank  34 - IO_L0N_GC_34
NET  U1_B34_LVDS_14_P          LOC = AR12; # Bank  34 - IO_L1P_GC_34
NET  U1_B34_LVDS_14_N          LOC = AT12; # Bank  34 - IO_L1N_GC_34
NET  U1_B34_LVDS_00_P         LOC = AR10; # Bank  34 - IO_L2P_A15_D31_34
NET  U1_B34_LVDS_00_N         LOC = AT10; # Bank  34 - IO_L2N_A14_D30_34
NET  U1_B34_LVDS_09_P         LOC = AK10; # Bank  34 - IO_L3P_A13_D29_34
NET  U1_B34_LVDS_09_N         LOC = AL10; # Bank  34 - IO_L3N_A12_D28_34
NET  U1_B34_LVDS_01_P         LOC = AU11; # Bank  34 - IO_L4P_A11_D27_34
NET  U1_B34_LVDS_01_N          LOC = AU10; # Bank  34 -
IO_L4N_VREF_A10_D26_34
NET  U1_B34_LVDS_16_P         LOC = AV12; # Bank  34 - IO_L5P_A09_D25_34
NET  U1_B34_LVDS_16_N         LOC = AV11; # Bank  34 - IO_L5N_A08_D24_34
NET  U1_B34_LVDS_03_P         LOC = AM11; # Bank  34 - IO_L6P_A07_D23_34
NET  U1_B34_LVDS_03_N         LOC = AM10; # Bank  34 - IO_L6N_A06_D22_34
NET  U1_B34_LVDS_19_P         LOC = AW11; # Bank  34 - IO_L7P_A05_D21_34
NET  U1_B34_LVDS_19_N         LOC = AY11; # Bank  34 - IO_L7N_A04_D20_34
NET  U1_B34_LVDS_10_P          LOC = AP13; # Bank  34 - IO_L8P_SRCC_34
NET  U1_B34_LVDS_10_N          LOC = AR13; # Bank  34 - IO_L8N_SRCC_34
NET  U1_B34_LVDS_12_P          LOC = AL12; # Bank  34 - IO_L9P_MRCC_34
NET  U1_B34_LVDS_12_N          LOC = AM12; # Bank  34 - IO_L9N_MRCC_34
NET  U1_B34_LVDS_02_P         LOC = AW10; # Bank  34 - IO_L10P_MRCC_34
NET  U1_B34_LVDS_02_N         LOC = AY10; # Bank  34 - IO_L10N_MRCC_34
NET  U1_B34_LVDS_07_P         LOC = BA10; # Bank  34 - IO_L11P_SRCC_34
NET  U1_B34_LVDS_07_N         LOC = BB10; # Bank  34 - IO_L11N_SRCC_34
NET  U1_B34_LVDS_06_P        LOC = AN11; # Bank  34 - IO_L12P_A03_D19_34
NET  U1_B34_LVDS_06_N        LOC = AP10; # Bank  34 - IO_L12N_A02_D18_34
NET  U1_B34_LVDS_13_P        LOC = AT13; # Bank  34 - IO_L13P_A01_D17_34
```

```
NET  U1_B34_LVDS_13_N         LOC = AU12; # Bank  34 - IO_L13N_A00_D16_34
NET  U1_B34_LVDS_17_P           LOC = AY12; # Bank  34 - IO_L14P_A25_34
NET  U1_B34_LVDS_17_N           LOC = BA12; # Bank  34 -
IO_L14N_VREF_A24_34
NET  U1_B34_LVDS_18_P           LOC = AK13; # Bank  34 - IO_L15P_A23_34
NET  U1_B34_LVDS_18_N           LOC = AL13; # Bank  34 - IO_L15N_A22_34
NET  U1_B34_LVDS_04_P           LOC = BB11; # Bank  34 - IO_L16P_A21_34
NET  U1_B34_LVDS_04_N           LOC = BC11; # Bank  34 - IO_L16N_A20_34
NET  U1_B34_LVDS_11_P           LOC = BD11; # Bank  34 - IO_L17P_A19_34
NET  U1_B34_LVDS_11_N           LOC = BD10; # Bank  34 - IO_L17N_A18_34
NET  U1_B34_LVDS_15_P           LOC = AN13; # Bank  34 - IO_L18P_A17_34
NET  U1_B34_LVDS_15_N           LOC = AN12; # Bank  34 - IO_L18N_A16_34
NET  U1_B34_LVDS_08_P           LOC = BB12; # Bank  34 - IO_L19P_VRN_34
NET  U1_B34_LVDS_08_N           LOC = BC12; # Bank  34 - IO_L19N_VRP_34

##
## GTX REFCLKS:
##
NET  U2_MGTREFCLK0_100_P       LOC = BA37; # Bank 100 - MGTREFCLK0P_100
NET  U2_MGTREFCLK0_100_N       LOC = BA38; # Bank 100 - MGTREFCLK0N_100
NET  U2_MGTREFCLK1_100_P       LOC = AW37; # Bank 100 - MGTREFCLK1P_100
NET  U2_MGTREFCLK1_100_N       LOC = AW38; # Bank 100 - MGTREFCLK1N_100
NET  U2_MGTREFCLK0_101_P       LOC = AU37; # Bank 101 - MGTREFCLK0P_101
NET  U2_MGTREFCLK0_101_N       LOC = AU38; # Bank 101 - MGTREFCLK0N_101
NET  U2_MGTREFCLK1_101_P       LOC = AR37; # Bank 101 - MGTREFCLK1P_101
NET  U2_MGTREFCLK1_101_N       LOC = AR38; # Bank 101 - MGTREFCLK1N_101
NET  U2_MGTREFCLK0_103_P       LOC = AF35; # Bank 103 - MGTREFCLK0P_103
NET  U2_MGTREFCLK0_103_N       LOC = AF36; # Bank 103 - MGTREFCLK0N_103
NET  U2_MGTREFCLK1_103_P       LOC = AD35; # Bank 103 - MGTREFCLK1P_103
NET  U2_MGTREFCLK1_103_N       LOC = AD36; # Bank 103 - MGTREFCLK1N_103
NET  U2_MGTREFCLK0_104_P       LOC = AB35; # Bank 104 - MGTREFCLK0P_104
NET  U2_MGTREFCLK0_104_N       LOC = AB36; # Bank 104 - MGTREFCLK0N_104
NET  U2_MGTREFCLK1_104_P       LOC =  Y35; # Bank 104 - MGTREFCLK1P_104
NET  U2_MGTREFCLK1_104_N       LOC =  Y36; # Bank 104 - MGTREFCLK1N_104
NET  U2_MGTREFCLK0_111_C_P     LOC =  AU8; # Bank 111 - MGTREFCLK0P_111
NET  U2_MGTREFCLK0_111_C_N     LOC =  AU7; # Bank 111 - MGTREFCLK0N_111
NET  U2_MGTREFCLK1_111_C_P     LOC =  AR8; # Bank 111 - MGTREFCLK1P_111
NET  U2_MGTREFCLK1_111_C_N     LOC =  AR7; # Bank 111 - MGTREFCLK1N_111
NET  U2_MGTREFCLK0_114_C_P     LOC = AB10; # Bank 114 - MGTREFCLK0P_114
NET  U2_MGTREFCLK0_114_C_N     LOC =  AB9; # Bank 114 - MGTREFCLK0N_114
NET  U2_MGTREFCLK1_114_C_P     LOC =  Y10; # Bank 114 - MGTREFCLK1P_114
NET  U2_MGTREFCLK1_114_C_N     LOC =   Y9; # Bank 114 - MGTREFCLK1N_114

##
## GTH REFCLKS:
##
NET  U2_MGTREFCLK_106_P        LOC =  R41; # Bank 106 - MGTREFCLKP_106
NET  U2_MGTREFCLK_106_N        LOC =  R42; # Bank 106 - MGTREFCLKN_106
NET  U2_MGTREFCLK_107_P        LOC =  J41; # Bank 107 - MGTREFCLKP_107
NET  U2_MGTREFCLK_107_N        LOC =  J42; # Bank 107 - MGTREFCLKN_107
NET  U2_MGTREFCLK_108_P        LOC =  E41; # Bank 108 - MGTREFCLKP_108
NET  U2_MGTREFCLK_108_N        LOC =  E42; # Bank 108 - MGTREFCLKN_108
NET  U2_MGTREFCLK_116_P        LOC =   R4; # Bank 116 - MGTREFCLKP_116
NET  U2_MGTREFCLK_116_N        LOC =   R3; # Bank 116 - MGTREFCLKN_116
NET  U2_MGTREFCLK_117_P        LOC =   J4; # Bank 117 - MGTREFCLKP_117
NET  U2_MGTREFCLK_117_N        LOC =   J3; # Bank 117 - MGTREFCLKN_11
NET  U2_MGTREFCLK_118_P        LOC =   E4; # Bank 118 - MGTREFCLKP_118
NET  U2_MGTREFCLK_118_N        LOC =   E3; # Bank 118 - MGTREFCLKN_118
```

```
##
## INTERLOCKEN AIRMAX CONNECTOR FLOW CONTROL:
##
NET  U2_AMR4_FC_LS_SYNC         LOC =  C12; # Bank  35 - IO_L0P_35
NET  U2_AMR4_FC_LS_DATA         LOC =  C11; # Bank  35 - IO_L0N_35
NET  U2_AMR4_FC_LS_CK           LOC =  A13; # Bank  35 - IO_L1P_35

NET  U2_AMH4_FC_LS_SYNC         LOC =  A12; # Bank  35 - IO_L1N_35
NET  U2_AMH4_FC_LS_DATA         LOC =  B11; # Bank  35 - IO_L2P_SM0P_35
NET  U2_AMH4_FC_LS_CK           LOC =  A10; # Bank  35 - IO_L2N_SM0N_35

##
## INTERLOCKEN AIRMAX CONNECTOR I/O CONTROL:
##
NET  U2_AMH4_IO7                LOC =  G34; # Bank  25 - IO_L14P_25
NET  U2_AMH4_IO6               LOC =  F34; # Bank  25 - IO_L14N_VREF_25
NET  U2_AMH4_IO5              LOC =  R33; # Bank  25 - IO_L15P_SM15P_25
NET  U2_AMH4_IO4              LOC =  P33; # Bank  25 - IO_L15N_SM15N_25
NET  U2_AMH4_IO3                LOC =  J34; # Bank  25 - IO_L17P_25
NET  U2_AMH4_IO2                LOC =  H34; # Bank  25 - IO_L17N_25
NET  U2_AMH4_IO1                LOC =  R31; # Bank  25 - IO_L18P_GC_25
NET  U2_AMH4_IO0                LOC =  R32; # Bank  25 - IO
```

Appendix E

ML630C Schematic Page List

Table E-1: **ML630C Schematic Page List**

Page No.	Contents	Ref. Des. on This Page	Figure 1-2 Callout No.
1	Title and Disclaimer	NA	
2	PGA U1 Block Diagram	NA	
3	PGA U2 Block Diagram	NA	
4	JTAG Chain Diagram	NA	
Begin Circuitry Shared by Both FPGA U1 and FPGA U2			
5	SystemACE IC with CompactFlash Socket	U47, U46	18
6	Embedded JTAG USB Mini-B connector	J20	16
6	Embedded JTAG CY7C68013A and XC2C256	U48, U45	17
7	Embedded JTAG 24LC00T EEPROM, MAX6412UK22 POR, DS2411 ESN and support circuitry	U39, U40, U37	NA
8	Board-wide fixed 3.3V (6A) TI PTH12000WAH voltage regulator	U6	15
9	SMA differential clock inputs, four pairs.	J167/8, J169/J170, J171/2, J9/J10	37, 38, 39, 40
9	Each pair drives a 1-to-2 3.3V LVPECL ICS85311AMLF clock buffer	U96, U97, U98, U99	37, 38, 39, 40
10	I^2C controlled clock generation: I^2C bus TI TXS0104EDR level-shifter, I^2C 1-to-8 mux PCS9548APW, M24C03 EEPROM	U128, U31, U59	47
10	Four I^2C programmable Si570BAB000544DG 10 MHz–810 MHz 3.3V LVDS clock sources (bottom of board)	U43, U44, U51, U52	41
10	Each Si570 clock source drives a 1-to-2 3.3V LVPECL ICS85311AMLF clock buffer (bottom of board)	U53, U54, U55, U56	41
11	Pg.10 3.3V LVPECL clock buffer resistor terminations, Pg.12, 13 ICS85356AGILF mux input resistor terminations	NA	NA
12	Three dual 2-to-1 ICS85356AGILF 3.3V LVDS in, 3.3V LVPECL out differential clock mux	U102, U115, U116	45a
12	Differential SMA input pair to ICS854S006AGILF 1-to-6 3.3V LVDS clock buffer (bottom of board)	U126, J124, J125	45a, 43

Table E-1: **ML630C Schematic Page List**

Page No.	Contents	Ref. Des. on This Page	Figure 1-2 Callout No.
13	Three dual 2-to-1 ICS85356AGILF 3.3V LVDS in, 3.3V LVPECL out differential clock mux	U120, U121, U122	45b
13	Differential SMA input pair to ICS854S006AGILF 1-to-6 3.3V LVDS clock buffer (bottom of board)	U127, J126, J127	45b, 44
14	Two TI SN65LVCP408PAP 8x8 differential clock cross-point switch ICs	U57, U58	42
14	Two 1-to-2 3.3V LVPECL ICS85311AMLF clock buffers (bottom of board)	U113, U114	46
	Begin FPGA U1 Specific Circuitry Pages		
15	FPGA U1 USB Mini-B connector and SI CP2103GM USB-to-UART Bridge IC	J54, U26	24
15	I^2C programmable Si570BAB000544DG 10 MHz-810 MHz 3.3V LVDS clock source (bottom of board)	U64	46
15	Driving ICS854S006AGILF 1-to-6 3.3V LVDS clock buffer (top of board)	U13	46
16	FPGA U1 SITIME SIT9102AI-243N25E200.0000 fixed 200 MHz 2.5V LVDS clock source (bottom of board)	U22	25
16	FPGA U1 PROG. P.B. switch, INIT and DONE LEDs	SW5, DS20, DS56	21
16	FPGA U1 4 user P.B. and 1 user 8-pole DIP switch, eight user LEDs, 2X6 user GPIO male header, 2X5 VGA video debug header	SW4,6,8,9, SW7; DS10-DS17, J285, J16	23a, 23b
17	FPGA U1 System Monitor power filter and thermal diode test points	J183, J119	NA
18	FPGA U1 MGTX Banks 100, 101, 102; MGTREFCLKXP/N_101; Part of 24-channel GTX U1-to-U2 interface	U1	1
19	FPGA U1 MGTX Banks 103, 104, 105; MGTREFCLKXP/N_104; Part of 24-channel GTX U1-to-U2 interface	U1	1
20	FPGA U1 MGTH Banks 106, 107, 108; FCI AirMax "Interlaken" male plug connector P3	P3, U1	1, 32
21	FCI AirMax "Interlaken" female receptacle connector J3; Two P3/J3 control signal TXB0104DR level-shifters	J3, U107, U108	32
22	FPGA U1 MGTH Banks 116, 117, 118; "Interlaken" P3/J3 connectivity	U1	1
23	FPGA U1 MGTX Banks 110, 111, 112; FCI AirMax "Interlaken" male plug connector P2	P2	34
24	FCI AirMax "Interlaken" female receptacle connector J2; Two P2/J2 control signal TXB0104DR level-shifters	J2, U105, U106	34
25	FCI AirMax "Interlaken" Female receptacle connector J1 and J2 series 0.1 µF RX capacitors	NA	NA

Table E-1: **ML630C Schematic Page List**

Page No.	Contents	Ref. Des. on This Page	Figure 1-2 Callout No.
26	FPGA U1 MGTX Banks 113, 114, 115; FCI AirMax "Interlaken" male plug connector P1	U1	31
27	FCI AirMax "Interlaken" female receptacle connector J1; Two P1/J1 control signal TXB0104DR level-shifters	J1, U103, U104	31
28	FPGA U1 Bank 28 (P.B. inputs) and Bank 38 (DIP SW inputs)	U1	1
29	BLANK - Placeholder page	NA	NA
30	FPGA U1 Bank 27 no-connect and Bank 37 no-connect	U1	NA
31	BLANK - Placeholder page	NA	NA
32	FPGA U1 Bank 0 (Configuration) and Bank RSVD	U1	1
33	FPGA U1 Bank 31 FMC1 Conn. J290 P/N pairs HB[18:00]	U1	1
33	FPGA U1 Bank 21 FMC1 Conn. J290 P/N pairs HB[21:20], HA[23:17], U1_AMH2_IO[7:0],U1_AMH1_IO[7:0]	U1	1
34	FPGA U1 Bank 22 U1_B34_LVDS_[19:00]_P/N; Bank 23 U1_B33_LVDS_[19:00]_P/N	U1	1
35	FPGA U1 Bank 24 U1_B32_LVDS_[19:00]_P/N	U1	1
35	FPGA U1 Bank 25 U1_USER_IO_[6:1], U1_USER_LED_8:1], U1_AMH3_IO[7:0], U1_VGA_IF, U1_LVDS_OSC_P/N	U1	1
36	FPGA U1 Bank 26 U1_B26_LVDS_[19:00]_P/N; Bank 32 FMC1 Connector LA[33:17]	U1	1
37	FPGA U1 Bank 33 FMC1 Conn. J290 P/N pairs LA[16:00], FMC1_CLK1_M2C_P/N	U1	1
37	FPGA U1 Bank 34 FMC1 Conn. J290 P/N pairs HA[16:00], FMC1_CLK0_M2C_P/N	U1	1
38	FPGA U1 Bank 35 U1_AMH3_FC_LS_IF, U1_AMH2_FC_LS_IF, U1_AMH1_FC_LS_IF, U1_SDA/SCL_MAIN, U1_SI570_5_P/N, U1_SI570_4_P/N, U1_USB_UART_IF	U1	1
38	FPGA U1 Bank 36 no-connect	U1	1
39	FMC1 Connector J290 Row A, B and C	J290	48
40	FMC1 Connector J290 Row D; FMC1 JTAG bypass header J51; U1 FPGA video debug 2x6 male header J16 with color scaling resistors	J16, J290	23, 48
41	FMC1 Connector J290 Row E, F and G	J290	48
42	FMC1 Connector J290 Row H, J and K	J290	48
43	FMC1 Connector J290 GND	J290	48
44	FPGA U1 Bank MGTHAVCCPLL_L and R power; FPGA U1 Bank MGTHAVTT_L and R power	U1	1

Table E-1: **ML630C Schematic Page List**

Page No.	Contents	Ref. Des. on This Page	Figure 1-2 Callout No.
45	FPGA U1 Bank MGTHAVCCRX_L and R power; FPGA U1 Bank MGTHAVCC_L and R power	U1	1
46	FPGA U1 Bank MGTHAGND_L and R power	U1	1
47	FPGA U1 Bank MGTAVCC_LN, LS, RN and RS power	U1	1
48	FPGA U1 Bank MGTAVTT_LN, LS, RN and RS power	U1	1
49	FPGA U1 Bank GND1 and GND2	U1	1
50	FPGA U1 Bank V_{CCINT} and V_{CCAUX}	U1	1
51	FPGA U1 12V input power connectors J122 and J141, U1 fan power header J221	J122,J141,J221	4
52	U1/U2 core power UCD9240 controller U8 CD74BC4051 temperature mux U28	U28	7
52	U1 MGTH power UCD9240 controller U19 CD74BC4051 temperature mux U15	U15	7
52	U1/U2 MGTX power UCD9240 controller U32 CD74BC4051 temperature mux U27	U27	7
53	U1/U2 core power UCD9240 controller U8	U8	7
54	U1 core power V_{CCINT} U10, U41 TI PTD08A020W 40A power circuit with series current sense resistors and U16, U42 op amps	U10, U16, U41, U42	9
55	U1 core power V_{CCAUX} U12 TI PTD08A020W 20A power circuit with series current sense resistors and U17 op amp	U12, U17	9
56	U2 core power V_{CCINT} U81, U82 TI PTD08A020W 40A power circuit with series current sense resistors and U85, U86 op amps	U81, U82, U85, U86	12
57	U2 core power V_{CCAUX} U83 TI PTD08A020W 20A power circuit with series current sense resistors and U87 op amp	U83, U87	12
58	U1 MGTH power TI UCD9240 controller U19	U19	7
59	U1 MGTH power MGTHAVCC U3 TI PTH08A010W 10A power circuit with series current sense resistors and U33 op amp	U3, U33	11
60	U1 MGTH power MGTHAVCCRX U14 TI PTH08A006W 6A power circuit with series current sense resistors and U34 op amp	U14, U34	11
61	U1 MGTH power MGTHAVTT U20 TI PTH08A006W 6A power circuit with series current sense resistors and U35 op amp	U20, U35	11
62	U1 MGTH power MGTHAVCCPLL U21 TI PTH08A006W 6A power circuit with series current sense resistors and U36 op amp	U21, U36	11

Table E-1: **ML630C Schematic Page List**

Page No.	Contents	Ref. Des. on This Page	Figure 1-2 Callout No.
63	U1/U2 MGX power TI UCD9240 controller U32	U32	7
64	U1 MGTX power MGTXAVCC U4 TI PTH08A010W 10A power circuit with series current sense resistors and U29 op amp	U4, U29	10
65	U1 MGTX power MGTXAVTT U5 TI PTH08A010W 10A power circuit with series current sense resistors and U30 op amp	U5, U30	10
66	U2 MGTX power MGTXAVCC U73 TI PTH08A010W 10A power circuit with series current sense resistors and U94 op amp	U73, U94	13
67	U2 MGTX power MGTXAVTT U74 TI PTH08A010W 10A power circuit with series current sense resistors and U95 op amp	U74, U95	13
68	BLANK - Placeholder page	NA	NA
	Begin FPGA U2 Specific Circuitry Pages		
69	FPGA U2 SI CP2103GM USB-to-UART Bridge IC	U79	29
69	I2C programmable Si570BAB000544DG 10 MHz–810 MHz 3.3V LVDS clock source (bottom of board)	U65	46
69	driving ICS854S006AGILF 1-to-6 3.3V LVDS clock buffer (top of board)	U18	46
70	FPGA U2 SITIME SIT9102AI-243N25E200.0000 fixed 200 MHz 2.5V LVDS clock source (bottom of board)	U63	30
70	FPGA U2 PROG. P.B. switch, INIT and DONE LEDs	SW11, DS54, DS29	26
70	FPGA U2 4 USER P.B. and 1 user 8-pole DIP switch, eight user LEDs, 2X6 user GPIO male header, 2X5 VGA video debug header	SW12-15, SW16; DS30-DS35,DS37,DS38; J103, J110	27,28
71	FPGA U2 System Monitor power filter and thermal diode test points	J76, J77	NA
72	FPGA U2 MGTX Banks 100, 101, 102; MGTREFCLKXP/N_101; Part of 24-channel GTX U1-to-U2 interface	U2	2
73	FPGA U1 MGTX Banks 103, 104, 105; MGTREFCLKXP/N_104; Part of 24-channel GTX U1-to-U2 interface	U2	2
74	FPGA U2 MGTH Banks 106, 107, 108; FCI AirMax "Interlaken" male plug connector P4	P4, U2	35, 2
75	FCI AirMax "Interlaken" Female receptacle connector J4; Two P4/J4 control signal TXB0104DR level-shifters	J4, U109, U110	35
76	FPGA U2 MGTH Banks 116, 117, 118; "Interlaken" P4/J4 connectivity	U2	2
77	FCI AirMax "Interlaken" female receptacle connector J4 series 0.1 µF RX capacitors	NA	NA

Table E-1: **ML630C Schematic Page List**

Page No.	Contents	Ref. Des. on This Page	Figure 1-2 Callout No.
78	FPGA U2 MGTX Banks 110, 111, 112; FCI AirMax "Interlaken" male plug connector P2	U2	35
79	FPGA U2 MGTX Banks 113, 114, 115	U2	2
80	FPGA U2 Bank 28 (P.B. inputs) and Bank 38 (DIP SW inputs)	U2	2
81	BLANK - Placeholder page	NA	NA
82	FPGA U2 Bank 27 no-connect and Bank 37 no-connect	U2	
83	BLANK - Placeholder page	NA	NA
84	FPGA U2 Bank 0 (Configuration) and Bank RSVD	U2	2
85	FPGA U2 Bank 31 FMC2 Conn. J104 P/N pairs HA[16:00]; FMC2_CLK0_M2C_P/N	U2	2
85	FPGA U2 Bank 21 FMC2 Conn. J104 P/N pairs LA[16:00]; FMC2_CLK1_M2C_P/N	U2	2
86	FPGA U2 Bank 22 FMC2 Conn. J104 P/N pairs LA[33:17]	U2	2
86	FPGA U2 Bank 23 FMC2 Conn. J104 P/N pairs HB[18:00]	U2	2
87	FPGA U2 Bank 24 FMC2 Conn. J104 P/N pairs HB[21:20]; HA[23:17]; U2_LVDS_OSC_P/N	U2	2
87	FPGA U2 Bank 25 U2_USER_IO_[6:1], U2_USER_LED_[8:1], U1_AMH4_IO[7:0], U2_VGA_IF	U2	2
88	FPGA U2 Bank 26 U1_B26_LVDS_[19:00]_P/N; Bank 32 U1_B32_LVDS_[19:00]_P/N	U2	2
89	FPGA U2 Bank 33 U1_B33_LVDS_[19:00]_P/N; Bank 34 U1_B34_LVDS_[19:00]_P/N	U2	2
90	FPGA U2 Bank 35 U2_AMH4_FC_LS_IF, U2_SDA/SCL_MAIN, U2_SI570_5_P/N, U2_SI570_4_P/N, U2_USB_UART_IF; U2_GTHREFCLK_LS_SEL[1:0]	U2	2
90	FPGA U2 Bank 36 no-connect	U2	2
91	FMC2 Connector J104 Row A, B and C	J104	49
92	FMC2 Connector J104 Row D; FMC2 JTAG bypass header J101; U2 FPGA video debug 2x6 male header J110 with color scaling resistors	J104, J110	28, 49
93	FMC2 Connector J104 Row E, F and G	J104	49
94	FMC2 Connector J104 Row H, J and K	J104	49
95	FMC2 Connector J104 GND	J104	49
96	FPGA U2 Bank MGTHAVCCPLL_L and R power; FPGA U2 Bank MGTHAVTT_L and R power	U2	2
97	FPGA U2 Bank MGTHAVCCRX_L and R power; FPGA U2 Bank MGTHAVCC_L and R power	U2	2

Table E-1: **ML630C Schematic Page List**

Page No.	Contents	Ref. Des. on This Page	Figure 1-2 Callout No.
98	FPGA U2 Bank MGTHAGND_L and R power	U2	2
99	FPGA U2 Bank MGTAVCC_LN, LS, RN and RS power	U2	2
100	FPGA U2 Bank MGTAVTT_LN, LS, RN and RS power	U2	2
101	FPGA U2 Bank GND1 and GND2	U2	2
102	FPGA U2 Bank V_{CCINT} and V_{CCAUX}	U2	2
103	FPGA U2 12V input power connectors J75 and J102, U2 fan power header J105	J75, J102, J105	4
104	U2 MGTH UCD9240 controller U77 CD74BC4051 temperature mux U60	U60	7
105	U2 MGTH power TI UCD9240 controller U77	U77	7
106	U2 MGTH power MGTHAVCC U72 TI PTH08A010W 10A power circuit with series current sense resistors and U90 op amp	U72, U90	14
107	U2 MGTH power MGTHAVCCRX U67 TI PTH08A006W 6A power circuit with series current sense resistors and U9 op amp	U67, U91	14
108	U2 MGTH power MGTHAVTT U68 TI PTH08A006W 6A power circuit with series current sense resistors and U92 op amp	U68, U92	14
109	U2 MGTH power MGTHAVCCPLL U69 TI PTH08A006W 6A power circuit with series current sense resistors and U93 op amp	U69, U93	14
110	ML630 Mechanical Components	NA	NA
111	ML630 Board FPGA U1 Power Block Diagram	NA	NA
112	ML630 Board FPGA U2 Power Block Diagram	NA	NA
113	ML630 REV B to REV C change list	NA	NA

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Appendix F

Documents and Resources

Documents

Links to specific documents relevant to Virtex®-6 devices, the ML630 Virtex-6 HXT Optical Transmission Network Evaluation Board, and intellectual property are listed here:

1. DS080, *System ACE CompactFlash Solution*.
2. DS150, *Virtex-6 Family Overview*
3. DS152, *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics*
4. UG360, *Virtex-6 FPGA Configuration User Guide*
5. UG361, *Virtex-6 FPGA SelectIO Resources User Guide*
6. UG362, *Virtex-6 FPGA User Guide: Clocking Resources*
7. UG364, *Virtex-6 FPGA Configurable Logic Block User Guide*
8. UG365, *Virtex-6 FPGA Packaging and Pinout Specifications*
9. UG366, *Virtex-6 FPGA GTX Transceivers User Guide*
10. UG370, *Virtex-6 FPGA System Monitor User Guide*
11. UG371, *Virtex-6 FPGA GTH Transceivers User Guide*
12. DS581, *XPS External Peripheral Controller (EPC) Data Sheet*
13. DS606, *XPS IIC Bus Interface (v2.00a) Data Sheet*

Other documents associated with Xilinx devices, design tools, intellectual property, boards, and kits are available at the Xilinx documentation website at:

http://www.xilinx.com/support/documentation/index.htm

Webpages

General information for the ML630 board and evaluation kit is available at:

http://www.xilinx.com/products/boards-and-kits/EK-V6-ML630-G.htm

View and download the latest ML630 board schematics, bill of materials, reference design files, and user guides from:

http://www.xilinx.com/products/boards/ml630/reference_designs.htm

Product Support

The Xilinx product support website provides access to product support resouces including contact information, training, forums, access to an answer record database, and more. Go to:

http://www.xilinx.com/support.