INVENTEK SYSTEMS

ISM43362-B81
Wi-Fi SiP Module
eS-WiFi™
802.11 b/g/n
Data Sheet

Table of Contents

1 GENERAL DESCRIPTION

The Inventek ISM43362-B81 is an 802.11 b/g/n Wi-Fi Radio SiP which is designed for embedded wireless solutions and offers a cost-effective high performance Broadcom radio device (BCM43362) packaged in an 81 pin (8.1mm x 8.6 mm) ball grid array. It includes standards-based wired and wireless technologies to enable IP infrastructures for smart grid, smart home, security, building automation, toys, robots, remote health and wellness monitoring and other IoT and M2M applications.

The SiP is based on IEEE802.11 b/g/n antenna diversity single-stream align technology. The solution helps to reduce development time, lower manufacturing costs, save board space, and ease certification.

Summary of Key Features:

- 802.11 b/g/n compliant based on Broadcom MAC/Baseband/Radio device.
- Diverse serial interface — SDIO v2.0, gSPI
- On-chip functionality Single-chip — MAC/BB/RF
- Frequency Band — 2.4 GHz
- Network Standard — 802.11b, 802.11g, 802.11n (single stream)
- Modulation Modes — CCK and OFDM with BPSK, QPSK, 16 QAM, 64QAM
- Hardware Encryption — WEP, WPA/WPA2
- Supported Data Rates — IEEE 802.11b 1 – 11 Mbps
IEEE 802.11g 6 – 54 Mbps
IEEE 802.11n (2.4 GHz) 7.2 – 72.2 Mbps
- Advanced 1x1 802.11n features — Full/Half Guard Interval
- Operating Temperature — -30℃ to 85℃

Typical Applications:

- PDA, Pocket PC, computing devices.
- Building automation and smart energy control.
- Industrial sensing and remote equipment monitoring.
- Warehousing, logistics and freight management.
- PC and gaming peripherals.
- Printers, scanners, alarm and video systems.
- Medical applications including patient monitoring and remote diagnostics.

2 PART NUMBER DETAIL DESCRIPTION

2.1 *Ordering Information*

Device	Description	Ordering Number
ISM43362-B81	802.11 SIP Module based on Broadcom BCM43362	ISM43362-B81
ISM43362-B81-EVB	SDIO Evaluation Board	ISM43362-B81-EVB

3 GENERAL FEATURES

- Based on the Broadcom BCM43362 MAC/Baseband/Radio device.
- Supports Broadcom WICED SDK for “Virtual WICED” designs.
- IEEE 802.11n D7.0 -OFDM-72.2 Mbps -single stream w/20 MHz, Short GI
- IEEE 802.11g (OFDM 54 Mbps)
- IEEE 802.11b (DSSS 11Mbps)
- IEEE 802.11i (Security)
    - WPA (Wi-Fi Protected Access) –PSK/TKIP
    - WPA2 (Wi-Fi Protected Access 2)- AES/CCMP/802.1x Authentication
- Inputs +3.3 V tolerant
- Lead Free Design which is compliant with ROHS requirements.
- EMI/EMC Metal Shield recommended for best RF performance in noisy environments and to accommodate for lower RF emissions/signature for easier FCC compliance.

3.1 *Limitations*

Inventek Systems products are not authorized for use in safety-critical applications (such as life support) where a failure of the Inventek Systems product would reasonably be expected to cause severe personal injury or death.

4 COMPLEMENTARY DOCUMENTATION

4.1 *Inventek Systems*

- Evaluation Board
  - ISM43362-B81 SDIO Evaluation Board Specification
- Firmware (NDA/ SLA required)

5 SPECIFICATIONS

5.1 *Module Architecture / Block Diagram*

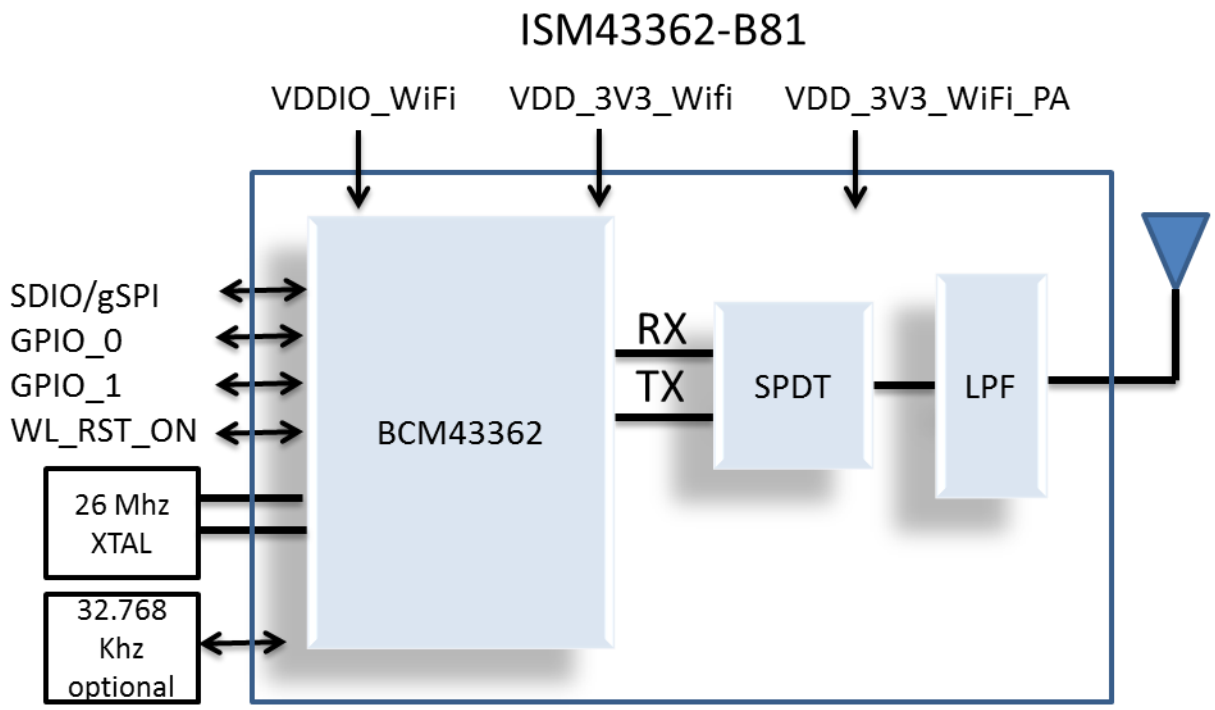


Figure 1 Inventek's ISM43362-B81 General Block Diagram

5.2 *Environmental Specifications*

Item	Description
Operating temperature range	-30 deg. C to +85 deg. C
Storage temperature range	-40 deg. C to +85 deg. C
Humidity	95% max non-condensing

Note 1: The optimal RF performance specified in this data sheet is only guaranteed for temperatures from -10°C to +65°C.

6 HARDWARE ELECTRICAL SPECIFICATIONS

6.1 *Recommended Operating Ratings*

Symbol	Min.	Typ.	Max.	Unit.
VDD_3V3_WIFI	3.0	3.3	3.6	V
VDD_3V3_WIFI_PA	3.0	3.3	3.6	V
VDDIO_WIFI	3.0	3.3	3.6	V
Voltage Ripple	+/- 2% max values not exceeding operating voltage			

7 Power Consumption

Condition: 250C, VDD_3V3_WiFi=VDD_3V3_WiFi_PA=VDDIO_WiFi=3.3V. .

Item	Condition	Min	Nom	Max	Unit
Tx mode(11b Max current)	11Mbps		345	410	mA
Tx mode(11g Max current)	54Mbps		250	310	mA
Tx mode(11n Max current)	MCS7		210	270	mA
Rx mode(Rx @Max gain)	11b (11Mbps)		115	150	mA
	11g (54Mbps)		115	150	mA
	11n (MCS7)		115	150	mA

8 Wi-Fi RF Specification

8.1 *RF Specification*

Conditions: VDD=3.3V; VDDIO=3.3V; TEMP: 25°C

Feature	Description
WLAN Standard	IEEE 802.11b/g/n, Wi-Fi compliant
Frequency Range	2.400 GHz ~ 2.497 GHz (2.4 GHz ISM Band)
Number of Channels	Ch1 ~ Ch14
Modulation	802.11 g/n : OFDM /64-QAM,16-QAM, QPSK, BPSK
	802.11b : CCK, DQPSK, DBPSK
Output Power	802.11b /11Mbps : 17 dBm ± 1.5 dB
	802.11g /54Mbps: 13 dBm ± 1.5 dB
	802.11n /72Mbps: 11 dBm ± 1.5 dB
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -86 dBm, typical
	- MCS=1 PER @ -85 dBm, typical
	- MCS=2 PER @ -85 dBm, typical
	- MCS=3 PER @ -84 dBm, typical
	- MCS=4 PER @ -80 dBm, typical
	- MCS=5 PER @ -78 dBm, typical
	- MCS=6 PER @ -72 dBm, typical
	- MCS=7 PER @ -69 dBm, typical
Receive Sensitivity (11g) @10% PER	- 6Mbps PER @ -89 dBm, typical
	- 9Mbps PER @ -88 dBm, typical
	- 12Mbps PER @ -88 dBm, typical
	- 18Mbps PER @ -87 dBm, typical
	- 24Mbps PER @ -83 dBm, typical
	- 36Mbps PER @ -80 dBm, typical
	- 48Mbps PER @ -75 dBm, typical
	- 54Mbps PER @ -72 dBm, typical
Receive Sensitivity (11b) @10% PER	- 1Mbps PER @ -93 dBm, typical
	- 2Mbps PER @ -91 dBm, typical
	- 5.5Mbps PER @ -89 dBm, typical
	- 11Mbps PER @ -87 dBm, typical
Data Rates	802.11b : 1, 2, 5.5, 11Mbps
	802.11g : 6, 9, 12, 18, 24, 36, 48, 54Mbps
Data Rate (20MHz ,Long GI,800ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps

Data Rate (20MHz ,short GI,400ns)	802.11n : 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps
Maximum Receive Input Level	802.11b : -10 dBm
	802.11g : -10 dBm

8.2 *802.11b Transmit*

802.11b Transmit					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Transmit output power level	1M/2M/5.5M/11M	15	17	19	dBm
Transmit center frequency tolerance		-25	0	25	ppm
Transmit spectrum mask	Fc-22MHz<F<Fc-11MHz & Fc+11MHz<F<Fc+22MHz(1/2/5.5/11Mbps; channel 1~13)			-30*	dBr
	F<Fc-22MHz & F>Fc+22MHz(1/2/5.5/11Mbps; channel 1~13)			-50*	dBr
Transmit power -on	10% ~ 90 %		0.3	2*	us
Transmit power -down	90% ~ 10 %		1.5	2*	us
Transmit modulation accuracy	1/2/5.5/11 Mbps		-17	-10	dB

* indicates IEEE802.11 specification

8.3 *802.11g Transmit*

802.11g Transmit					
Item	Condition	Min.	Typ.	Max.	Unit
Transmit output power level	6M/9M/12M/18M/24M/36M/48M/54M	11	13	15	dBm
					dBm
					dBm
Transmit center frequency tolerance		-20	0	20	ppm
Transmit modulation accuracy	6Mbps			-5*	dB
	9Mbps			-8*	dB
	12Mbps			-10*	dB
	18Mbps			-13*	dB
	24Mbps			-16*	dB
	36Mbps			-19*	dB
	48Mbps			-22*	dB
	54Mbps		-30	-25*	dB
Transmit spectrum mask	@ 11MHz			-20*	dBr
	@ 20MHz			-28*	dBr
	@ 30MHz			-40*	dBr

8.4 *802.11n Transmit*

802.11n Transmit					
Item	Condition	Min.	Typ.	Max.	Unit
Transmit output power level	HT20 MCS 0~7	9	11	13	dBm
					dBm
					dBm
Transmit center frequency tolerance	HT20 MCS 0~7	-20	0	20	ppm
Transmit modulation accuracy	HT20, MCS0~7		-30	-27*	dB
					dB
Transmit Spectrum mask	@ 11MHz			-20*	dBr
	@ 20MHz			-28*	dBr
	@ 30MHz			-45*	dBr

8.5 *802.11b Receiver*

802.11 b Receiver					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Receiver minimum input level sensitivity (PER< 8 %)	1Mbps		-90	-80*	dBm
	2Mbps		-90	-80*	dBm
	5.5Mbps		-88	-76*	dBm
	11Mbps		-85	-76*	dBm
Receiver maximum input level sensitivity (PER< 8 %)	1/2/5.5/11 Mbps			-10*	dBm

* indicates IEEE802.11_2012 specification

8.6 *802.11g Receiver*

802.11g Receiver					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Receiver minimum input level sensitivity (PER<10 %)	6Mbps		-85	-82*	dBm
	9Mbps		-85	-81*	dBm
	12Mbps		-85	-79*	dBm
	18Mbps		-84.5	-77*	dBm
	24Mbps		-82	-74*	dBm
	36Mbps		-78.5	-70*	dBm
	48Mbps		-74	-66*	dBm
	54Mbps		-70	-65*	dBm
Receiver maximum input level (PER<10%)	6/9/12/18/24/36/48/54			-20*	dBm

* indicates IEEE802.11_2012 specification

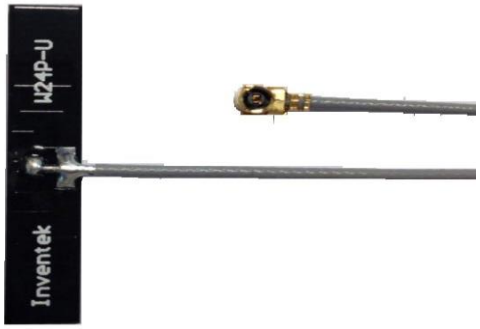
8.7 *802.11n Receiver*

802.11n Receiver					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Receiver minimum input level sensitivity (PER<10 %)	HT20, MCS0		-85	-82*	dBm
	HT20, MCS1		-83	-79*	dBm
	HT20, MCS2		-81	-77*	dBm
	HT20, MCS3		-79	-74*	dBm
	HT20, MCS4		-76	-70*	dBm
	HT20, MCS5		-73	-66*	dBm
	HT20, MCS6		-70	-65*	dBm
	HT20, MCS7		-68	-64*	dBm
Receiver maximum input level (PER<10%)	MSC0~MSC7			-20*	dBm

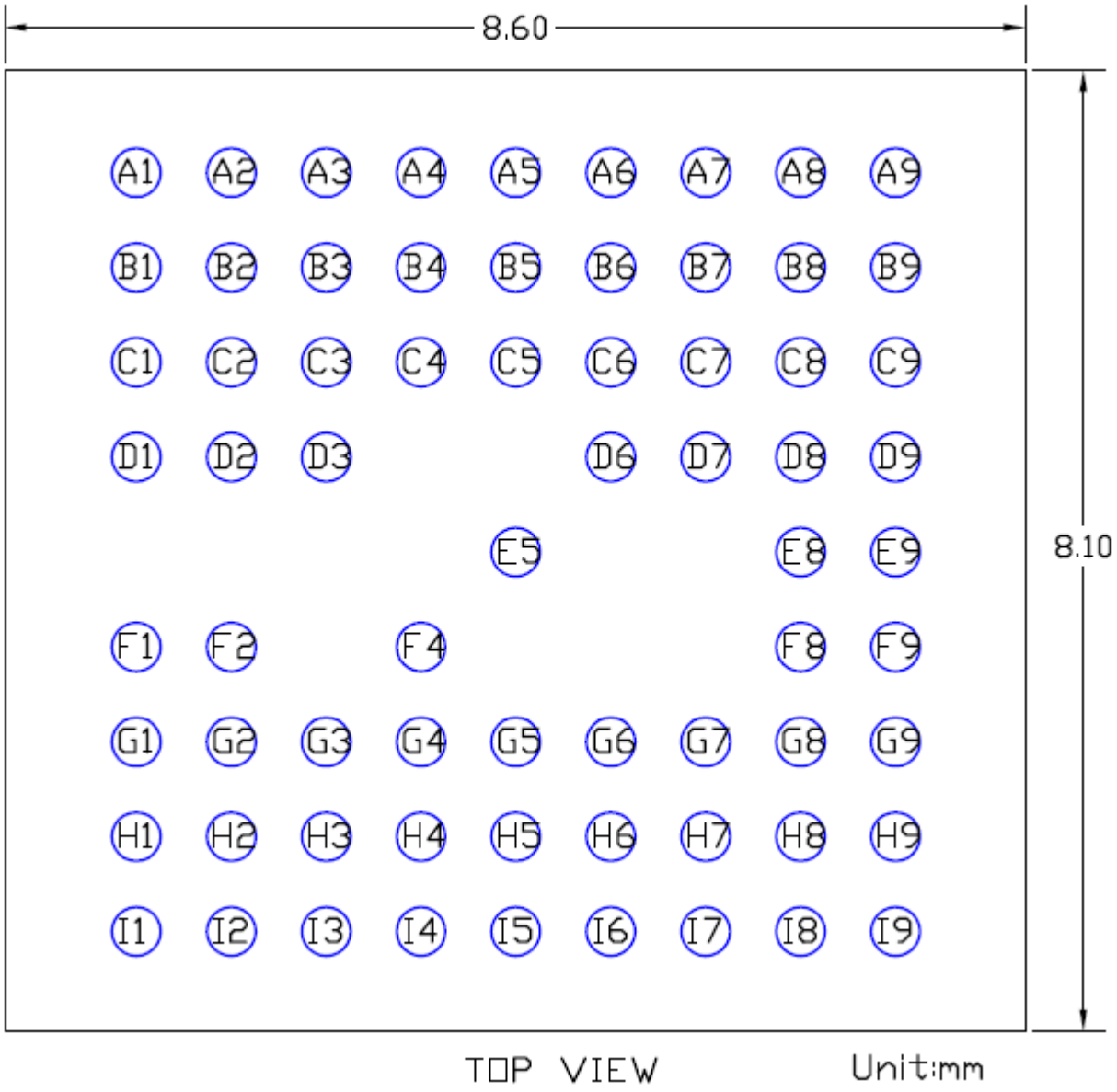
* indicates IEEE802.11_2012 specification

8.8 *External Antenna Option*

The Inventek W24P-U PCB antenna can be found on the Inventek Website.



9 ISM43362-B81 Module's Dimensions Top View (mm)



.

Figure 2 Module Dimensions- Top View

10 ISM43362-B81 Pin Definition

Pin Number	Pin Name	type	Power	Description
A1	S_GND	I/O	-	Ground for DC-DC
A2	VDD_3V3_Wifi	P	-	WiFi power supply
A3	GND	-	-	Ground
A4	GND	-	-	Ground
A5	GND	-	-	Ground
A6	GND	-	-	Ground
A7	ANT	I/O	-	RF transmitter output and RF receiver input
A8	GND	-	-	Ground
A9	GND	-		Ground
B1	S_GND	I/O	-	Ground for DC-DC
B2	S_GND	I/O	-	Ground for DC-DC
B3	VDD_3V3_WiFi	P	-	Wi-Fi power supply
B4	GND	-	-	Ground
B5	VDD_3V3_WiFi_PA			Wi-Fi PA power supply
B6	GND	-	-	Ground
B7	GND	-	-	Ground
B8	GND	-	-	Ground
B9	GND	-	-	Ground
C1	S_GND	I/O	-	Ground for DC-DC
C2	S_GND	I/O	-	Ground for DC-DC
C3	GND	-	-	Ground
C4	RF_SW_CTRL_ANT1	I/O		Antenna diversity control signal
C5	RF_SW_CTRL_ANT0	I/O		Antenna diversity control signal
C6	GND	-	-	Ground
C7	GND	-	-	Ground
C8	GND	-	-	Ground
C9	GND	-	-	Ground
D1	GND	-	-	Ground
D2	S_GND	I/O	-	Ground for DC-DC
D3	GND	-	-	Ground
D6	GND	-	-	Ground
D7	GND	-	-	Ground
D8	GND	-	-	Ground
D9	GND	-	-	Ground
E5	GPIO_0	I	-	Interface select: 0:SDIO 1:SPI

Pin Number	Pin Name	type	Power	Description
E8	GND	-	-	Ground
E9	GND	-	-	Ground
F1	GND	-	-	Ground
F2	SDIO_D1	I/O	-	SDIO:WiFi_SDIO_DATA1;gSPI :IRQ, interrupt
F4	GPIO_1	O		WLAN to host wake up signal
F8	GND	-	-	Ground
F9	GND	-	-	Ground
G1	SDIO_D0	I/O	-	SDIO:WiFi_SDIO_DATA0; gSPI: Data output
G2	SDIO_CLK	I/O	-	SDIO:WiFi_SDIO_CLK; gSPI: SCLK,clock.
G3	SDIO_CMD	I/O		SDIO:WIFI_SDIO_DATA_CMD; gSPI: Data input
G4	WL_RST_N	I/O		WIFI Reset (If use Only WiFi Function)
G5	WL_CLK_REQ	I/O		WIFI_CLK_Request
G6	OSC_OUT	O		Xtal output
G7	GND	-	-	Ground
G8	GND	-	-	Ground
G9	GND	-	-	Ground
H1	GND	-	-	Ground
H2	VDDIO_WIFI	P	-	DC supply for WIFI and I/O.
H3	SDIO_D3	I/O		SDIO:WIFI_SDIO_DATA_3;gSPI:Card Select
H4	32K_PWM_OUT	I		WiFi 32.768KHz (Sleep Clock) input
H5	SDIO_D2	I/O		SDIO:WIFI_SDIO_DATA2; gSPI: Not Used
H6	OSC_IN	I		Xtal input
H7	GND	-	-	Ground
H8	GND	-	-	Ground
H9	GND	-	-	Ground
I1	GND	-	-	Ground
I2	GND	-	-	Ground
I3	GND	-	-	Ground
I4	GND	-	-	Ground
I5	GND	-	-	Ground
I6	GND	-	-	Ground
I7	GND	-	-	Ground
I8	GND	-	-	Ground
I9	GND	-	-	Ground

11 Boot Sequence

Shown below is the WLAN boot-up sequence from power-up to firmware download, including the initial device power-on reset(POR) evoked by the WL_RST_N(pin G4) signal. After initial power-up, the WL_RST_N signal can be held low to disable the ISM43362 or pulsed low induce a subsequent reset

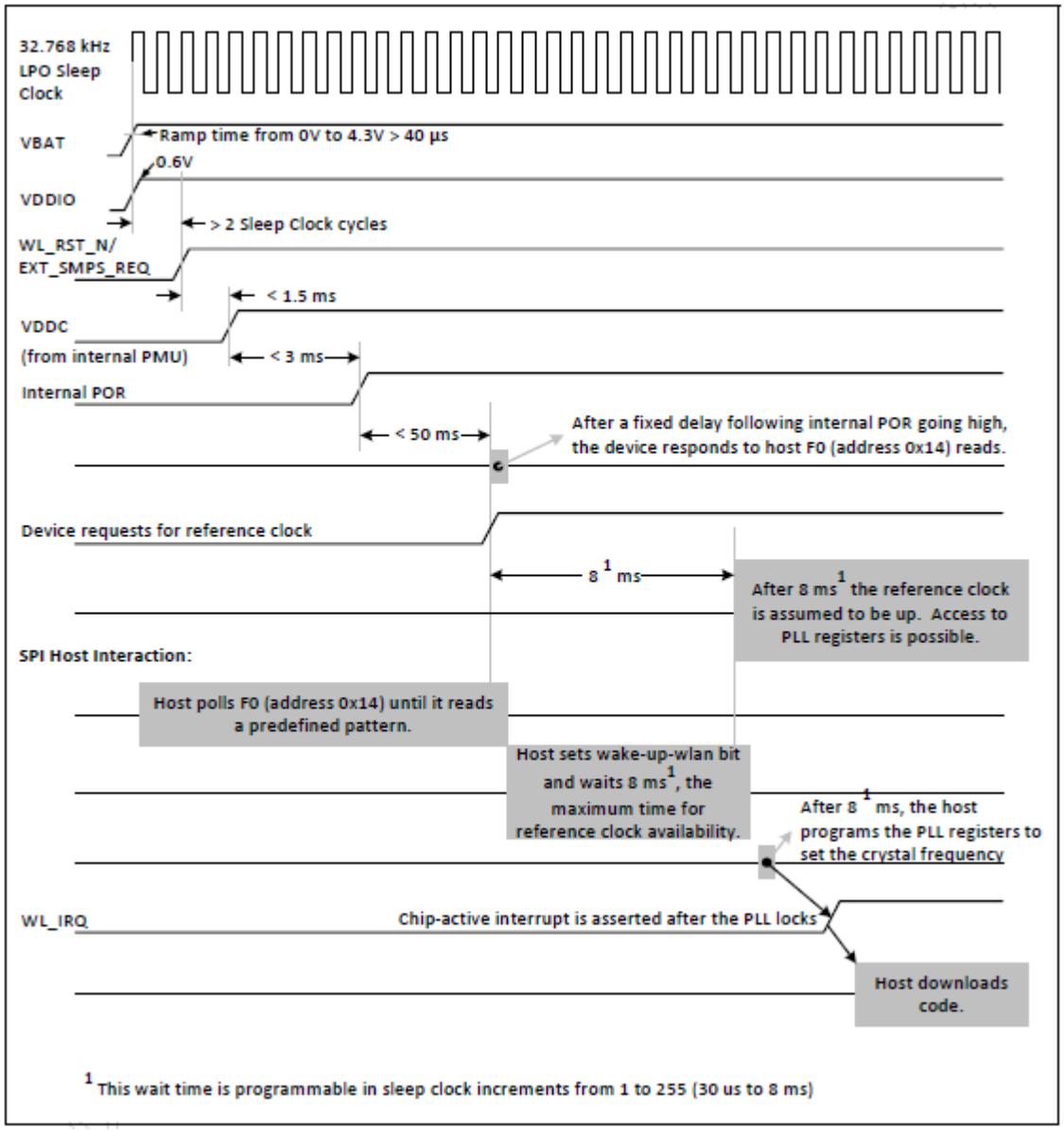
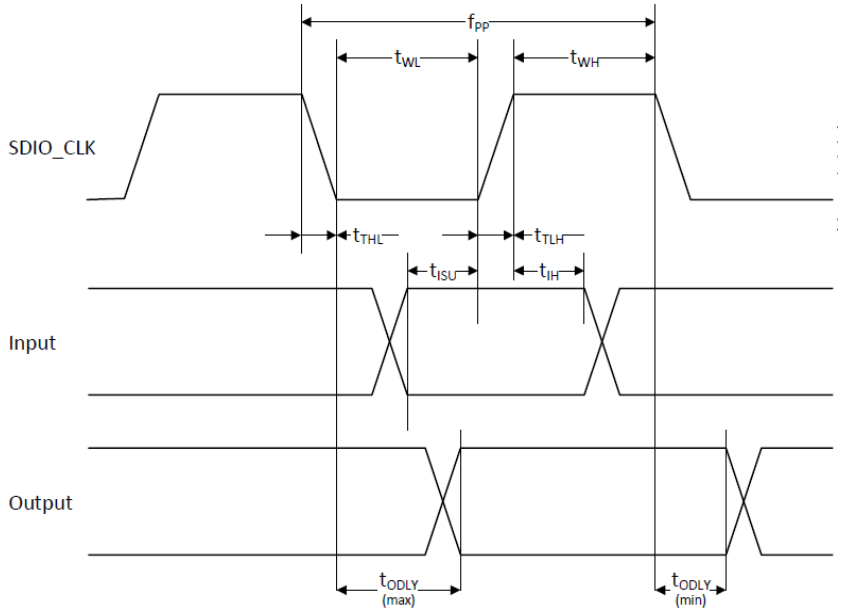


Figure 3 Boot Sequence

12 Communications Interfaces

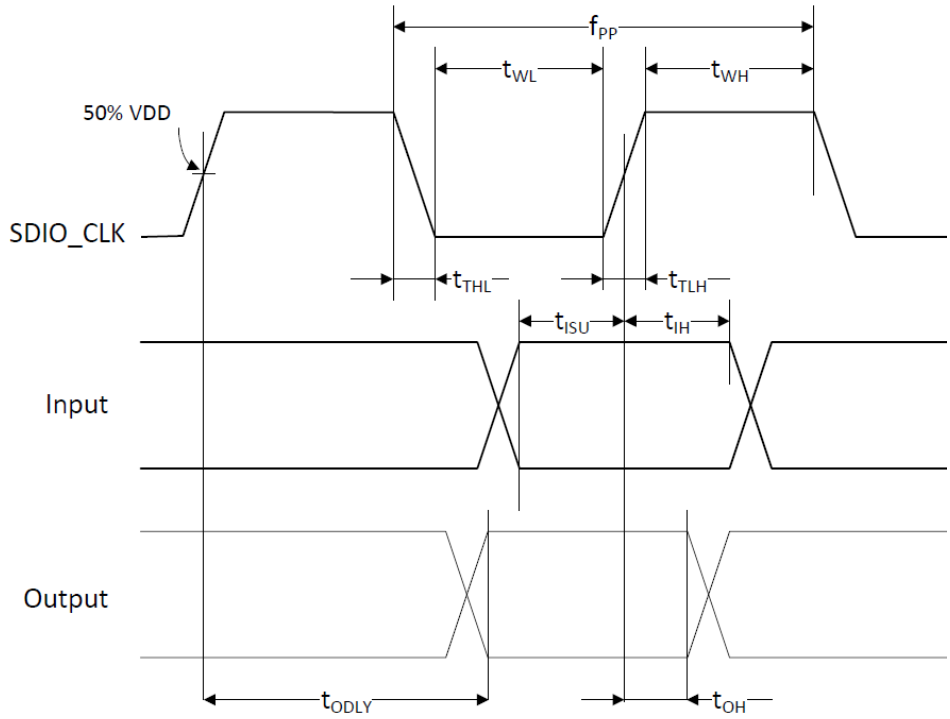
12.1 *SDIO Timing (Default Mode)*



SDIO Bus Timing (Default Mode)

Parameter	*Symbol*	*Min.*	Typ.	Max.	*Unit*
Frequency – Data Transfer mode	fPP	0	-	25	MHz
Frequency – Identification mode	fOD	0	-	400	KHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Output delay time – Data Transfer mode	tODLY	0	-	14	ns
Output delay time – Identification mode	tODLY	0	-	50	ns

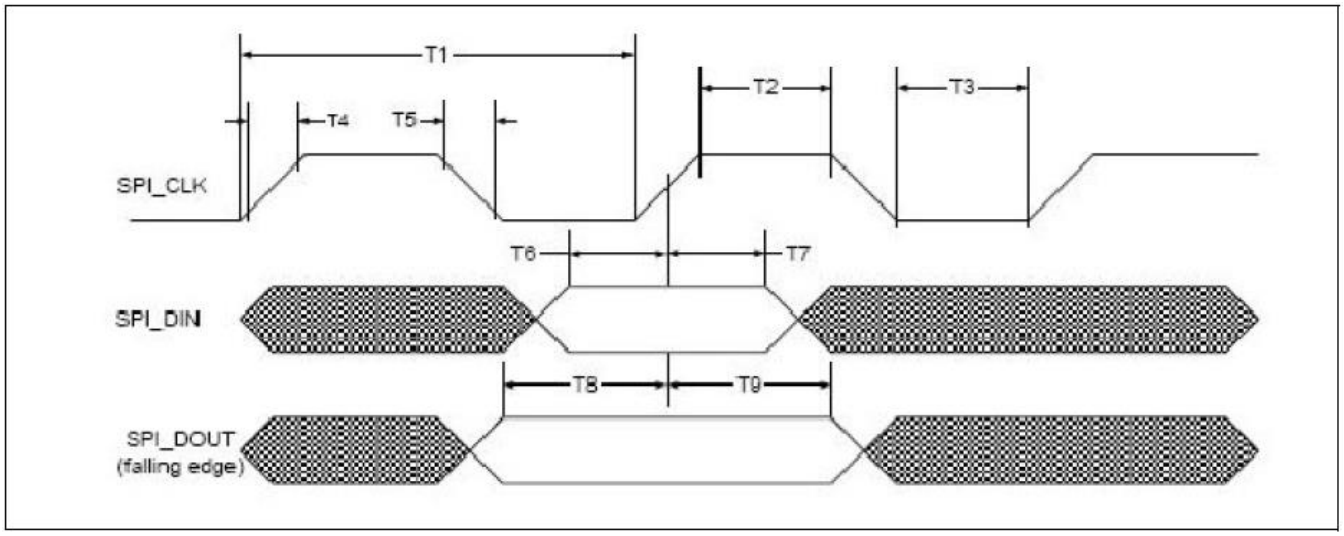
12.2 *SDIO Timing (High Speed Mode)*



SDIO Bus Timing (High-Speed Mode)

Parameter	*Symbol*	*Min.*	Typ.	Max.	*Unit*
Frequency – Data Transfer mode	fPP	0	-	50	MHz
Frequency – Identification mode	fOD	0	-	400	KHz
Clock low time	tWL	7	-	-	ns
Clock high time	tWH	7	-	-	ns
Clock rise time	tTLH	-	-	3	ns
Clock low time	tTHL	-	-	3	ns
Input setup time	tISU	6	-	-	ns
Input hold time	tIH	2	-	-	ns
Output delay time – Data Transfer mode	tODLY	0	-	14	ns
Output hold time	tOH	2.5	-	-	ns
Total system capacitance (each line)	CL	-	-	40	ns

12.3 *gSPI Interface Characteristics*



gSPI Timing

Parameter	Symbol	Min.	Max.	Unit	note
Clock period	T1	20.8	-	ns	Fmax = 48 MHz
Clock high/low	T2/T3	(0.45 × T1) – T4	(0.55 × T1) – T4	ns	-
Clock rise/fall time	T4/T5	-	2.5	ns	-
Input setup time	T6	5.0	-	ns	Setup time, SIMO valid to SPI_CLK active edge
Input hold time	T7	5.0	-	ns	Hold time, SPI_CLK active edge to SIMO invalid
Output setup time	T8	5.0	-	ns	Setup time, SOMI valid before SPI_CLK rising
Output hold time	T9	5.0	-	ns	Hold time, SPI_CLK active edge to SOMI invalid
CSX to clock[a]	-	7.86	-	ns	CSX fall to 1st rising edge
Clock to CSX[c]	-	-	-	ns	Last falling edge to CSX high

gSPI Timing Parameters

a. SPI_CSx remains active for entire duration of gSPI read/write/write_read transaction(i.e., overall words for multiple word transaction).

Mode	SDIO	gSPI
Data0	SDIO D0	DO:Data Output
Data1	SDIO D1	IRQ:Interrupt
Data2	SDIO D2	NC:Not Used
Data3	SDIO D3	CS:Card Select
CLK	SDIO CLK	SCLK:Clock
CMD	SDIO CMD	DI:Data Input

Table: SDIO mode and gSPI mode

12.4 *External 32.768KHz Low Power Oscillator*

The ISM43362-B81 SiP uses an optional secondary low frequency clock for low power mode timing. A precision external 32.768 kHz clock that meets the specifications listed in the table below is required.

The ISM43362-B81 SiP will auto-detect the LPO clock. If it senses a clock on the 32K_PWM_OUT (PinH4), it will use that clock. If it doesn't sense a clock, it will use its own internal LPO.

To minimize current during power saving mode, the external 32.768 kHz oscillator must be used.
-To use the internal LPO: Tie 32K_PWM_OUT to ground. Do not leave this pin floating.
-To use an external LPO: Connect the external 32.768KHz clock to 32K_PWM_OUT.

The module will auto-detect the LPO clock. If it senses a clock on the 32K_PWM_OUT (PinH4), it will use that clock. If it doesn't sense a clock, it will use its own internal LPO.

The use of this pin is optional. If you use an external 32.768 kHz or feed 32.768 KHz in to ISM43362 module from HOST, it must meet specification as shown below. The external 32.768 KHz oscillator must be used to enable power saving mode.

Symbol	*Parameter*	*Conditions/Notes*	*Specification*			
			Min.	Typ.	Max.	*Unit*
Fr	Frequency	-	-	32768	-	Hz
△f/fr	Frequency tolerance	At 25^{0}C	-30	-	+30	ppm
		-20^{0}C <Ta<+70^{0}C	-150	-	+40	
		-30^{0}C <Ta<+85^{0}C	-220	-	+40	
Duty cycle	-	-	30	-	70	%
Vol	Output low voltage	-	0	-	0.2	V
Voh	Output high voltage	-	0.7Vio	-	Vio	V
Tr/Tf	Rise and fall time	-	-	-	100	Ns
-	Signal type	Digital				
-	Clock jitter	Integrated over 300 Hz to 15kHz	-	-	30	ns
-	Input impedance	Resistive	10	-	-	MΩ
		Capacitive	-	-	2	pF
-	Input amplitude	Fail safe, 3.3V digital I/O	-	-	3.63	V

External 32.768 KHz Sleep Clock Specification

13 Reference Clock for WLAN

The ISM43362 needs an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components.

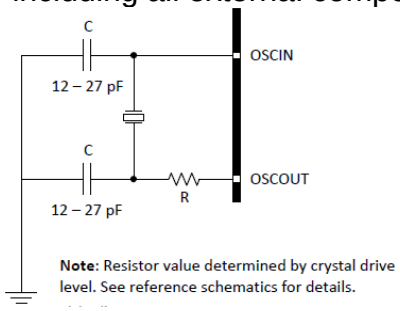


Figure 4 Xtal relative layout

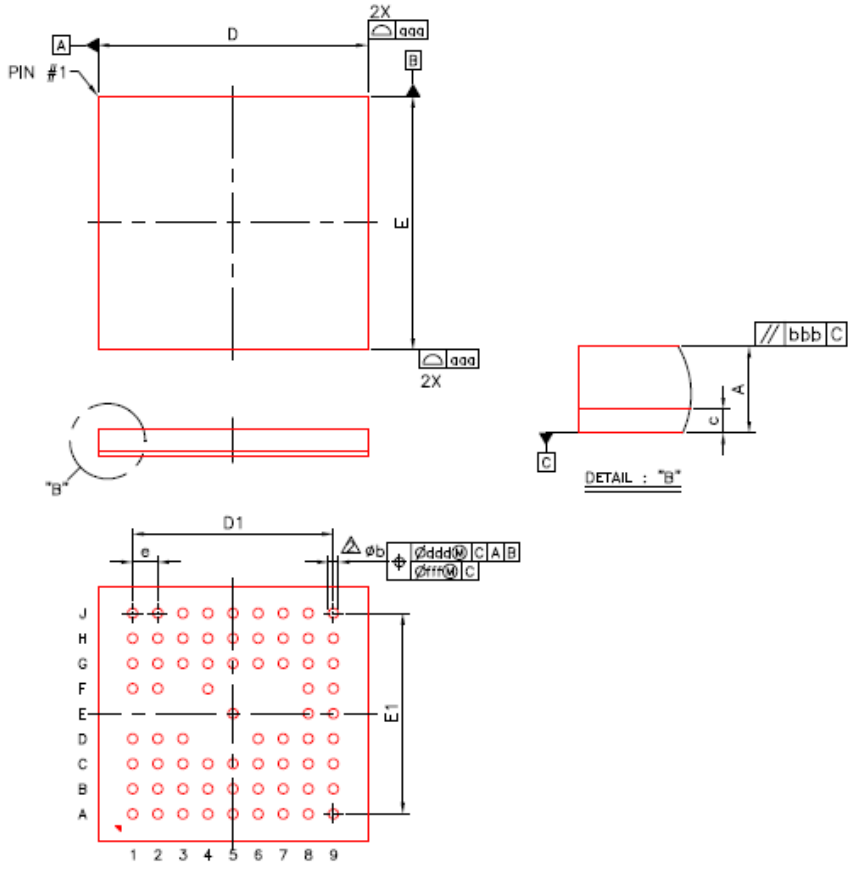
Parameter	*Conditions/Notes*	*Crystal*			*External Frequency Reference*			
		Min.	Typ.	Max.	*Min.*	Typ.	Max.	*Unit*
Frequency	-	Between 12MHz and 52MHz[a]						
Crystal load capacitance	-	-	12	-				pF
ESR	-	-	-	60				Ω
Input Impedance (OSCIN)[b]	Resistive				30k	100k	-	Ω
	Capacitive				-	-	7.5	pF
Input Impedance (WRF_TCXO_IN)[b]	Resistive				30k	100k	-	Ω
	Capacitive				-	-	4	pF
OSCIN input voltage	AC-coupled analog signal				400	-	1200	mV_{p-p}
OSCIN input low level	DC-coupled analog signal				0	-	0.2	V
OSCIN input high level	DC-coupled analog signal				1.0	-	1.36	V
WRF_TCXO_IN input Voltage	C-coupled analog signal[c]				400	-	TCXO_VDD[d]	mV_{p-p}
Frequency tolerance Initial + over temperature	-	-20	-	20	-20	-	20	ppm
Duty cycle	26 MHz clock				40	50	60	%
Phase Noise[e,f] (IEEE 802.11 b/g)	26 MHz clock at 1kHz offset				-	-	-119	dBc/Hz
	26 MHz clock at 10kHz offset				-	-	-129	dBc/Hz
	26 MHz clock at 100kHz offset				-	-	-134	dBc/Hz
	26 MHz clock at 1MHz offset				-	-	-139	dBc/Hz
Phase Noise[e,f] (IEEE 802.11 n, 2.4GHz)	26 MHz clock at 1kHz offset				-	-	-124	dBc/Hz
	26 MHz clock at 10kHz offset				-	-	-134	dBc/Hz
	26 MHz clock at 100kHz offset				-	-	-139	dBc/Hz
	26 MHz clock at 1MHz offset				-	-	-144	dBc/Hz

Figure 5 External Clock requirements

a. The frequency step size is approximately 80 Hz. The ISM43362-B81 does not auto-detect the reference clock frequency; the frequency is specified in the software/NVRAM file.
b. The internal clock buffer connected to this pin will be turned off when the ISM43362-B81 SiP goes into Sleep mode.
When the clock buffer turns on and off, there will be a small impedance variation up to ±15%.
c. This input has an internal DC blocking capacitor, so do not include an external DC blocking capacitor.
d. The maximum allowable voltage swing for the WRF_TCXO_IN input is equal to the WRF_TCXO_VDD3P3 supply voltage range, which is 1.7V to 3.3V.
e. For a clock reference other than 26MHz, 20 x log(f/26) dB should be added to the limits, where f= the reference clock frequency in MHz.
f. If the selected clock has a flat phase-noise response above 100kHz, then it is acceptable to subtract 1dB from all 1kHz,10kHz and 100kHz values shown, and ignore the 1MHz requirement.

14 Mechanical Specification

The dimensions of the WiFi SiP SiP are 8.6mm (W) x 8.1mm (L) x 1.0mm (H): (Tolerance: +/- 0.1mm)



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.81	0.90	0.94	0.032	0.035	0.037
c	0.16	0.20	0.24	0.006	0.008	0.009
D	8.50	8.60	8.70	0.335	0.339	0.343
E	8.00	8.10	8.20	0.315	0.319	0.323
D1/E1	---	6.40	---	---	0.252	---
e	---	0.80	---	---	0.031	---
b	---	0.312	---	---	0.012	---
aaa		0.15			0.006	
bbb		0.10			0.004	
ddd		0.10			0.004	
fff		0.05			0.002	

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. DIMENSION b IS MEASURED AT THE MAXIMUM OPENING DIAMETER, PARALLEL TO PRIMARY DATUM C.

15 Recommend Footprint

Unit: mm

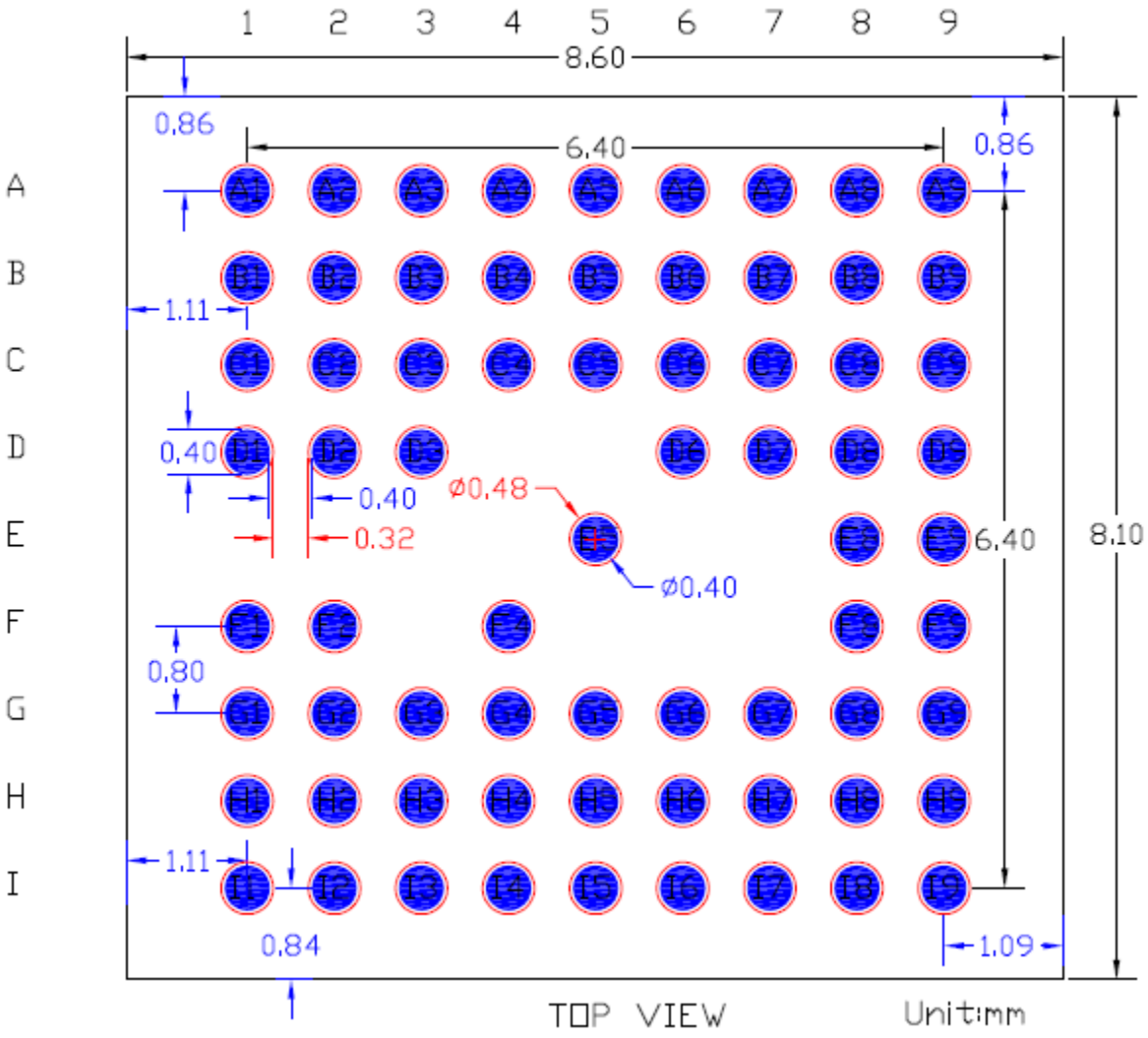


Figure 6 TOP View

Note:
Recommend footprint use NSMD (No-Solder Mask Define)
Padψ:0.4mm & Solder Maskψ: 0.48.

16 Recommended Stencil

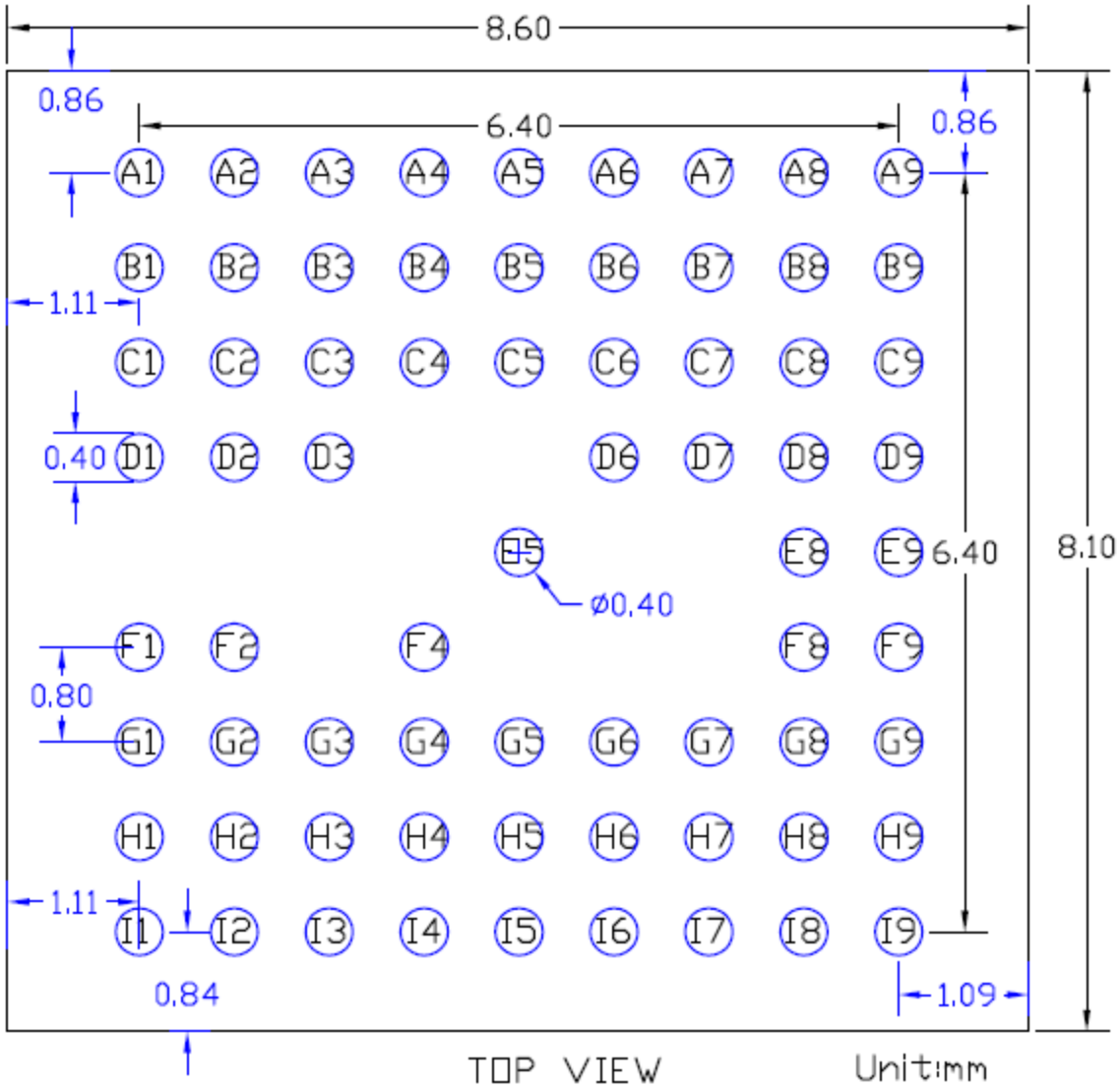
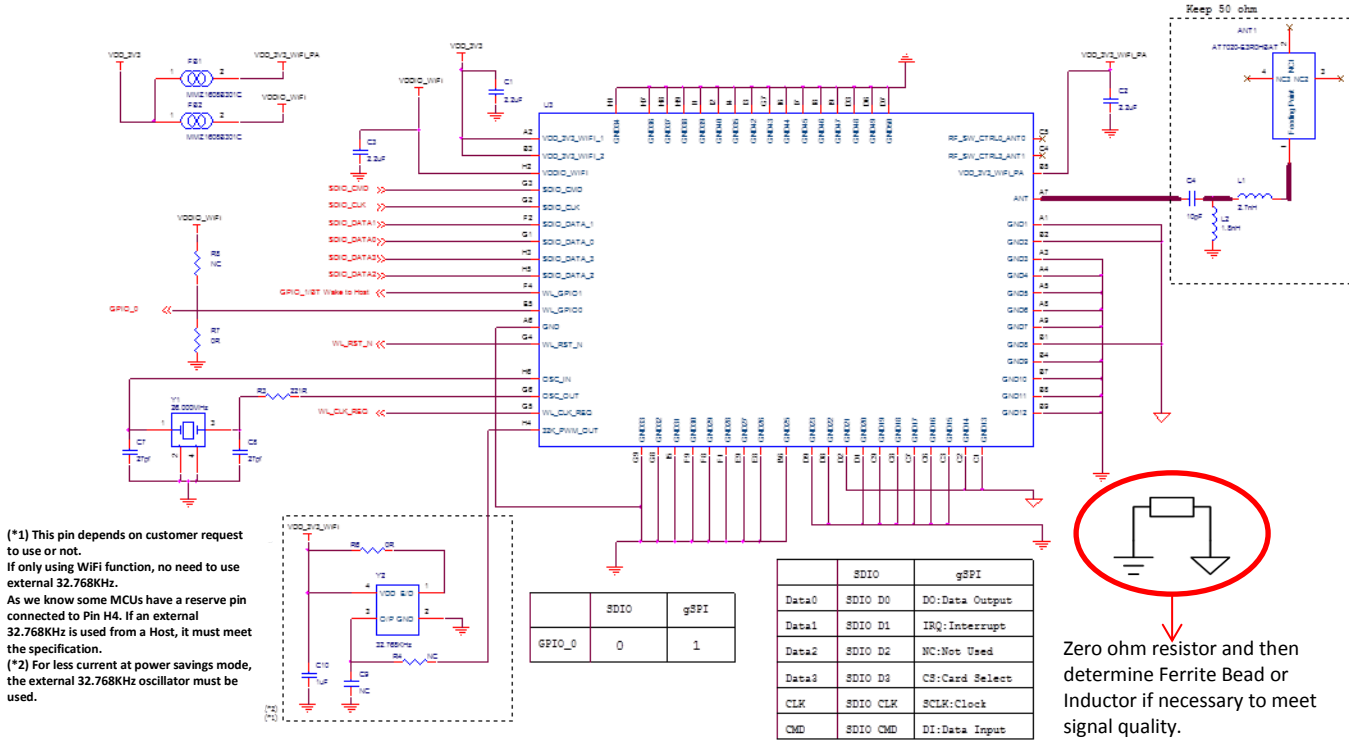


Figure 7 Note: Stencil Thickness: 0.06mm (typical)

17 Reference Schematic



	SDIO	gSPI
GPIO_0	0	1

	SDIO	gSPI
Data0	SDIO_D0	DO:Data Output
Data1	SDIO_D1	IRQ:Interrupt
Data2	SDIO_D2	NC:Not Used
Data3	SDIO_D3	CS:Card Select
CLK	SDIO_CLK	SCLK:Clock
CMD	SDIO_CMD	DI:Data Input

Figure 8 - ISM43362-B1 EVB Reference Schematic

*Note:

- C2 must be placed as close as possible to the ISM43362
- S_GND is the ground for the DC-DC convertors in the SiP.
    - The two GNDs should be separated islands at the SiP and then connected together. Reference Note above.

18 Power Supply

The ISM43362-B81 requires 3 power supplies:

1. VDDIO_WiFi
2. VDD_3V3_WiFi
3. VDD_3V3_WiFi_PA

Typical voltage is 3.3V. Please add bypass capacitor.

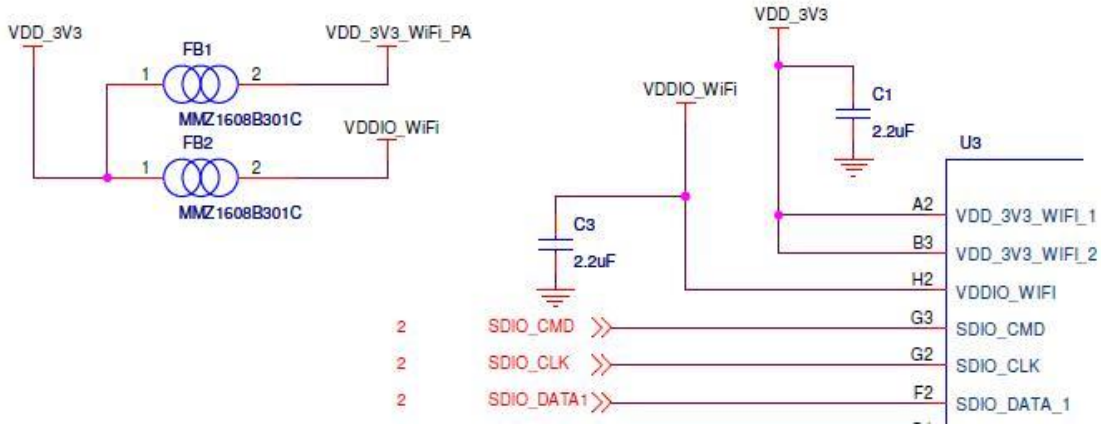


Figure 9 VDD_3V3 and VDDIO_WiFi diagram

The placement of C2 is critical and requires careful placement as close to the ball B5. Please keep this VDD_3V3_WiFi_PA signal clear from and critical signals.

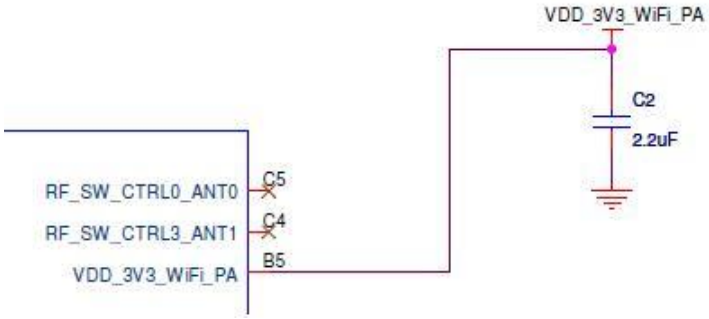


Figure 10 VDD_3V3_WiFi_PA diagram

18.1 *SDIO and GSPI CONFIGURATION*

The ISM43362 SDIO and gSPI strapping options. The below table 2.2, shows the SDIO and gSPI pin definitions. Keep SDIO signal equal length. Typically we recommend SDIO for most applications.

	SDIO	gSPI
GPIO_0	0	1

Figure 11 SDIO and gSPI option

.

Pin definition	SDIO	gSPI
G1	SDIO_DATA0	SPI_MISO
F2	SDIO_DATA1	SPI_IRQ
H5	SDIO_DATA2	-
H3	SDIO_DATA3	SPI_CSX
G3	SDIO_CMD	SPI_MOSI
G2	SDIO_CLK	SPI_CLK

Figure 12 SDIO and gSPI pin definition

18.2 *26MHz Xtal schematic and layout*

As shown below, there should only be ground on the 1st and 2nd layer surround the OSC_IN, OSC_OUT, and 32K_PWM_OUT traces. There should not be any signal or power trace underneath the OSC_IN, OSC_OUT, and 32K_PWM_OUT traces. Place XTAL close to OSC_IN, OSC_OUT, and 32K_PWM_OUT pins. OSC_IN, OSC_OUT, and 32K_PWM_OUT traces have to be as short as possible. Place load capacitors close to Xtal in and out pins. The XTAL specification must meet below table 2.4.

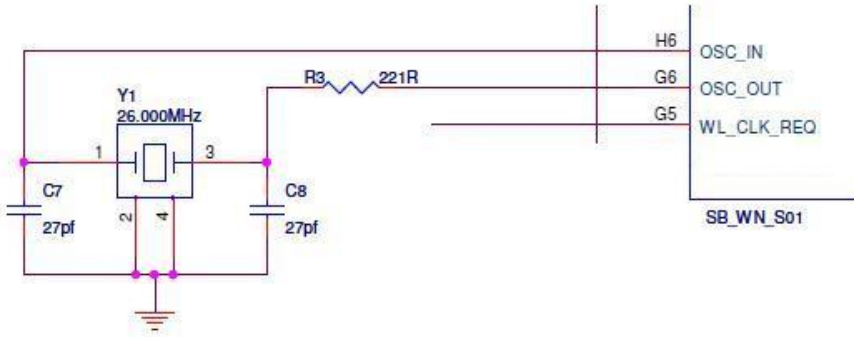


Figure 13 XTAL schematic

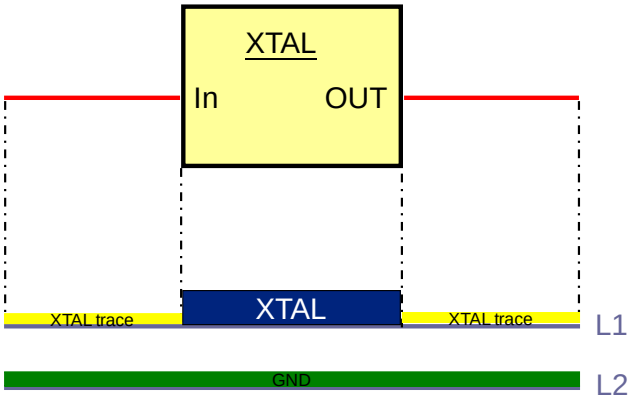


Figure 14 XTAL layout

18.3 *2.4 GHz RF TRACE*

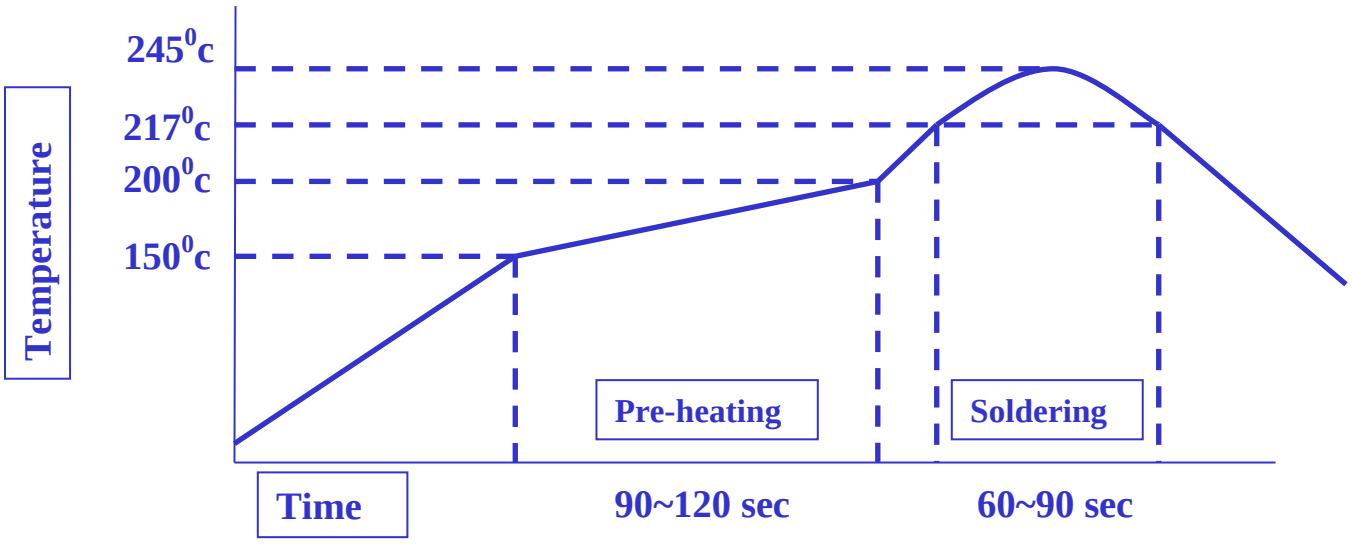
It is recommended that the RF antenna trace be routed on the top layer with the 2nd layer as the ground reference. Use a “Microstrip transmission line” model for the RF path.

19 Product Compliance Considerations

RoHS: Restriction of Hazardous Substances (RoHS) directive has come into force since 1st July 2006 all electronic products sold in the EU must be free of hazardous materials, such as lead. Inventek is fully committed to being one of the first to introduce lead-free products while maintaining backwards compatibility and focusing on a continuously high level of product and manufacturing quality.

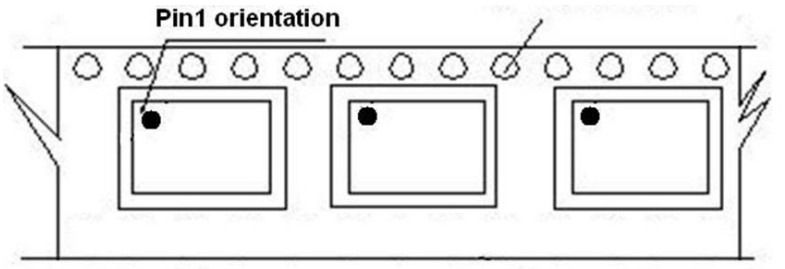
EMI/EMC: The Inventek module design embeds EMI/EMC suppression features and accommodations to allow for higher operational reliability in noisier (RF) environments and easier integration compliance in host (OEM) applications.

20 Reflow Profile



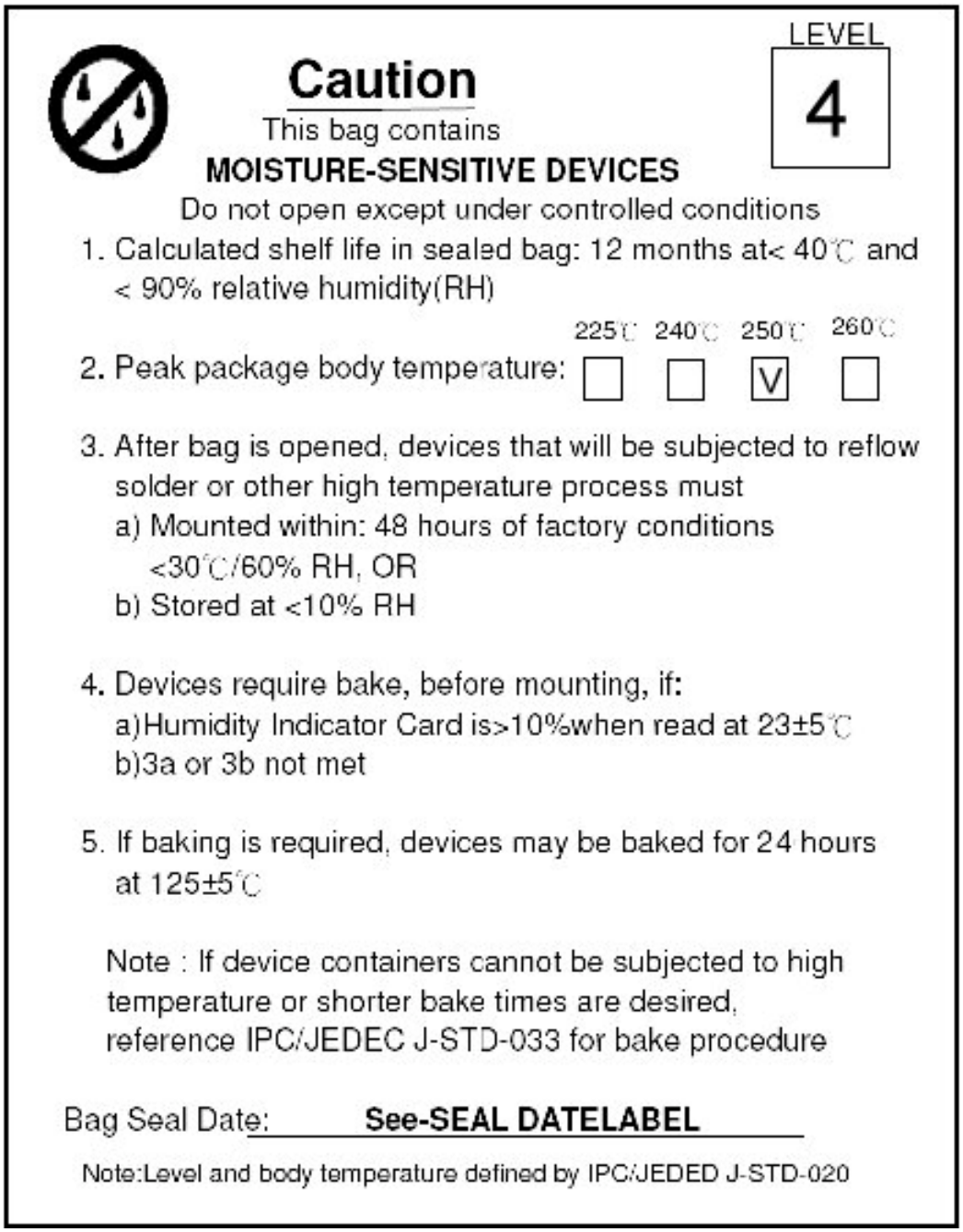
21 Packaging Information

21.1 *Tape/Reel : The ISM43362-B81 comes in Tape and Reel.*



Feeding direction (Into Reel)

21.2 *MSL Level / Storage Condition*



21.3 *Device baking requirements prior to assembly*

Boards must be baked prior to rework or assembly to avoid damaging moisture sensitive components during localized reflow. The default bake cycles is 24 hours at 125C.
Maintaining proper control of moisture uptake in components is critical.
Before opening the shipping bag and attempting solder reflow, you should maintain a minimal out-of-bag time and ensure the highest possible package reliability for the final product.

22 REVISION CONTROL

Document : ISM43362-B81	Wi-Fi module
Internal Release	DOC-DS-20076-2.2

Date	Author	Revision	Comment
4/23/2014	FMT	1.0	Preliminary
4/27/2014	FMT	2.0	Preliminary- Added Ref. design
11/12/2014	AS	2.1	Page 25, Grounding scheme
11/13/14	AS	2.2	Page 25, Grounding Scheme Update

23 CONTACT INFORMATION

Inventek Systems
2 Republic Road
Billerica Ma, 01862
Tel: 978-667-1962
Sales@inventeksys.com

www.inventeksys.com