International
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REFERENCE DESIGN

IRAUDAMP6

250W/8Ω x 2 Channel Class D Audio Power Amplifier Using the IRS20957S and IRF6785

By

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CAUTION:

International Rectifier suggests the following guidelines for safe operation and handling of IRAUDAMP6 Demo board;

- **Always wear safety glasses whenever operating Demo Board**
- **Avoid physical contact with exposed metal surfaces when operating Demo Board**
- **Turn off Demo Board when placing or removing measurement probes**

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Introduction

The IRAUDAMP6 reference design is a two-channel, 250W/ch (8Ω) load half-bridge Class D audio power amplifier. This reference design demonstrates how to use the IRS20957S Class D audio controller and gate driver IC, implement protection circuits, and design an optimum PCB layout using the IRF6785 DirectFET MOSFETs. This reference design does not require increasing the size of the heatsink or require fan cooling for normal operation (one-eighth of continuous rated power).The reference design provides all the required housekeeping power supplies for ease of use. The two-channel design is scalable for power and the number of channels.

Applications

- AV receivers
- Home theater systems
- Mini component stereos
- Powered speakers
- Sub-woofers
- Musical Instrument amplifiers

Features

Output Power:	250W x 2 channels (8Ω load),
Residual Noise:	90μV, IHF-A weighted, AES-17 filter
Distortion:	0.005% THD+N @ 125W, 8Ω
Efficiency:	96% @ 250W, 8Ω, single-channel driven, Class D stage
Multiple Protection Features:	Over-current protection (OCP), high side and low side Over-voltage protection (OVP), Under-voltage protection (UVP), high side and low side DC-protection (DCP), Over-temperature protection (OTP)
PWM Modulator:	Self-oscillating half-bridge topology with optional clock synchronization

Specifications

General Test Conditions (unless otherwise noted)		Notes / Conditions
Supply Voltages	±73.5V	
Load Impedance	8-4Ω	
Self-Oscillating Frequency	400kHz	No input signal, Adjustable
Gain Setting	33dB	1Vrms input yields rated power

Electrical Data	Typical	Notes / Conditions
IR Devices Used	IRS20957S Audio Controller and Gate-Driver, IRF6785 DirectFET MOSFETs	
Modulator	Self-oscillating, second order sigma-delta modulation, analog input	
Power Supply Range	± 38V to ±75V	Bipolar power supply
Output Power CH1-2: (1% THD+N)	320W	1kHz
Output Power CH1-2: (10% THD+N)	410W	1kHz

Rated Load Impedance	8-4Ω	Resistive load
Idling Supply Current	±85mA	No input signal
Total Idle Power Consumption	11.9W	No input signal
Channel Efficiency	96%	Single-channel driven, 250W, Class D stage

.

Audio Performance	***Before Demodulator**	**Class D Output**	**Notes / Conditions**
THD+N, 1W THD+N, 10W THD+N, 60W THD+N, 100W THD+N, 200W	0.008% 0.003% 0.0015% 0.002% 0.009%	0.008% 0.004% 0.002% 0.004% 0.009%	1kHz, Single-channel driven
Dynamic Range	117dB	113dB	A-weighted, AES-17 filter, Single-channel operation
Residual Noise, 22Hz - 20kHzAES17	70μV	110μV	Self-oscillating – 400kHz
Damping Factor	2000	906	1kHz, relative to 8Ω load
Channel Separation	92dB 90dB 72dB	92dB 80dB 62dB	100Hz 1kHz 10kHz
Frequency Response : 20Hz-20kHz : 20Hz-35kHz	N/A	±0.25dB ±1dB	1W, 8Ω Load

Thermal Performance	**Typical**	**Notes / Conditions**
Idling	T_C =30°C T_{PCB}=36°C	No signal input, T_A=25°C
2ch x 31.25W (1/8 rated power)	T_C =54°C T_{PCB}=65°C	Continuous, T_A=25°C
2ch x 250W (Rated power)	T_C =80°C T_{PCB}=106°C	At OTP shutdown @ 150 sec, T_A=25°C

Physical Specifications

Dimensions	7.76”(L) x 5.86”(W) x 2.2”(H) 192 mm (L) x 149mm (W) x56mm(H)
Weight	0.54kgm

Connection Setup

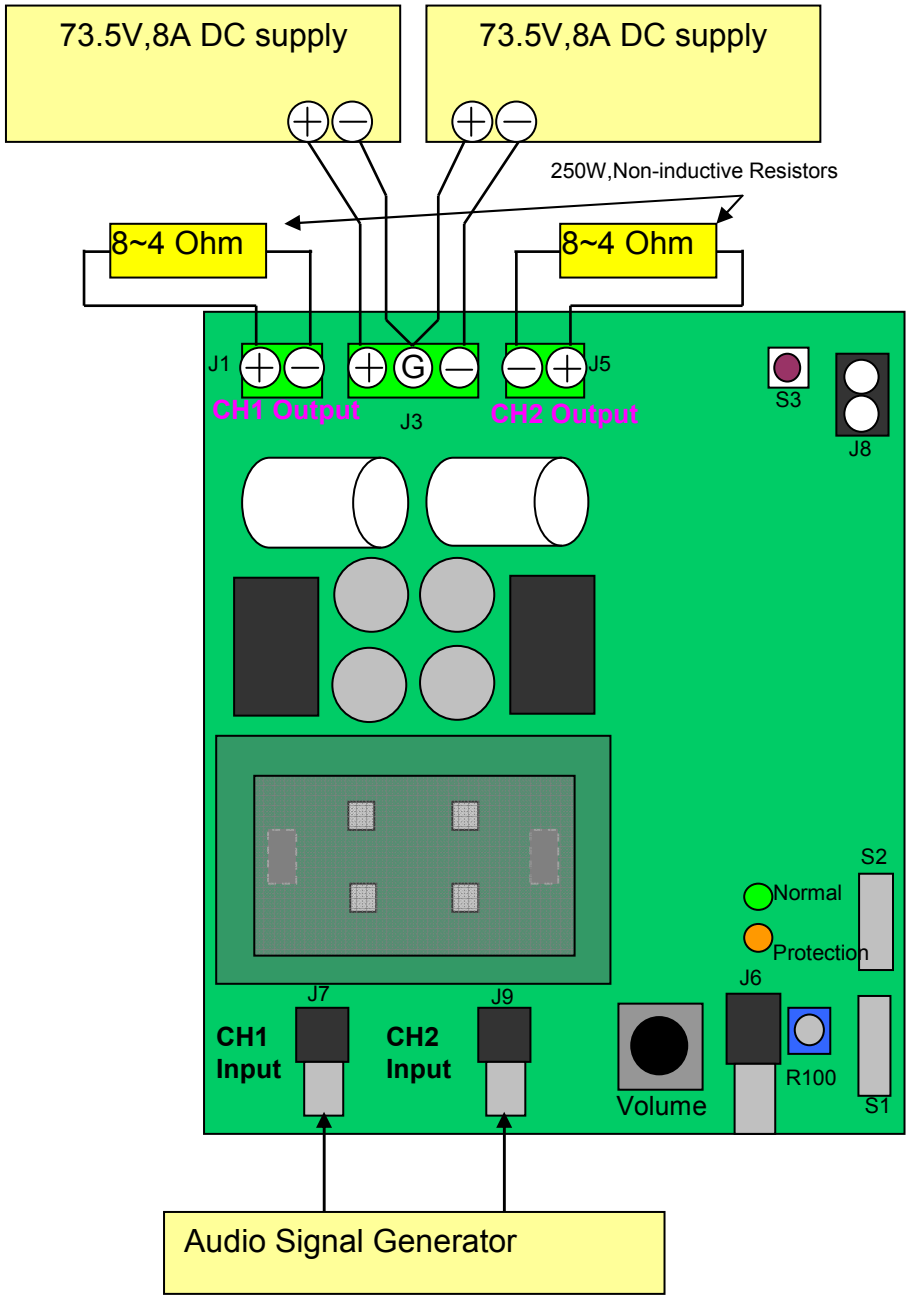


Fig 1 Typical Test Setup

Connector Description

CH1 IN	J7	Analog input for CH1
CH2 IN	J9	Analog input for CH2
POWER	J3	Positive and negative supply (+B / -B)
CH1 OUT	J1	Output for CH1
CH2 OUT	J5	Output for CH2
EXT CLK	J6	External clock sync
DCP OUT	J8	DC protection relay output

Test Procedures

Test Setup:

1. Connect 8Ω-250 W dummy loads to output connectors (J1 and J5 as shown on Fig 1) and parallel it with input of Audio Precision analyzer (AP).
2. Connect the Audio Signal Generator to J7 and J9 for CH1 and CH2 respectively (AP).
3. Set up the dual power supply with voltages of ±73.5V;set current limit to 8A.
4. TURN OFF the dual power supply before connecting to ON of the unit under test (UUT).
5. Set switch S1 to middle position (self oscillating).
6. Set volume level knob R130 fully counter-clockwise (minimum volume).
7. Connect the dual power supply to J3. as shown on Fig 1

Power up:

8. Turn ON the dual power supply. The ±B supplies must be applied and removed at the same time.
9. Red LED (Protection) should turn on almost immediately and turn off after about 3s.
10. Green LED (Normal) then turns on after red LED is extinguished and should stay on.
11. Quiescent current for the positive supply should be 84mA ±10mA at +73.5V.
12. Quiescent current for the negative supply should be 80mA ±10mA at –73.5V.
13. Push S3 switch(Trip and Reset push-buttom)to restart the sequence of LEDs indicators,which should be the same as noted above in steps 9-10.

Switching Frequency test

14. Monitor switching waveform at VS1/J4(pin9-12)of CH1 and VS2/J3(pin1-4)CH2 on Daughter Board using an Oscilloscope.
15. For IRAUDAMP6, the self-oscillating switching frequency is pre-calibrated to 400 KHz. To modify the IRAUDAMP6 frequency, change the values of potentiometers R49 and R74 for CH1 and CH2 respectively.

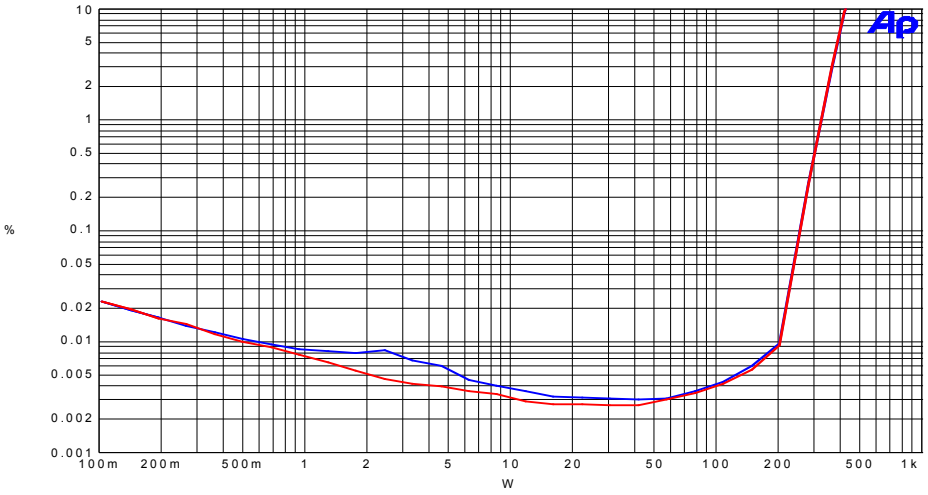
Functionality Audio Tests:

16. Apply 1V RMS at 1kHz sinusoidal signal from the Audio Signal Generator.
17. Turn control volume up (R130 clock-wise) to obtain an output reading of 250Watts.
18. For all subsequent tests as shown on the Audio Precision graphs below (Fig 2- Fig7), the measurements are taken across J1 and J5 with an AES-17 Filter. Observe that a 1 V_{RMS} input generates an output voltage of 44.7 V_{RMS}.
19. Sweep the audio signal voltage from 15 mV_{RMS} to 1 V_{RMS}.
20. Monitor the output signals at J1/J5 with an oscilloscope. The waveform must be a non distorted sinusoidal signal.

Test Setup using Audio Precision (Ap):

21. Use an unbalanced-floating signal from the generator outputs.
22. Use balanced inputs taken across output terminals, J1 and J5.
23. Connect Ap frame ground to GND at terminal J7/J9.
24. Select the AES-17 filter(pull-down menu) for all the testing except frequency response.
25. Sweep the input signal voltage from 15 mV_{RMS} to 1 V_{RMS}.
26. Run Ap test programs for all subsequent tests as shown in Fig 2- Fig 7below.

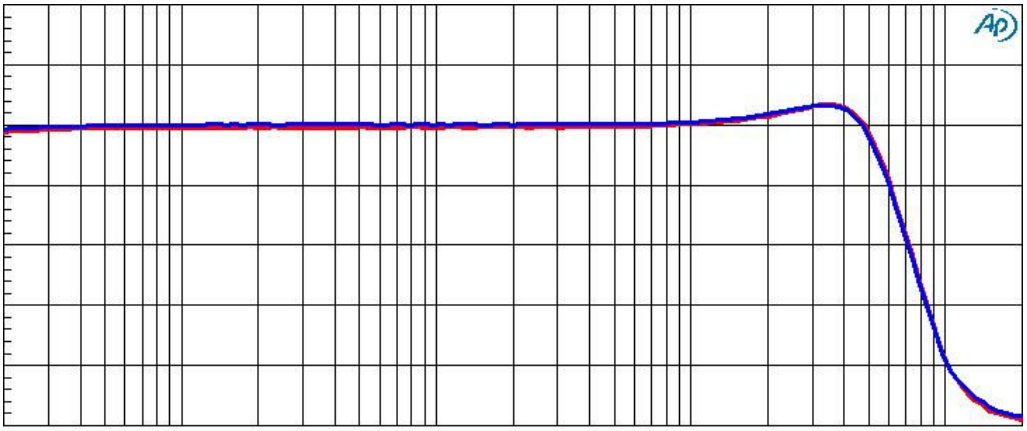
Performance and test graphs



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Blue	Solid	2	Anlr.THD+N Ratio	Left	CH2
1	3	Red	Solid	2	Anlr.THD+N Ratio	Left	CH1

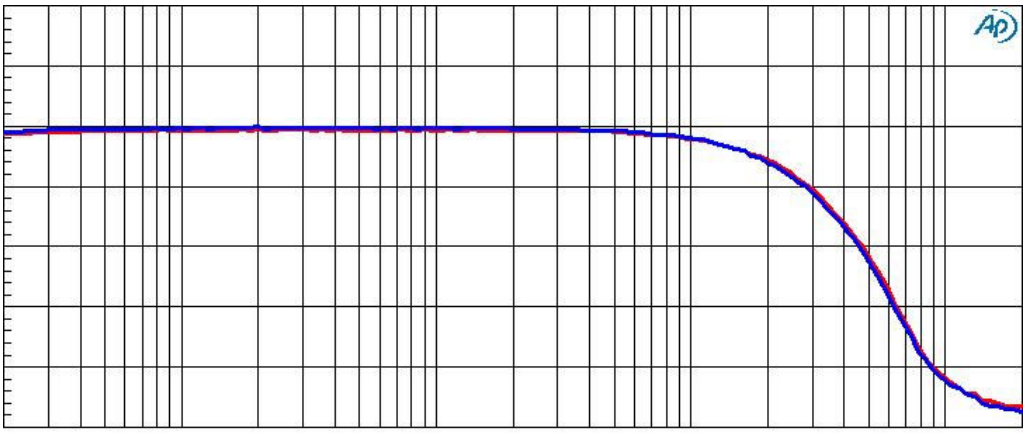
±B Supply = ±73.5V, 8 Ω Resistive Load

Fig 2 IRAUDAMP6, THD+N versus Power, Stereo, 8 Ω



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	2	Red	Solid	3	Anlr.Level B	Left	CH1_8Ohm
2	2	Blue	Solid	3	Anlr.Level B	Left	CH2_8Ohm

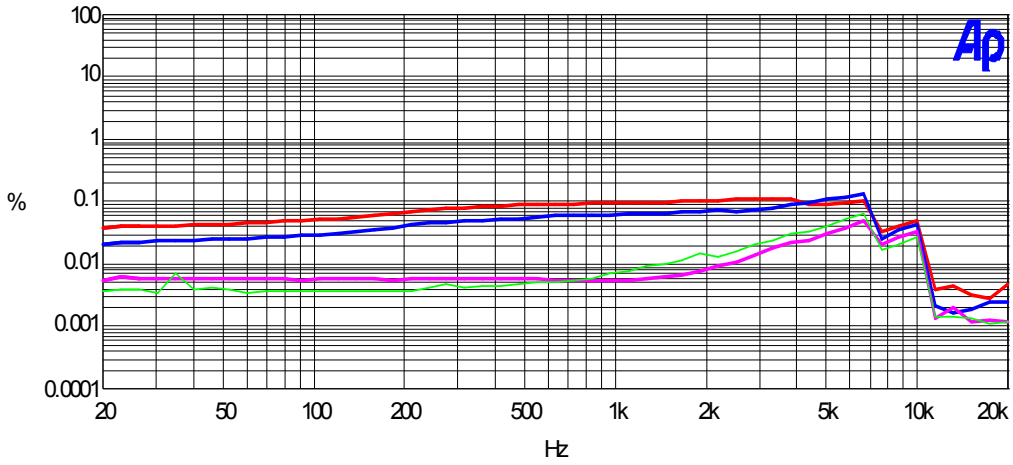
8 ohm load



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	2	Red	Solid	3	Anlr.Level B	Left	CH1_4Ohm
2	2	Blue	Solid	3	Anlr.Level B	Left	CH2_4Ohm

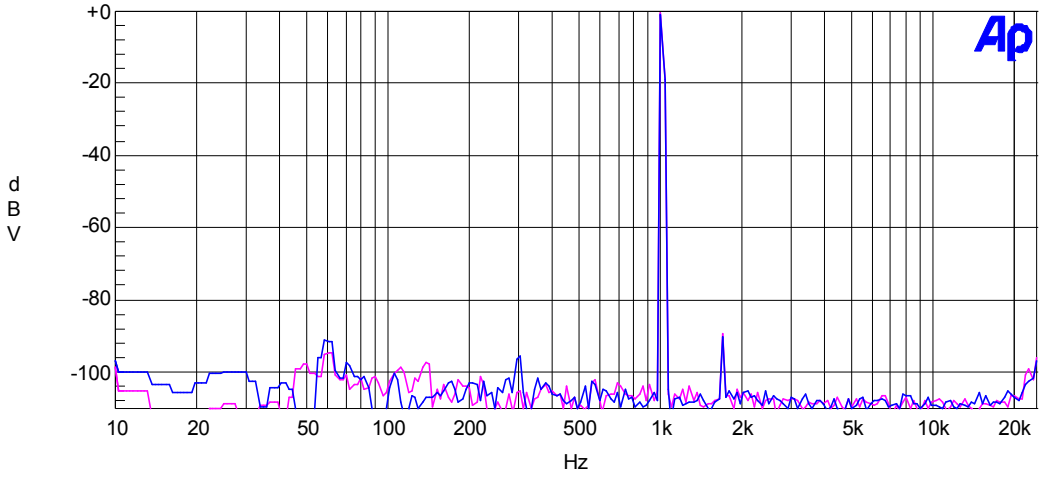
4 ohm load

Fig 3 IRAUDAMP6, Frequency response



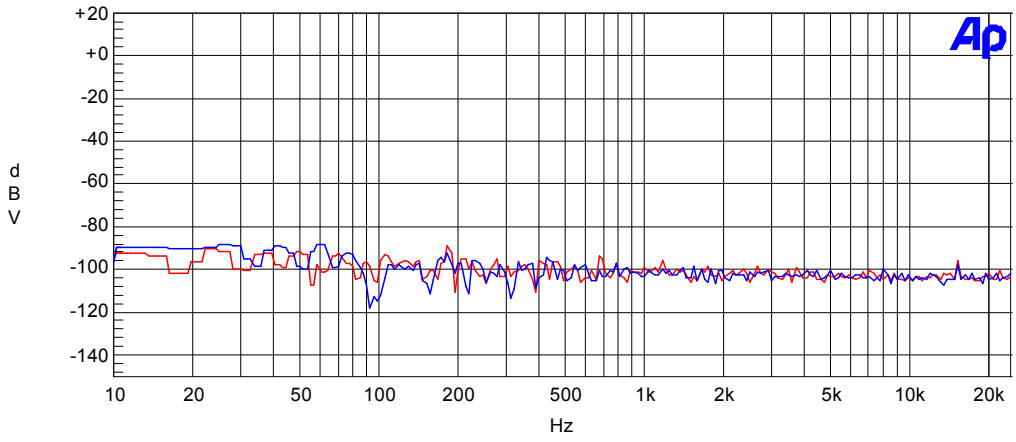
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Anlr.THD+N Ratio	Left	125W L
1	2	Blue	Solid	2	Anlr.THD+N Ratio	Left	125W R
2	1	Magenta	Solid	2	Anlr.THD+N Ratio	Left	25W L
2	2	Green	Solid	1	Anlr.THD+N Ratio	Left	25W R

Fig 4 THD+N Ratio vs. Frequency



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Magenta	Solid	1	Fft.Ch.1 Ampl	Left	
1	2	Blue	Solid	1	Fft.Ch.2 Ampl	Left	

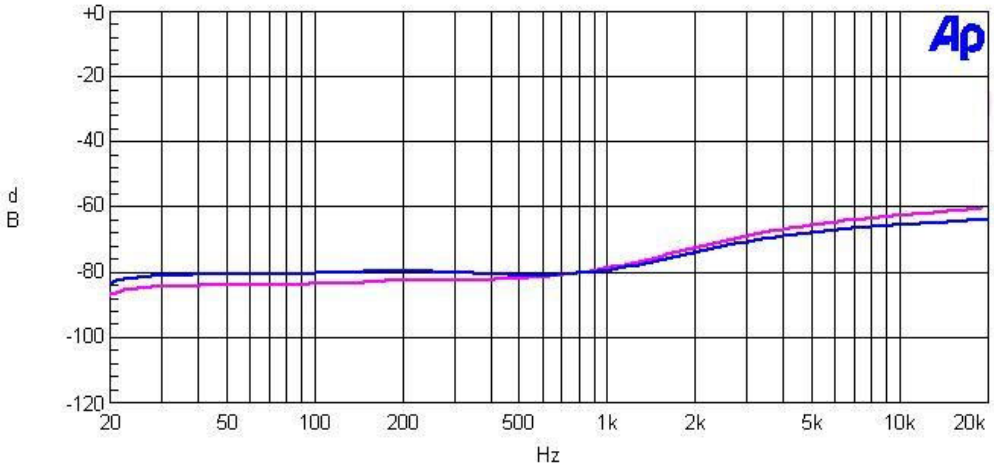
Fig 5, 1V output Frequency Spectrum



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	Fft.Ch.1 Ampl	Left	
1	2	Blue	Solid	1	Fft.Ch.2 Ampl	Left	

No signal, Self Oscillator @ 400kHz

Fig 6, IRAUDAMP6 Noise Floor



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Magenta	Solid	2	Anlr.Ratio	Left	CH1
1	2	Blue	Solid	2	Anlr.Ratio	Left	CH2

Fig 7, Channel separation vs. frequency

IRAUDAMP6 Overview

The IRAUDAMP6 features a 2CH self-oscillating type PWM modulator for the lowest component count, highest performance and robust design. This topology represents an analog version of a second-order sigma-delta modulation having a Class D switching stage inside the loop. The benefit of the sigma-delta modulation, in comparison to the carrier-signal based modulation, is that all the error in the audible frequency range is shifted to the inaudible upper-frequency range by nature of its operation. Also, sigma-delta modulation allows a designer to apply a sufficient amount of error correction.

The IRAUDAMP6 self-oscillating topology consists of following essential functional blocks.

- Front-end integrator
- PWM comparator
- Level shifters
- Gate drivers and MOSFETs
- Output LPF

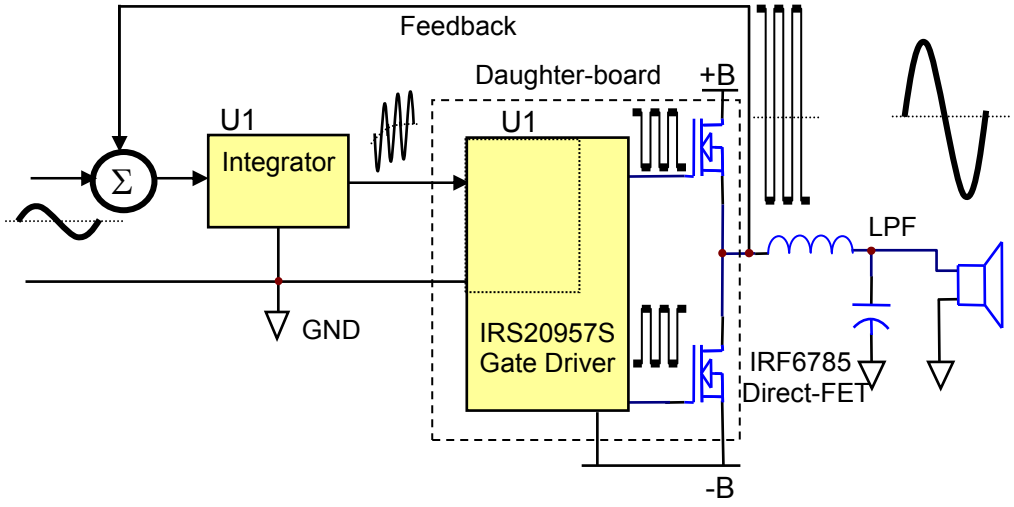


Fig 8, Simplified Block Diagram of Class D Amplifier

Functional Descriptions

Class D Operation

Referring to CH1 as an example, the op-amp U6 forms a front-end second-order integrator with C38, C42 & R50 + R49P. This integrator receives a rectangular feedback waveform from the Class D switching stage and outputs a quadratic oscillatory waveform as a carrier signal. To create the modulated PWM signal, the input signal shifts the average value of this quadratic waveform (through gain relationship between R40,AR154 and R38 + R39) so that the duty varies according to the instantaneous value of the analog input signal. The IRS20957 input comparator processes the signal to create the required PWM signal. This PWM signal is internally level-shifted down to the negative supply rail where this signal is split into two signals, with opposite polarity and added deadtime, for high-side and low-side MOSFET gate signals, respectively. The IRS20957 drives two IRF6785 DirectFET MOSFETs in the power stage to provide the amplified PWM waveform. The amplified analog output is re-created by demodulating the amplified PWM. This is done by means of the LC low-pass filter (LPF) formed by L4 and C34, which filters out the Class D switching carrier signal.

Power Supplies

The IRAUDAMP6 has all the necessary housekeeping power supplies onboard and only requires a pair of symmetric power supplies ranging from ±38 V to ±82 V (+B, GND, -B) for operation. The internally-generated housekeeping power supplies include a ±5 V supply for analog signal processing (preamp, etc.), while a +12 V supply (V_{CC}), referenced to –B, is included to supply the Class D gate-driver stage.

For the externally-applied power, a regulated power supply is preferable for performance measurements, but not always necessary. The bus capacitors, C45 ~ C48 on the motherboard, along with high-frequency bypass-caps C19 ~ C26 on daughter board, address the high-frequency ripple current that result from switching action. In designs involving unregulated power supplies, the designer should place a set of bus capacitors, having enough capacitance to handle the audio-ripple current, externally. Overall regulation and output voltage ripple for the power supply design are not critical when using the IRAUDAMP6 Class D amplifier as the power supply rejection ratio (PSRR) of the IRAUDAMP6 is excellent (Fig 9).

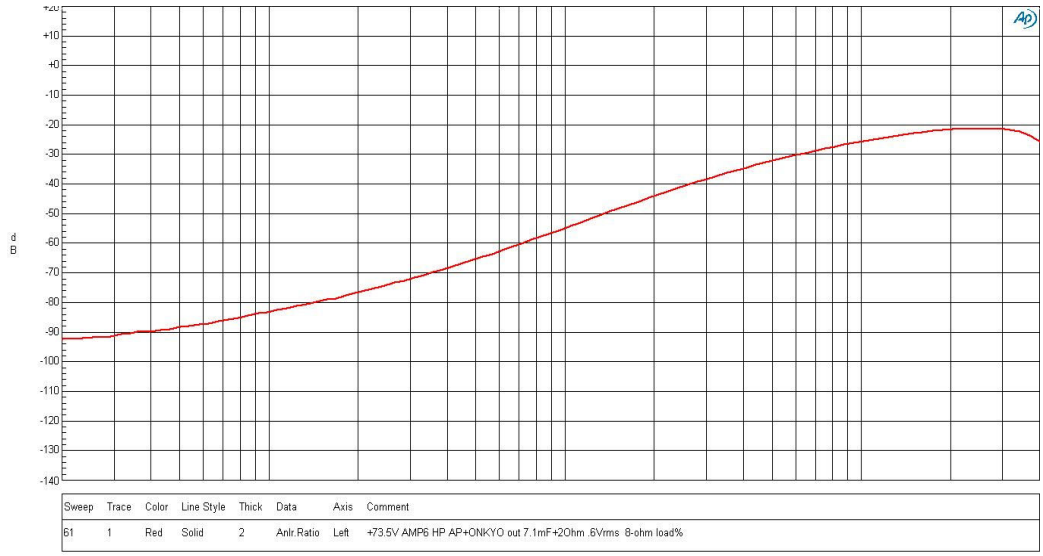


Fig 9, Amp6 Power Supply Rejection Ratio (PSRR)

Bus Pumping

Since the IRAUDAMP6 is a half-bridge configuration, bus pumping does occur. Under normal operation during the first half of the cycle, energy flows from one supply through the load and into the other supply, thus causing a voltage imbalance by pumping up the bus voltage of the receiving power supply. In the second half of the cycle, this condition is opposite, resulting in bus pumping of the other supply.

These conditions worsen bus pumping:

– Lower frequencies (bus-pumping duration is longer per half cycle)
– Higher power output voltage and/or lower load impedance (more energy transfers between supplies)
– Smaller bus capacitors (the same energy will cause a larger voltage increase)

The IRAUDAMP6 has protection features that will shutdown the switching operation if the bus voltage becomes too high (>82 V) or too low (<36 V). One of the easiest countermeasures is to drive both of the channels out of phase so that one channel consumes the energy flow from the other and does not return it to the power supply. Bus voltage detection is only done on the –B supply as the effect of the bus pumping on the supplies is assumed to be symmetrical in amplitude (although opposite in phase).

House Keeping Power Supply

The internally-generated housekeeping power supplies include ±5V for analog signal processing, and +12V supply (V_{CC}) referred to the negative supply rail -B for DirectFET gate drive. The gate driver section of the IRS20957 uses VCC to drive gates of the DirectFETs. V_{CC} is referenced to –B (negative power supply). D6, R4 and C15 form a bootstrap floating supply for the HO gate driver.

Input

A proper input signal is an analog signal ranging from 20Hz to 20kHz with up to 3 V_{RMS} amplitude with a source impedance of no more than 600 Ω. Input signal with frequencies from 30kHz to 60kHz may cause LC resonance in the output LPF, causing a large reactive current flowing through the switching stage, and the LC resonance can activate OCP.

The IRAUDAMP6 has an RC network called a Zobel network (R45 and C36) to damp the resonance and prevent peaking frequency response with light loading impedance. (Fig 10), but is not thermally rated to handle continuous supersonic frequencies. These supersonic input frequencies therefore should be avoided. Separate mono RCA connectors provide input to each of the two channels. Although both channels share a common ground, it is necessary to connect each channel separately to limit noise and crosstalk between channels.

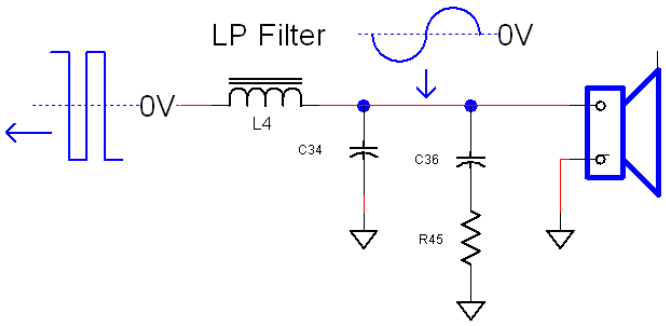


Fig 10 Output Low Pass Filter and Zobel Network

Output

Both outputs for the IRAUDAMP6 are single-ended and therefore have terminals labeled (+) and (-) with the (-) terminal connected to power ground. Each channel is optimized for a 8 Ω speaker load for a maximum output power of 250 W.

Load Impedance

Each channel is optimized for a 8 Ω speaker load in half bridge.

Gain Setting / Volume Control

The IRAUDAMP6 has an internal volume control (potentiometer R130 labeled, “VOLUME”) for gain adjustment. Gain settings for both channels are tracked and controlled by the volume control IC (U_2) setting the gain from the microcontroller IC (U_3). The total gain is a product of the power-stage gain, which is constant (+33 dB), and the input-stage gain that is directly-controlled by the volume adjustment. The volume range is about 100 dB with minimum volume setting to mute the system with an overall gain of less than -60 dB. For best performance in testing, the internal volume control should be set to 1 Vrms input will result in rated output power (250 W into 8 Ω).

Efficiency

Fig 11 shows efficiency characteristics of the IRAUDAMP6. The high efficiency is achieved by following major factors:

1) Low conduction loss due to the DirectFETs offering low $R_{DS(ON)}$
2) Low switching loss due to the DirectFETs offering low input capacitance for fast rise and fall times

Secure dead-time provided by the IRS20957, avoiding cross-conduction

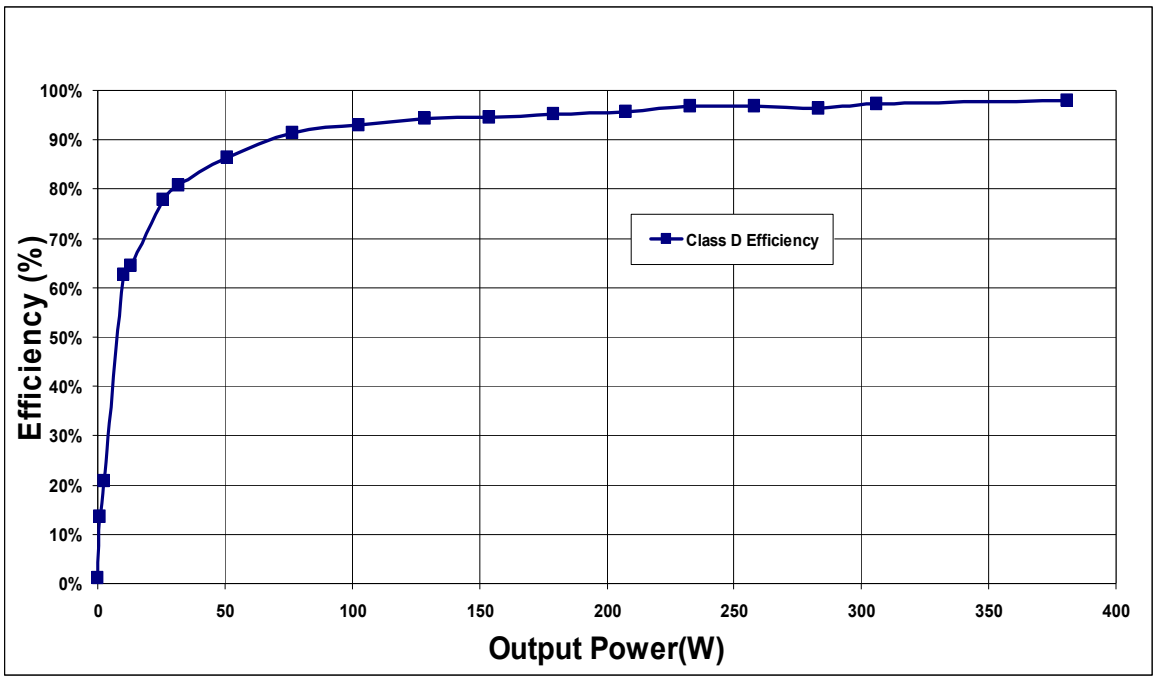


Fig 11, IRAUDAMP6 8 ohms load Stereo, ±B supply = ±73.5V

Output Filter Design and Preamplifier

The audio performance of the IRAUDAMP6 depends on a number of different factors. The section entitled, “Typical Performance” presents performance measurements based on the overall system, including the preamp and output filter. While the preamp and output filter are not part of the Class D power stage, they have a significant effect on the overall performance.

Output filter

The amplified PWM output is reconstructed back to an analog signal by the output LC LPF. Demodulation LC low-pass filter (LPF) formed by L4 and C34, filters out the Class D switching carrier signal leaving the audio output at the speaker load. A single stage output filter can be used with switching frequencies of 400 kHz and greater; a design with a lower switching frequency may require an additional stage of LPF.

Since the output filter is not included in the control loop of the IRAUDAMP6, the reference design cannot compensate for performance deterioration due to the output filter. Therefore, it is important to understand what characteristics are preferable when designing the output filter:

1) The DC resistance of the inductor should be minimal and be within 20 m_Ohm or less.
2) The linearity of the output inductor and capacitor should be high with respect to load current and voltage.

Preamplifier

The preamp allows partial gain of the input signal, and in the IRAUDAMP6, controls the volume. The preamp itself will add distortion and noise to the input signal, resulting in a gain through the Class D output stage and appearing at the output. Even a few micro-volts of noise can add significantly to the output noise of the overall amplifier. In fact, the output noise from the preamp contributes more than half of the overall noise to the system.

It is possible to evaluate the performance without the preamp and volume control, by moving resistors R154and R155 to R157 and R156, respectively. This effectively bypasses the preamp and connects the RCA inputs directly to the Class D power stage input. Improving the selection of preamp and/or output filter, will improve the overall system performance to approach that of the stand-alone Class D power stage.

Self-Oscillating PWM Modulator

The IRAUDAMP6 Class D audio power amplifier features a self-oscillating type PWM modulator for the lowest component count and robust design. This topology represents an analog version of a second-order sigma-delta modulation having a Class D switching stage inside the loop. The benefit of the sigma-delta modulation, in comparison to the carrier-signal based modulation, is that all the error in the audible frequency range is shifted to the inaudible upper-frequency range by nature of its operation. Also, sigma-delta modulation allows a designer to apply a sufficient amount of correction.

The self-oscillating frequency is determined by the total delay time inside the control loop of the system. The delay of the logic circuits, the IRS20957 gate-driver propagation delay, the IRF6785 switching speed, the time-constant of front-end integrator (e.g. R50 + R49, C38 and C42 for CH1)

and variations in the supply voltages are critical factors of the self-oscillating frequency. Under normal conditions, the switching-frequency is around 400 kHz with no audio input signal and a +/- 73.5 V supply.

Adjustments of Self-Oscillating Frequency

The PWM switching frequency in this type of self-oscillating switching scheme greatly impacts the audio performance, both in absolute frequency and frequency relative to the other channels. In absolute terms, at higher frequencies, distortion due to switching-time becomes significant, while at lower frequencies, the bandwidth of the amplifier suffers. In relative terms, interference between channels is most significant if the relative frequency difference is within the audible range. Normally when adjusting the self-oscillating frequency of the different channels, it is best to either match the frequencies accurately, or have them separated by at least 25 kHz.

Potentiometers for adjusting self-oscillating frequency	
R49	Switching frequency for CH1*
R74	Switching frequency for CH2*

*Adjustments have to be done at an idling condition with no signal input.

Switches and Indicators

There are two different indicators on the reference design:

- A Red LED, signifying a fault / shutdown condition when lit.
- A green LED on the motherboard, signifying conditions are normal and no fault condition is present.

There are three switches on the reference design:

- Switch S1 is an oscillator selector. This three-position switch is selectable for internal self-oscillator (middle position – “SELF”), or either internal (“INT”) or external (“EXT”) clock synchronization.
- Switch S2 is an internal clock-sync phase difference selector. This feature allows the designer to modify the clock-sync phase separation in order to avoid synchronized switching noise interference. With S2 is set to OFF, the sync-clock phase difference value is 180°.With S2 is set to INT, the clock-sync phase is set by potentiometer R100. With S2 is set to STG, one channel’s clock is quadrature-lagging
- Switch S3 is a trip and reset push-button. Pushing this button has the same effect of a fault condition. The circuit will restart about three seconds after the shutdown button is released.

Startup and Shutdown

One of the most important aspects of any audio amplifier is the startup and shutdown procedures. Typically, transients occurring during these intervals can result in audible pop- or click-noise on the output speaker. Traditionally, these transients have been kept away from the speaker through the use of a series relay that connects the speaker to the audio amplifier only after the startup transients have passed and disconnects the speaker prior to shutting down the amplifier. It is interesting to note that the audible noise of the relay opening and closing is not considered “click noise”, although in some cases, it can be louder than the click noise of non-relay-based solutions.

The IRAUDAMP6 does not use any series relay to disconnect the speaker from the audible transient noise, but rather a shunt-based click noise reduction circuit that yields audible noise levels that are far less that those generated by the relays they replace. This results in a more reliable, superior performance system.

For the startup and shutdown procedures, the activation (and deactivation) of the click-noise reduction circuit, the Class D power stage and the audio input (mute) controls have to be sequenced correctly to achieve the required click noise reduction. The overall startup sequencing, shutdown sequencing and shunt circuit operation are described below.

Click and POP Noise Reduction

To reduce the turn-on and turn-off click noise, a low impedance shunting circuit is used to minimize the voltage across the speaker during transients. For this purpose, the shunting circuit must include the following characteristics:

1) An impedance significantly lower than that of the speaker being shunted. In this case, the shunt impedance is ~100 mΩ, compared to the normal 8 Ω speaker impedance.
2) When deactivated, the shunting circuit must be able to block voltage in both directions due to the bi-directional nature of the audio output.
3) The shunt circuit requires some form of OCP. If one of the Class D output MOSFETs fails, or is conducting when the speaker mute (SP MUTE) is activated, the shunting circuit will effectively try to short one of the two supplies (+/-B).

The implemented click-noise reduction circuit is shown in Figure 12. Before startup or shutdown of the Class D power stage, the click-noise reduction circuit is activated through the SP MUTE control signal. With SP MUTE signal high, the speaker output is shorted through the back-to-back MOSFETs (U5 for Channel 1) with an equivalent on resistance of about 100 mΩ. The two transistors (U7 for Channel 1) are for the OCP circuit.

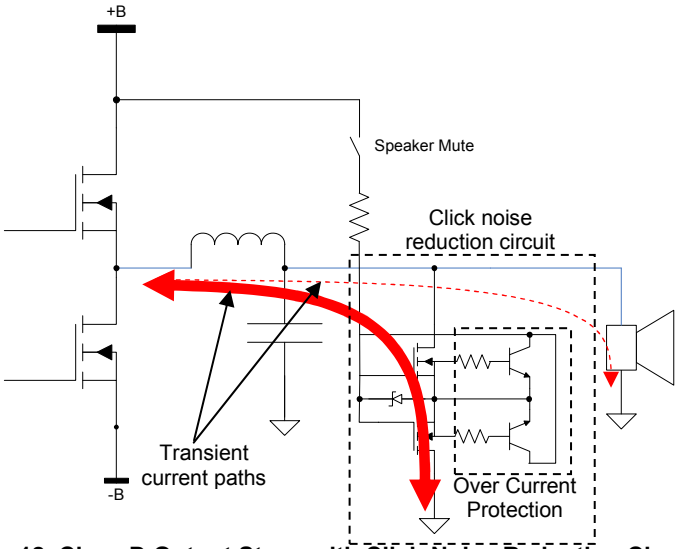


Fig 12, Class D Output Stage with Click-Noise Reduction Circuit

Startup and Shutdown Sequencing

The IRAUDAMP6 sequencing is achieved through the charging and discharging of the CStart capacitor C66. This, coupled to the charging and discharging of the voltage of CSD (C11 on daughter board for CH1) of the IRS20957, is all that is required for complete sequencing. The conceptual startup and shutdown timing diagrams are show in Figure 13.

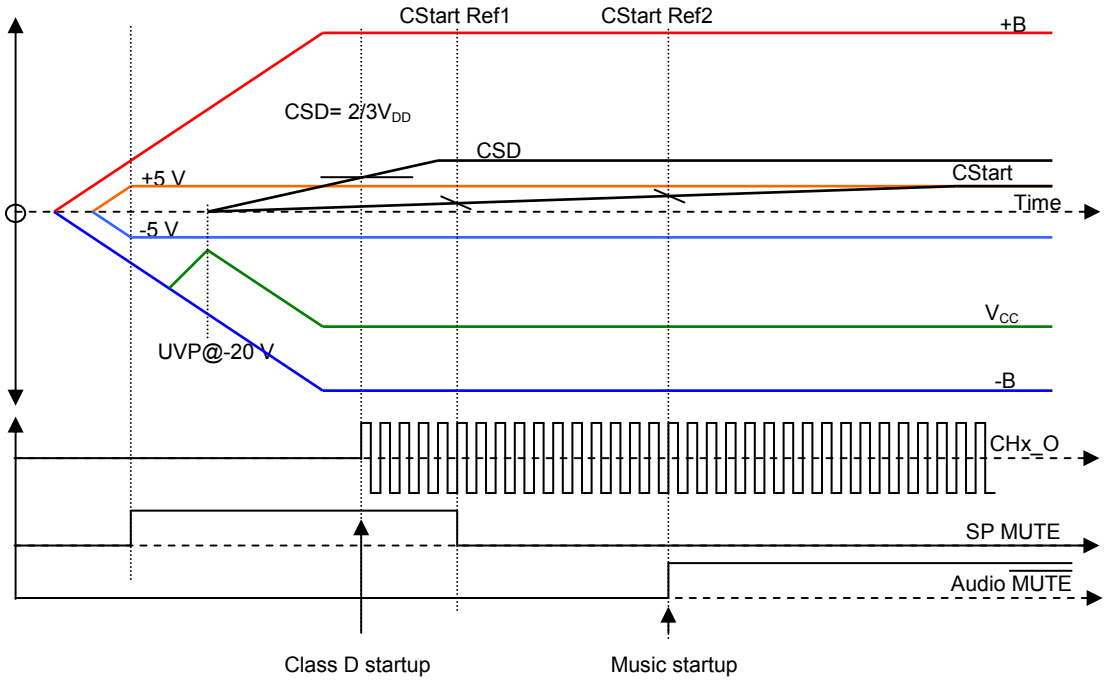


Fig 13, Conceptual Startup Sequencing of Power Supplies and Audio Section Timing

For startup sequencing, +/-B supplies startup at different intervals. As +/-B supplies reach +5 V and -5 V respectively, the analog supplies (+/-5 V) start charging and, once +B reaches ~16 V, V_{CC} charges. Once –B reaches -20 V, the UVP is released and CSD and CStart start charging. Once +/-5 V is established, the click-noise reduction circuit is activated through the SP MUTE control signal. As CSD reaches two-thirds V_{DD}, the Class D stage starts oscillating. Once the startup transient has passed, SP MUTE is released (CStart reaches Ref1). The Class D amplifier is now operational, but the preamp output remains muted until CStart reaches Ref2. At this point, normal operation begins. The entire process takes less than three seconds.

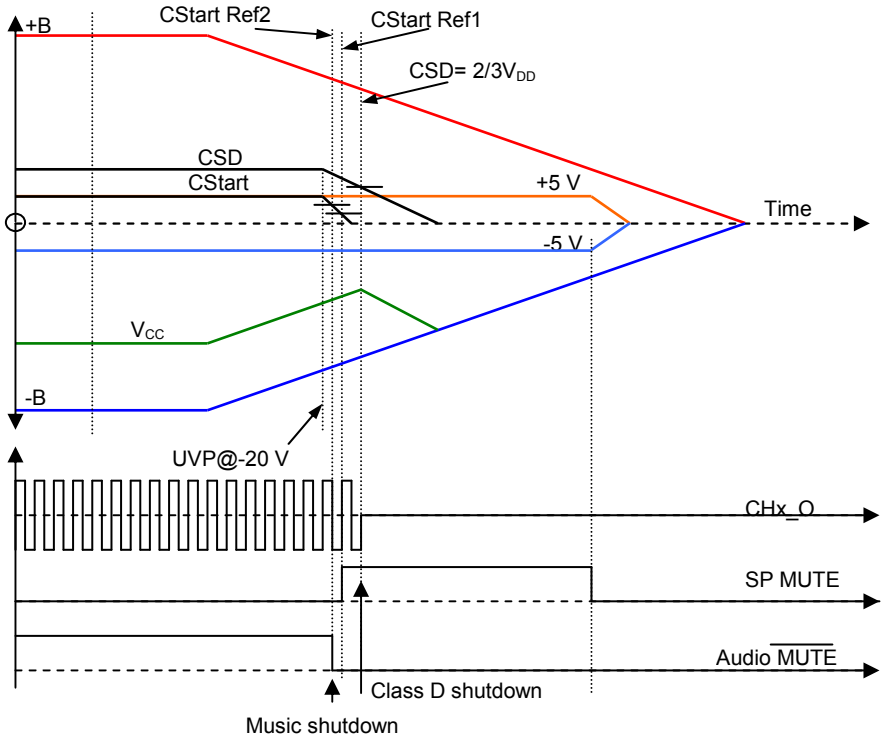


Fig 14, Conceptual Shutdown Sequencing of Power Supplies and Audio Section Timing

Shutdown sequencing is initiated once UVP is activated. As long as the supplies do not discharge too quickly, the shutdown sequence can be completed before the IRS20957 trips UVP. Once UVP is activated, CSD and CStart are discharged at different rates. In this case, threshold Ref2 is reached first and the preamp audio output is muted. Once CStart reaches threshold Ref1, the click-noise reduction circuit is activated (SP MUTE). It is then possible to shutdown the Class D stage (CSD reaches two-thirds V_{DD}). This process takes less than 200 ms.

For any external fault condition (OTP, OVP, UVP or DCP – see “Protection”) that does not lead to power supply shutdown, the system will trip in a similar manner as described above. Once the fault is cleared, the system will reset (similar sequence as startup).

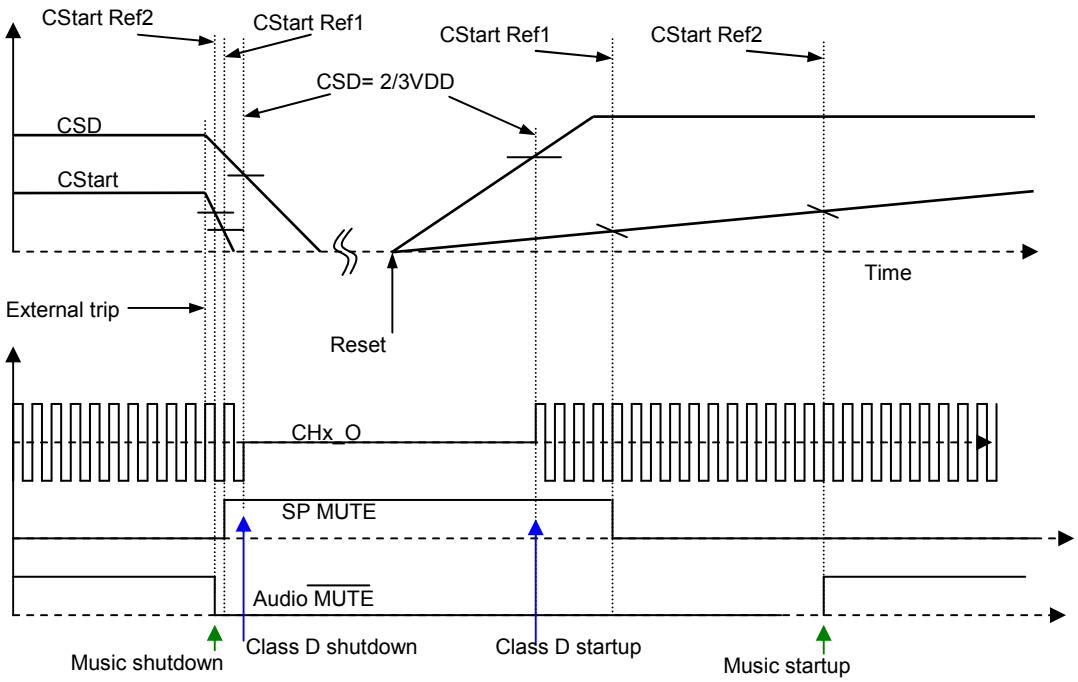


Fig 15, Conceptual Click Noise Reduction Sequencing at Trip and Reset

Selectable Dead-time

The IRS20957 determines its dead-time based on the voltage applied to the DT pin. An internal comparator translates which pre-determined dead-time is being used by comparing the DT voltage with internal reference voltages. A resistive voltage divider from V_{CC} sets threshold voltages for each setting, negating the need for a precise absolute voltage to set the mode. The threshold voltages between dead-time settings are set internally, based on different ratios of V_{CC} as indicated in the diagram below. In order to avoid drift from the input bias current of the DT pin, a bias current of greater than 0.5 mA is suggested for the external resistor divider circuit. Suggested values of resistance that are used to set a dead-time are given below. Resistors with up to 5% tolerance can be used.

Dead-time mode	Dead-time	R22	R19	DT Voltage
DT1	~15 ns	<10kΩ	Open	V_{CC}
DT2	~25 ns	5.6kΩ	4.7kΩ	0.46(V_{CC})
DT3	~35 ns	8.2kΩ	3.3kΩ	0.29(V_{CC})
DT4	~45 ns	Open	<10kΩ	COM

Recommended Resistor Values for Dead Time Selection

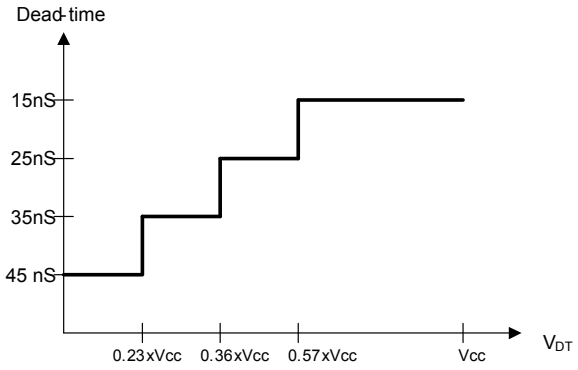


Fig 17 Dead-time Settings vs. V_{DT} Voltage

Level Shifters

The internal input level-shifter transfers the PWM signal down to the low-side gate driver section. The gate driver section has another level-shifter that level shifts up the high-side gate signal to the high-side gate driver section.

Protection System Overview

The IRS20957 integrates over current protection (OCP) inside the IC. The rest of the protections, such as over-voltage protection (OVP), under-voltage protection (UVP), and over temperature protection (OTP), are detected externally to the IRS20957.

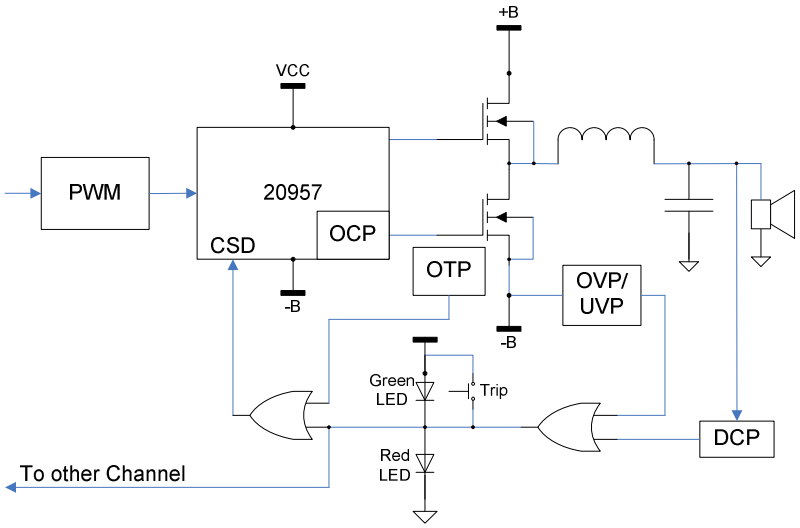


Fig 18, Functional Block Diagram of Protection Circuit Implementation

The external shutdown circuit will disable the output by pulling down CSD pins . If the fault condition persists, the protection circuit stays in shutdown until the fault is removed.

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Over-Current Protection (OCP)

The OCP internal to the IRS20957 shuts down the IC if an OCP is sensed in either of the output MOSFETs. For a complete description of the OCP circuitry, please refer to the IRS20957 datasheet. Here is a brief description:

Low-Side Current Sensing

The low-side current sensing feature protects the low side DirectFET from an overload condition from negative load current by measuring drain-to-source voltage across $R_{DS(ON)}$ during its on state. OCP shuts down the switching operation if the drain-to-source voltage exceeds a preset trip level.

The voltage setting on the OCSET pin programs the threshold for low-side over-current sensing. When the VS voltage becomes higher than the OCSET voltage during low-side conduction, the IRS20957 turns the outputs off and pulls CSD down to -VSS.

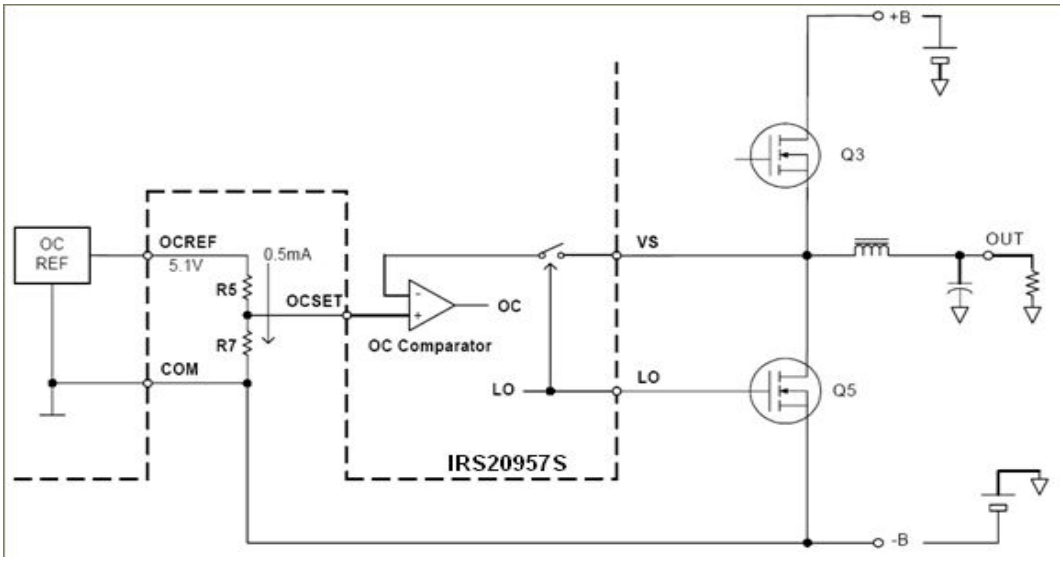

Fig 19 Simplified Functional Block Diagram of Low-Side Current Sensing

High-Side Current Sensing

The high-side current sensing protects the high side DirectFET from an overload condition from positive load current by measuring drain-to-source voltage across $R_{DS(ON)}$ during its on state. OCP shuts down the switching operation if the drain-to-source voltage exceeds a preset trip level.

High-side over-current sensing monitors drain-to-source voltage of the high-side DirectFET during the on state through the CSH and VS pins. The CSH pin detects the drain voltage with reference to the VS pin, which is the source of the high-side DirectFET. In contrast to the low-side current sensing, the threshold of the CSH pin to trigger OC protection is internally fixed at 1.2V. An external resistive divider R30, R32 and R34 are used to program a threshold . An external reverse blocking diode D8 is required to block high voltage feeding into the CSH pin during low-side conduction. By subtracting a forward voltage drop of 0.6V at D8, the minimum threshold which can be set for the high-side is 0.6V across the drain-to-source.

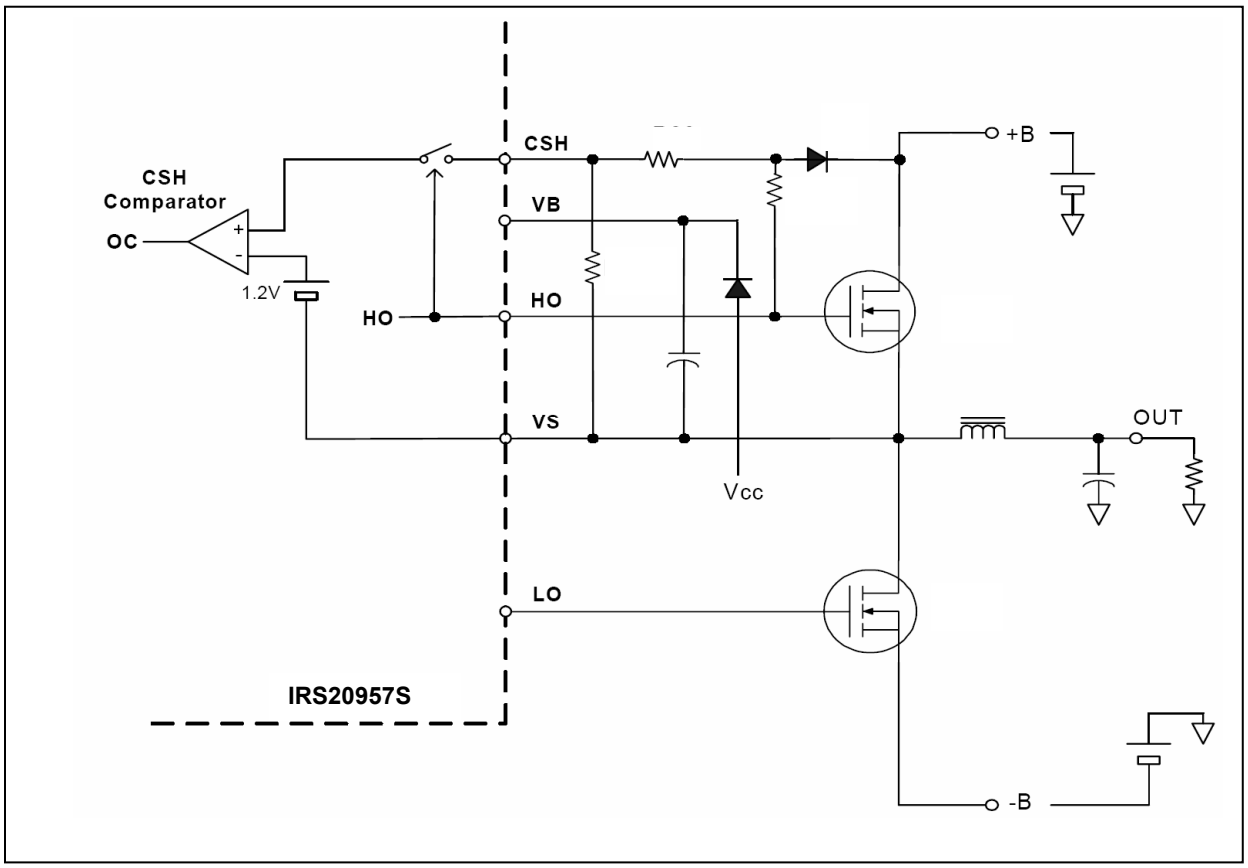

Fig 20, Simplified Functional Block Diagram of High-Side Current Sensing

Over-Voltage Protection (OVP)

OVP is provided externally to the IRS20957. OVP shuts down the amplifier if the bus voltage between GND and -B exceeds 82V. The threshold is determined by a Zener diode Z9. OVP protects the board from harmful excessive supply voltages, such as due to bus pumping at very low frequency-continuous output in stereo mode.

Under-Voltage Protection (UVP)

UVP is provided externally to the IRS20957. UVP prevents unwanted audible noise output from unstable PWM operation during power up and down. UVP shuts down the amplifier if the bus voltage between GND and -B falls below a voltage set by Zener diode Z8.

Speaker DC-Voltage Protection (DCP)

DCP protects speakers against DC output current feeding to its voice coil. DC offset detection detects abnormal DC offset and shuts down PWM. If this abnormal condition is caused by a MOSFET failure because one of the high-side or low-side MOSFETs short circuited and remained in the on state, the power supply needs to be cut off in order to protect the speakers. Output DC offset greater than ±2.1V triggers DCP.

Offset Null (DC Offset) Adjustment

The IRAUDAMP6 is designed such that no output-offset nullification is required. DC offsets are tested to be less than ±5 mV.
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Over-Temperature Protection (OTP)

A separate PTC resistor is placed in close proximity to the high-side IRF6785 DirectFET MOSFET for each of the amplifier channels. If the resistor temperature rises above 90 °C, the OTP is activated. The OTP protection will only shutdown the relevant channel by pulling low the CSD pin and will recover once the temperature at the PTC has dropped sufficiently. This temperature protection limit yields a PCB temperature at the MOSFET of about 100 °C. This setting is limited by the PCB material and not by the operating range of the MOSFET.

Thermal Considerations

With this high efficiency, the IRAUDAMP6 design can handle one-eighth of the continuous rated power, which is generally considered to be a normal operating condition for safety standards. Without increasing the size of a heatsink or forced air-cooling, the daughter board cannot handle continuous rated power.

Thermal Interface Material's Pressure Control

The DirectFET MOSFETs are attached to a heatsink with a thermal interface material (TIM). The pressure between DirectFET and TIM is controlled by depth of Heat Spreader's groove. Choose TIM which is recommended by **IR**. (Refer to AN-1035 for more details). TIM's manufacturer thickness, conductivity, & etc. determine pressure requirement. Below shows selection options recommended:

Common Thermal Interface Materials Cost Trades

Mfr.	Material	Type	Thickness (mils)	Pressure Required	Dispense/ Apply	Clips/ Screws	Can be applied to heat sink?	Mechanical Placement?
Dow Corning	1-4173	1 part heat-cured adhesive	#	Yes	Dispense	Clips	N	Y
Dow Corning	SE 4451	2 part heat-cured adhesive	#	Yes	Dispense	Clips	N	Y
Dow Corning	3-6652	2 part heat-cured adhesive	#	Yes	Dispense	Clips	N	Y
Dow Corning	TP-1500 Pad	Tacky - Phase Change at 52° C	10	>5psi, 20psi typ.	Apply	Clips	Y	Y
Bergquist	Gap Pad 3000	conformable filled polymer sheet	15	>10psi	Apply	Clips/ Screws	N	Y
Bergquist	Gap Pad 2000	conformable filled polymer sheet	10	>10psi	Apply	Clips/ Screws	N	Y
Bergquist	Hi Flow 300	Phase Change at 55°C	2.4	>10psi	Apply	Clips	Y	*
Bergquist	Hi Flow 625	Phase Change at 65°C	5	>10psi	Apply	Clips	Y	*
Bergquist	Hi Flow 818	Phase Change at 65°C	5.5	>10psi	Apply	Clips	Y	*
Bergquist	Sil Pad 800	Conformable silicone elastomer	5	>10 higher better	Apply	Clips/ Screws	Y	*
Bergquist	Sil Pad 900	Conformable silicone elastomer	9	>10 higher better	Apply	Clips/ Screws	Y	*
Bergquist	Sil Pad A1500	Conformable silicone elastomer	10	10-50psi	Apply	Clips/ Screws	Y	*
Bergquist	Sil Pad A2000	Conformable silicone elastomer	10	10-50psi	Apply	Clips/ Screws	Y	*
Bergquist	Bond Ply 100	Pressure sensitive adhesive tape	5	>10psi	Apply	Clips	Y	Y
Bergquist	Bond Ply 100	Pressure sensitive adhesive tape	11	>10psi	Apply	Clips	Y	Y
Thermoset (Lord)	Gelease MG-120	Thermal grease/gel	#	5-7lbf	Dispense	Clips	N	Y
Shin Etsu	X-23-7783D	Thermal grease	##	-	Dispense	Clips	N	Y
Shin Etsu	X-23-7762	Thermal grease	##	-	Dispense	Clips	N	Y

Fig 21, TIM Information

Check the TIM's compression deflection with constant rate of strain (example as Fig.10) base on manufacturer's datasheet. According to the stress requirement, find strain range for the TIM. Then, calculate heat spreader groove depth as below:

Groove Depth=DirectFET's Height +TIM's Thickness*strain

**DirectFET's height should be measured from PCB to the top of DirectFET after reflow. The average height of IRF6785 is 0.65mm.

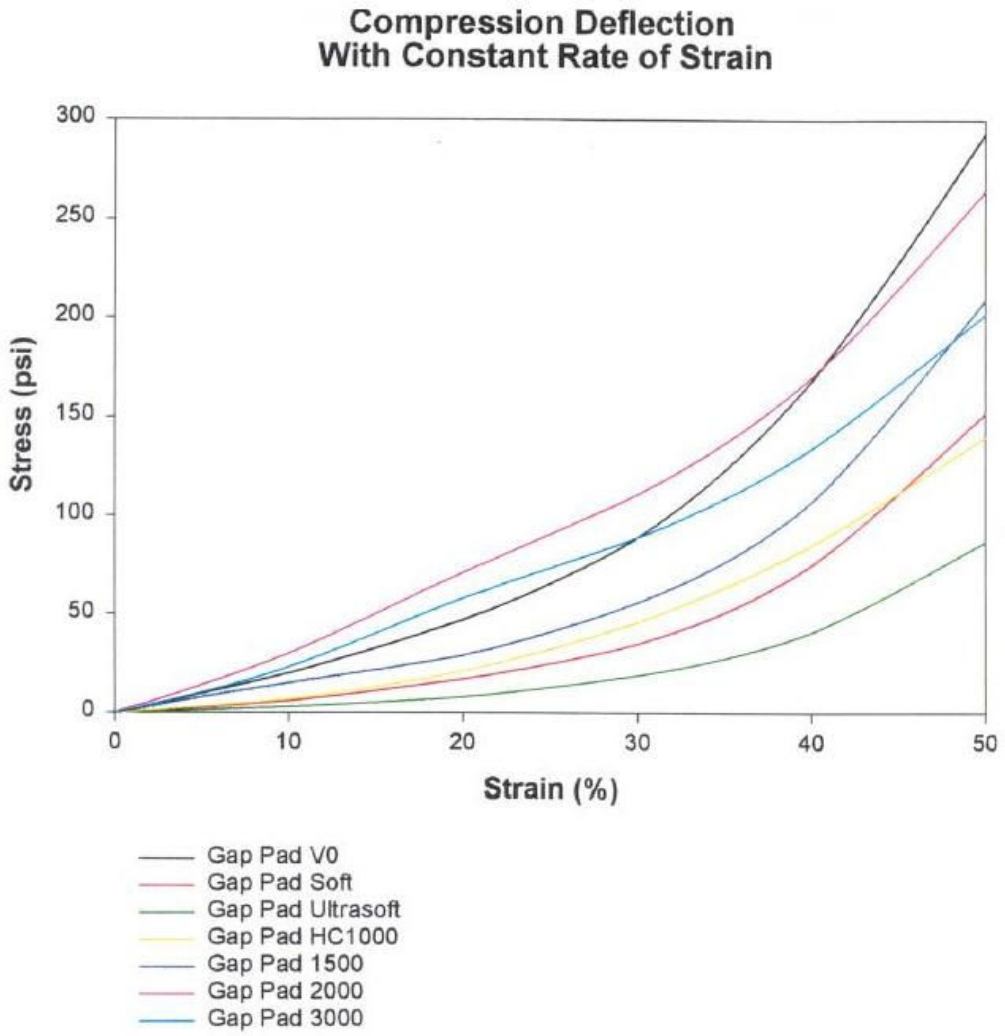

Fig 22, compression deflection with constant rate of strain

AMP6 Thermal pad pressure control calculation

PCB thickness=1.6mm

Heatsink thickness=2.54mm Weight=27.1g
(DCC58375837L-18B http://www.alphanovatech.com/c_dcc5837ue.html)

Thermal Pad thickness=2.03mm
(BER164-ND
http://search.digikey.com/scripts/DkSearch/dksus.dll?lang=en&site=US&WT.z_homepage_link=hp_go_button&KeyWords=BER164-ND+)

Spring : S001YJ1D FL=6.4mm SL=2.9mm (http://www.alphanovatech.com/c_springe.html)

Pressure Required:10-50psi(Fig21)

Clearance between push pin and heatsink:

1, Without Spring:
Pin height-PCB thickness-heatsink height(substructure height)-thermal pad thickness
=8.5-1.6-2.54-2.03=2.33mm

2, With Spring:(Assumption: pressure=50pci strain=30% according to Fig22)
Pin height-PCB thickness-heatsink height(substructure height)-thermal pad thickness*70%
=8.5-1.6-2.54-1.421=2.939mm=expected length

Spring length change=Free length-expected length=6.4-2.939=3.461mm
Spring strength= Spring length change*spring rate=3.461*5.19=17.96N
Strength to PCB=4* Spring strength+(heatsink weight*0.00098)=4*17.96+27.1*0.00098=**71.87N**
To have 50psi pressure we need strength as below:
1kg/cm^2=14.21psi; 1g/cm^2=0.0098N/cm^2
=>50psi=3.51kg/cm^2=3.51*1000*0.0098nN/cm^2=34.398N/cm^2

Heatsink S=5.79*3.68cm^2=21.31cm^2

Total strength we need=34.398*21.31N=**732.93N>>71.87N**
=>So spring does not have enough strength support push pin more than solid height.

Then, spring height=solid height
Clearance between push pin and heatsink=2.9mm
Pin height-PCB thickness-heatsink height (substructure height)-thermal pad thickness***X**%
X=72%

According to Fig22
When Strain=28%, Stress=45psi within the required range 10-50psi

Short Circuit Protection Response

Figs 23-24 show over current protection reaction time of the IRAUDAMP6 in a short circuit event. As soon as the IRS20957 detects an over current condition, it shuts down PWM. After one second, the IRS20957 tries to resume the PWM. If the short circuit persists, the IRS20957 repeats try and fail sequences until the short circuit is removed.

Short Circuit in Positive and Negative Load Current

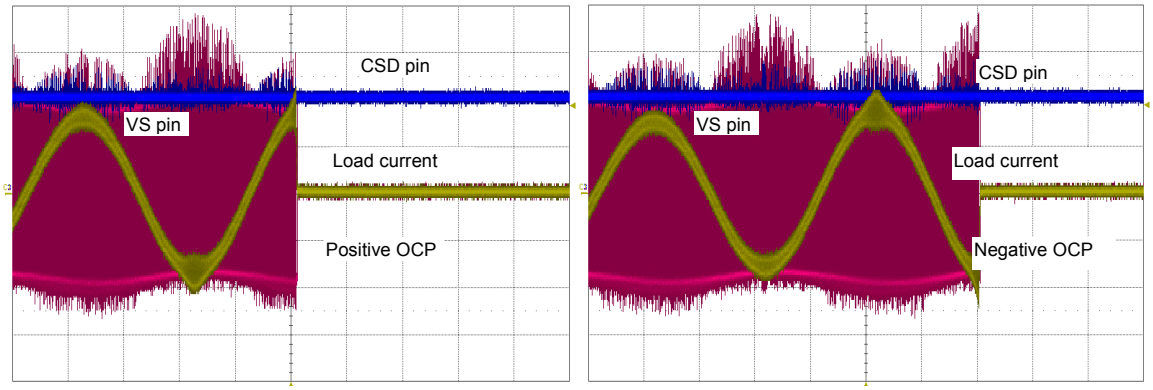

Fig 23, Positive and Negative OCP Waveforms

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OCP Waveforms Showing CSD Trip and Hiccup

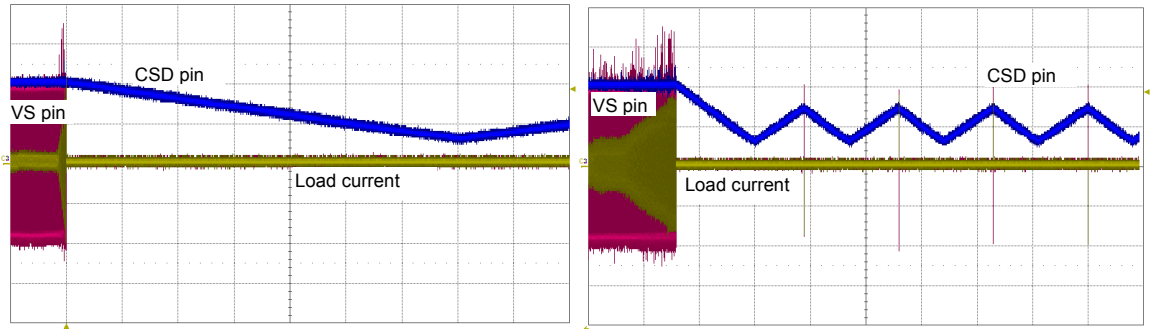
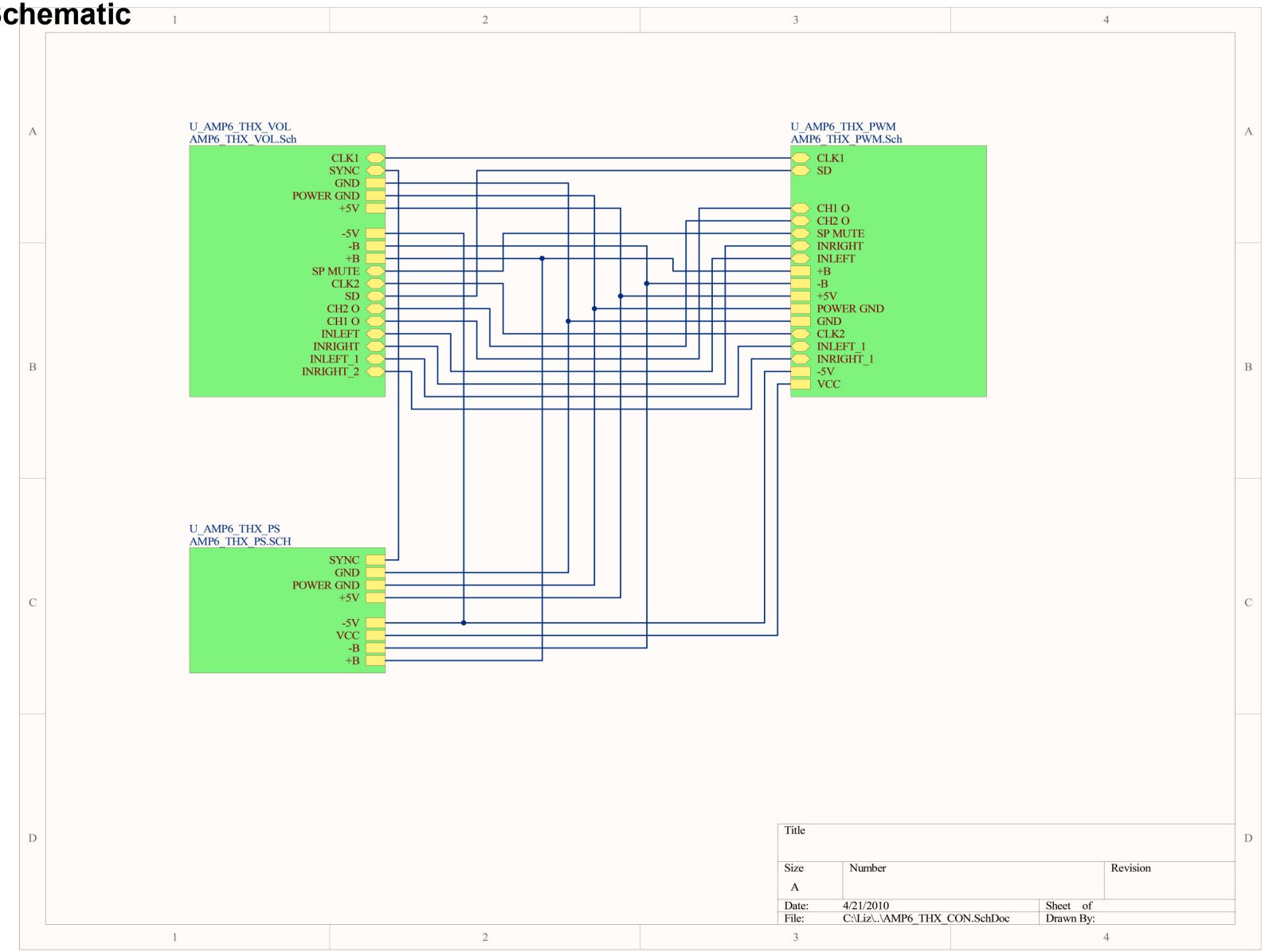
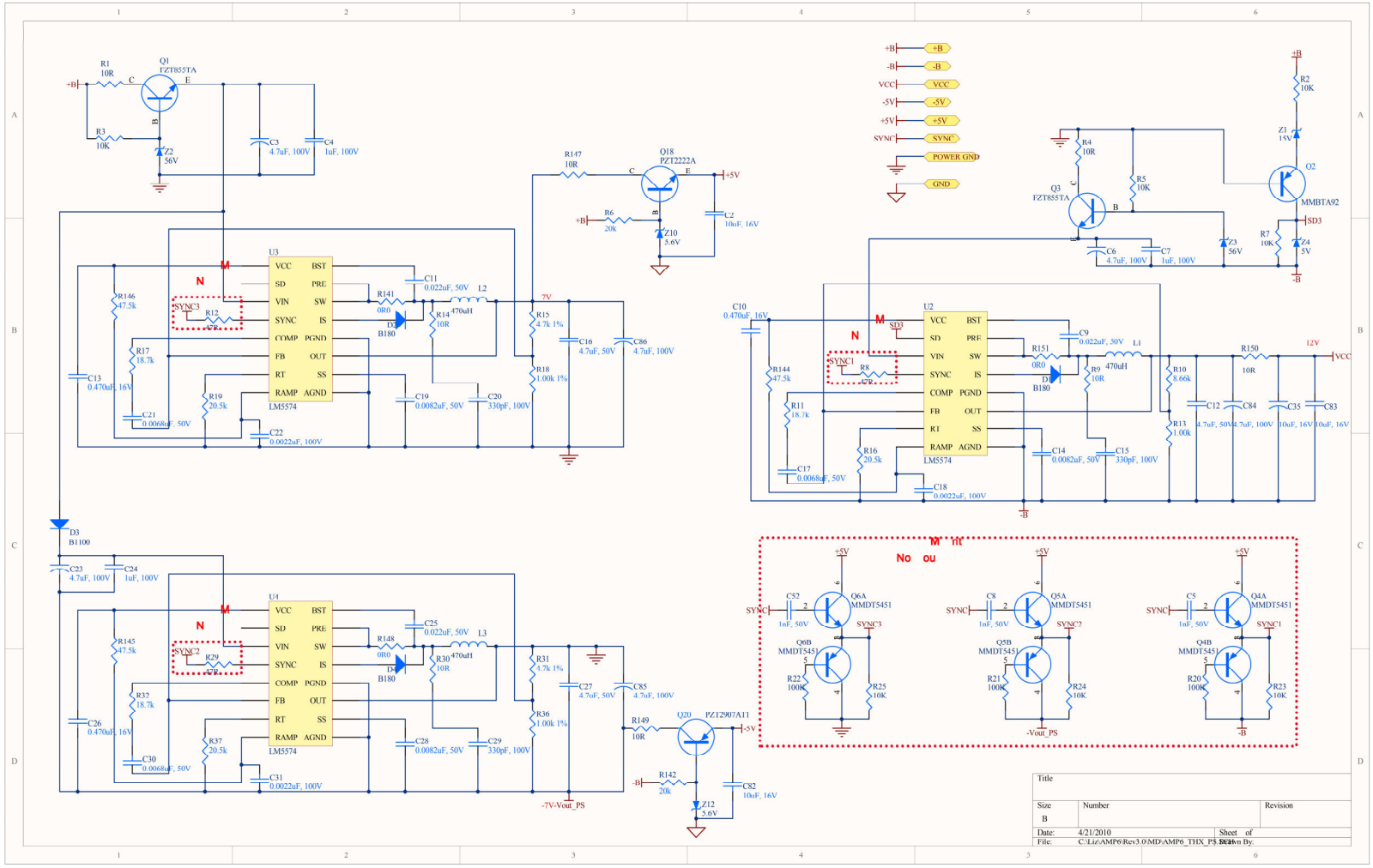
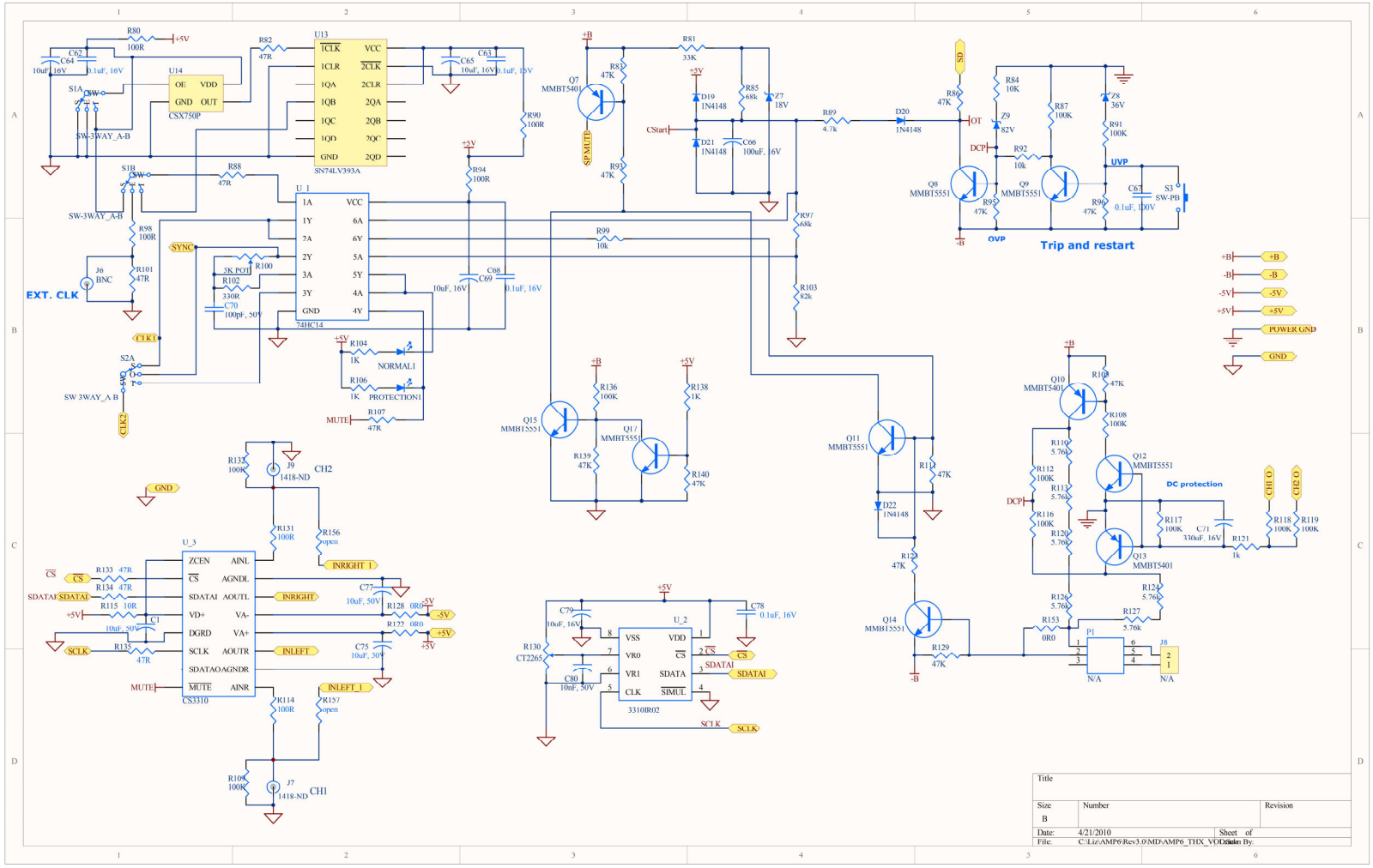


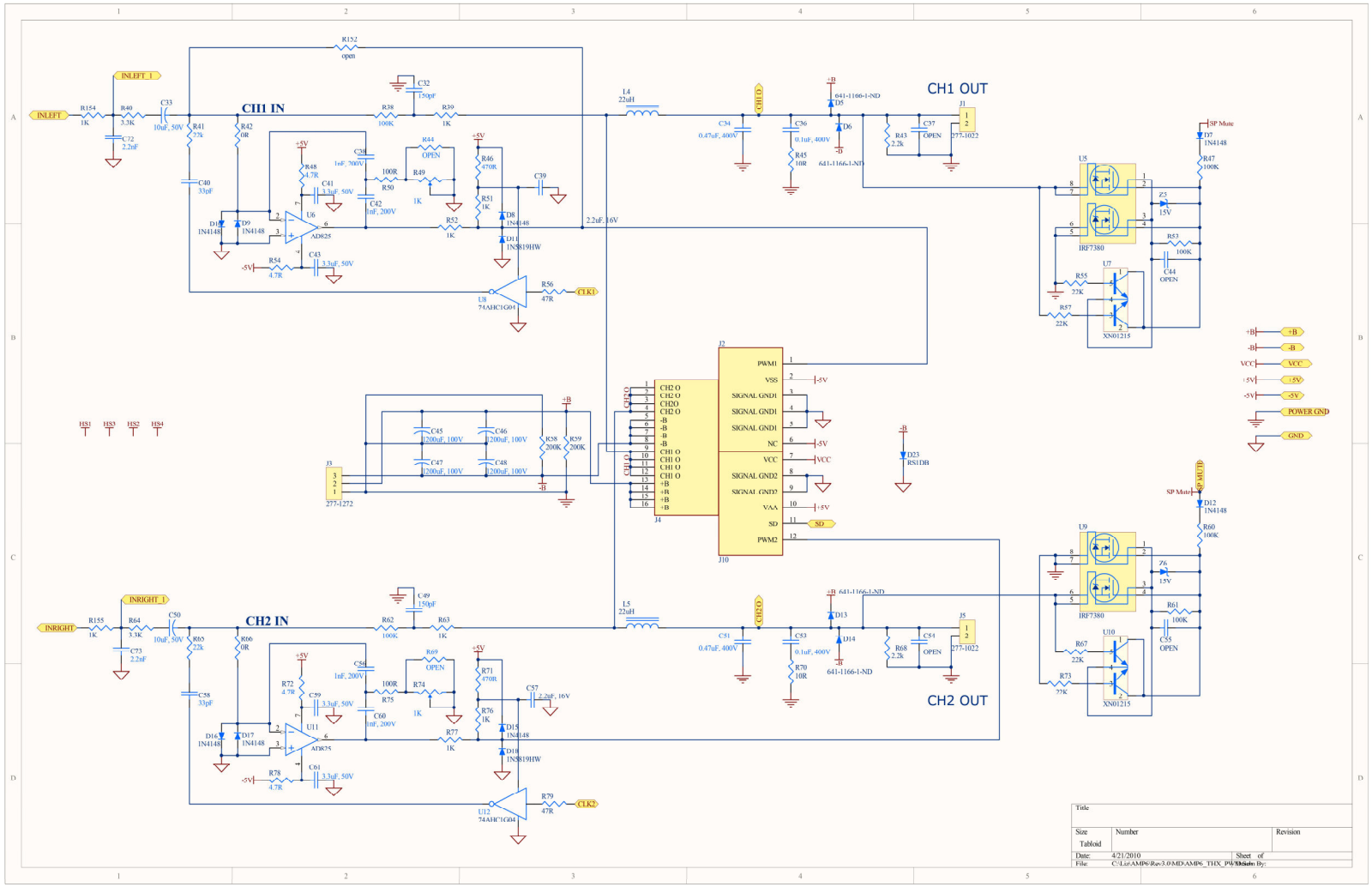
Fig 24 OCP Response with Continuous Short Circuit

Schematic


U_AMP6_THX_VOL
AMP6_THX_VOL.Sch
CLK1
SYNC
GND
POWER GND
+5V
-5V
-B
+B
SP MUTE
CLK2
SD
CH2 O
CH1 O
INLEFT
INRIGHT
INLEFT_1
INRIGHT_2
U_AMP6_THX_PWM
AMP6_THX_PWM.Sch
CLK1
SD
CH1 O
CH2 O
SP MUTE
INRIGHT
INLEFT
+B
-B
+5V
POWER GND
GND
CLK2
INLEFT_1
INRIGHT_1
-5V
VCC
U_AMP6_THX_PS
AMP6_THX_PS.SCH
SYNC
GND
POWER GND
+5V
-5V
VCC
-B
+B
Title
Size
A
Number
Revision
Date: 4/21/2010
Sheet of
File: C:\Liz\..\AMP6_THX_CON.SchDoc
Drawn By:


+B
-B
VCC
-5V
+5V
SYNC
POWER GND
GND
LM5574
VCC
BST
SD
PRE
VIN
SW
SYNC
IS
COMP
PGND
FB
OUT
RT
SS
RAMP
AGND
MMDT5451
MMBTA92
FZT855TA
PZT2222A
PZT2907AT1
B1100
B180
-7V-Vout_PS
-Vout_PS
Title
Size
B
Number
Revision
Date:
4/21/2010
Sheet of
File:
Drawn By:


EXT. CLK
Trip and restart
DC protection
POWER GND
GND
CH2
CH1
NORMAL1
PROTECTION1
INRIGHT_1
INRIGHT
INLEFT
INLEFT_1
SYNC
MUTE
SCLK
SDATAI
CS
OVP
UVP
DCP
Title
Size
B
Number
Revision
Date: 4/21/2010
Sheet of
File: C:\Liz\AMP6\Rev3.0\MD\AMP6_THX_VDD.sch
Drawn By:


CH1 IN
CH1 OUT
CH2 IN
CH2 OUT
INLEFT
INRIGHT
CLK1
CLK2
SD
PWM1
PWM2
VSS
VCC
VAA
NC
SIGNAL GND1
SIGNAL GND2
SP Mute
POWER GND
GND
IRF7380
XN01215
AD825
74AHC1G04
1N5819HW
1N4148
277-1022
RS1DB
641-1166-1-ND

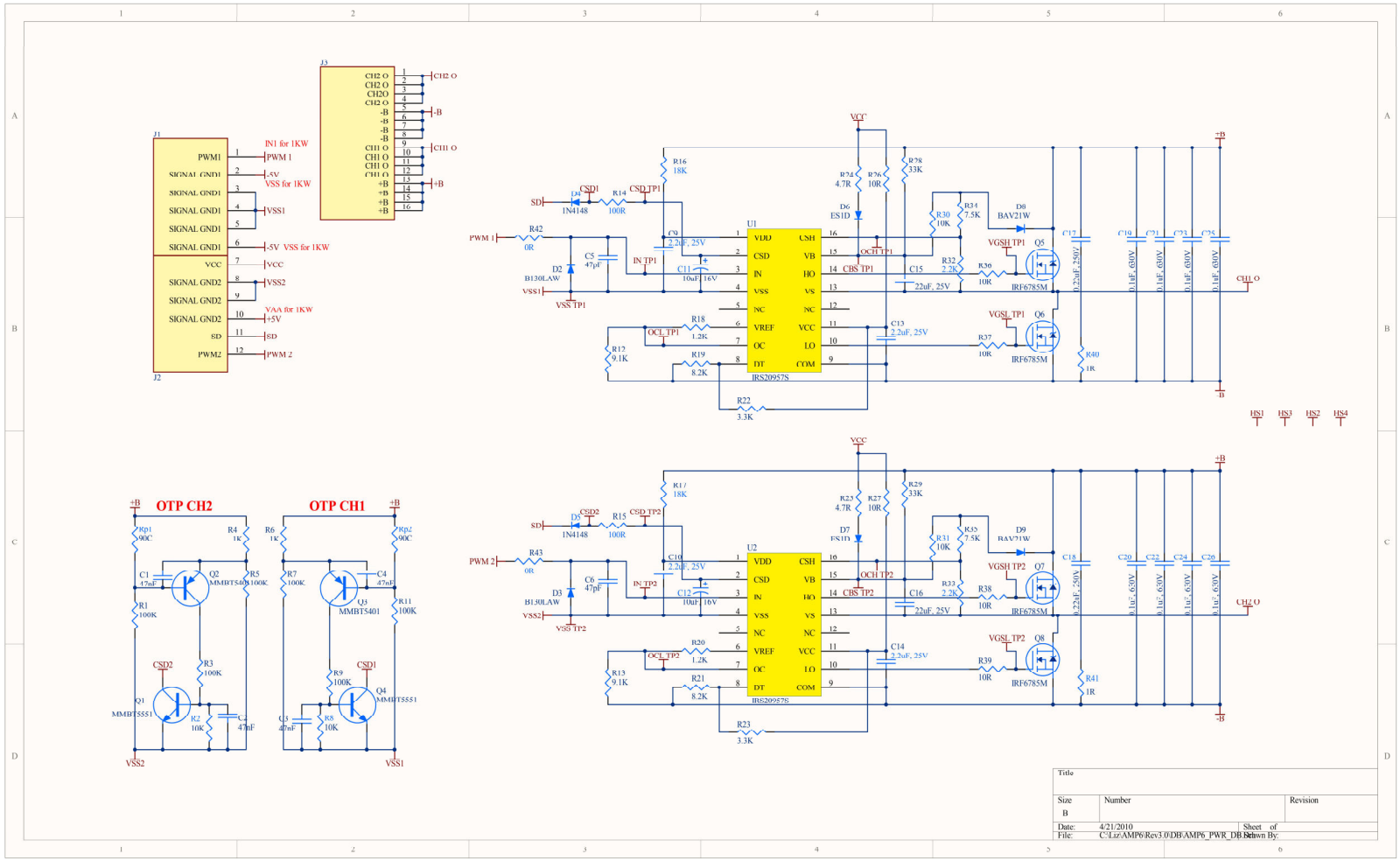


Fig 22 IRAUDAMP6 *Schematic*

IRAUDAMP6 Fabrication Materials

Table 1 IRAUDAMP6 Mother board's Materials

No	P/N	Designator	Description	Quantity	Vendor
1	565-1106-ND	C1, C33, C50, C75, C77	CAP 10UF 50V ELECT SMG RAD	5	Digikey
2	PCC13491CT-ND	C2, C82, C83	CAP 10UF 16V CERAMIC X7R 1206	3	Digikey
3	565-1147-ND	C3, C6, C23, C84, C85, C86	CAP 4.7UF 100V ELECT SMG RAD	6	Digikey
4	490-1857-1-ND	C4, C7, C24	CAP CER 1.0UF 100V 10% X7R 1210	3	Digikey
5	490-1644-1-ND	C9, C11, C25	CAP CER 22000PF 50V 5% C0G 0805	3	Digikey
6	478-1403-1-ND	C10, C13, C26	CAP CERM .47UF 10% 16V X7R 0805	3	Digikey
7	490-1864-1-ND	C12, C16, C27	CAP CER 4.7UF 50V 10% X7R 1210	3	Digikey
8	445-2685-1-ND	C14, C19, C28	CAP CER 8200PF 50V C0G 5% 0805	3	Digikey
9	PCC1982CT-ND	C15, C20, C29	CAP 330PF 100V CERAMIC X7R 0805	3	Digikey
10	478-3772-1-ND	C17, C21, C30	CAP CERM 6800PF 5% 50V X7R 0805	3	Digikey
11	478-3746-1-ND	C18, C22, C31	CAP CERM 2200PF 5% 100V X7R 0805	3	Digikey
12	445-2378-1-ND	C32, C49	CAP CER 150PF 3000V C0G 10% 1812	2	Digikey
13	338-1178-ND	C34, C51	CAP .33UF 2000VDC POLY FILM AXL	2	Digikey
14	PCE3101CT-ND	C35, C64, C65, C69, C79	CAP 10UF 16V ELECT FC SMD	5	Digikey
15	495-1311-ND	C36, C53	CAP .10UF 400V METAL POLYPRO	2	Digikey
16	PCC2009CT-ND	C38, C42, C56, C60	CAP CERAMIC 1000PF 200V NP0 1206	4	Digikey
17	PCC1931CT-ND	C39, C57	CAP 2.2UF 16V CERAMIC X7R 1206	2	Digikey
18	478-1281-1-ND	C40, C58	CAP CERM 33PF 5% 100V NP0 0805	2	Digikey
19	445-1432-1-ND	C41, C43, C59, C61	CAP CER 3.3UF 50V X7R 20% 1210	4	Digikey
20	565-1161-ND	C45, C46, C47, C48	CAP 1200UF 100V ELECT SMG RAD	4	Digikey
21	PCC1812CT-ND	C62, C63, C68, C78	CAP .1UF 16V CERAMIC X7R 0805	4	Digikey
22	565-1037-ND	C66	CAP 100UF 16V ELECT SMG RAD	1	Digikey
23	445-1418-1-ND	C67	CAP CER .10UF 100V X7R 10% 0805	1	Digikey
24	PCC101CGCT-ND	C70	CAP 100PF 50V CERM CHIP 0805 SMD	1	Digikey
25	493-1042-ND	C71	CAP 330UF 16V ELECT VR RADIAL	1	Digikey
26	445-2322-1-ND	C72, C73	CAP CER 2200PF 100V C0G 5% 0805	2	Digikey
27	PCC103BNCT-ND	C80	CAP 10000PF 50V CERM CHIP 0805	1	Digikey
28	B180DICT-ND	D1, D2, D4	DIODE SCHOTTKY 80V 1A SMA	3	Digikey
29	B1100-FDICT-ND	D3	DIODE SCHOTTKY 100V 1A SMA	1	Digikey
30	641-1166-1-ND	D5, D6, D13, D14	DIODE STANDARD 2A 400V SMB	4	Digikey
31	1N4148WDICT-ND	D7, D8, D9, D10, D12, D15, D16,	DIODE SWITCH 100V 400MW	8	Digikey

		D17	SOD-123		
32	1N5819HW-FDICT-ND	D11, D18	DIODE SCHOTTKY 40V 1A SOD123	2	Digikey
33	1N4148WTPMSCT-ND	D19, D20, D21, D22	DIODE SWITCH 100V 150MA SOD123	4	Digikey
34	RS1DB-FDICT-ND	D23	DIODE FAST REC 200V 1A SMB	1	Digikey
35	277-1271-ND	J1, J5	CONN TERM BLOCK 2POS 9.52MM PCB	2	Digikey
36	A26453-ND	J2	CONN RECEPT 6POS .100 VERT DUAL	1	Digikey
37	277-1272-ND	J3	CONN TERM BLOCK 3POS 9.52MM PCB	1	Digikey
38	A26454-ND	J4	CONN RECEPT 8POS .100 VERT DUAL	1	Digikey
39	A32248-ND	J6	CONN JACK BNC R/A 50 OHM PCB TIN	1	Digikey
40	CP-1418-ND	J7, J9	CONN RCA JACK R/A BLACK PCB	2	Digikey
41	N/A	J8	TERMINAL BLOCK 7.50MM VERT 2POS	1	Digikey
42	A26453-ND	J10	CONN RECEPT 6POS .100 VERT DUAL	1	Digikey
43	513-1051-1-ND	L1, L2, L3	INDUCTOR SHIELD PWR 470UH SMD	3	Digikey
44	7G31A-220M-R	L4, L5	Class D Inductor,22uH	2	Inductors, Inc
45	160-1143-ND	NORMAL1	LED 3MM GREEN TRANSPARENT	1	Digikey
46	N/A	P1	Power MOSFET Photovoltaic Relay	1	IR
47	160-1140-ND	PROTECTION1	LED 3MM HI-EFF RED TRANSPARENT	1	Digikey
48	FZT855CT-ND	Q1, Q3	TRANS NPN 150V 4000MA SOT-223	2	Digikey
49	MMBTA92DICT-ND	Q2	TRANSISTOR PNP -300V SOT-23	1	Digikey
50	MMBT5401DICT-ND	Q7, Q10, Q13	TRANS 150V 350MW PNP SMD SOT-23	3	Digikey
51	MMBT5551-7DICT-ND	Q8, Q9, Q11, Q12, Q14, Q15, Q17	TRANS 160V 350MW NPN SMD SOT-23	7	Digikey
52	PZT2222ACT-ND	Q18	TRANS AMP NPN GP 40V .5A SOT-223	1	Digikey
53	PZT2907AT1GOSCT-ND	Q20	TRANS SS SW PNP 600MA 60V SOT223	1	Digikey
54	PT10XCT-ND	R1, R4, R9, R14, R30	RES 10 OHM 1W 5% 2512 SMD	5	Digikey
55	P10KACT-ND	R2, R3, R5, R7, R84, R92, R99	RES 10K OHM 1/8W 5% 0805 SMD	7	Digikey
56	P20KACT-ND	R6, R142	RES 20K OHM 1/8W 5% 0805 SMD	2	Digikey
57	P47ACT-ND	R56, R79, R82, R88, R101, R107, R133, R134, R135	RES 47 OHM 1/8W 5% 0805 SMD	9	Digikey
58	RHM8.66KCRCT-ND	R10	RES 8.66K OHM 1/8W 1% 0805 SMD	1	Digikey
59	P18.7KCCT-ND	R11, R17, R32	RES 18.7K OHM 1/8W 1% 0805 SMD	3	Digikey
60	P1.00KCCT-ND	R13	RES 1.00K OHM 1/8W 1% 0805 SMD	1	Digikey
61	P4.7KCCT-ND	R15, R31	RES 4.70K OHM 1/8W 1% 0805 SMD	2	Digikey
62	P20.5KCCT-ND	R16, R19, R37	RES 20.5K OHM 1/8W 1% 0805 SMD	3	Digikey
63	P1.00KCCT-ND	R18, R36	RES 1.00K OHM 1/8W 1% 0805 SMD	2	Digikey
64	P100KACT-ND	R20, R21, R22, R47, R53, R60, R61, R87, R91, R108, R109, R112, R116, R117, R118, R119, R132, R136	RES 100K OHM 1/8W 5% 0805 SMD	15	Digikey

65	PPC100KW-3JCT-ND	R38, R62	RES 100K OHM METAL FILM 3W 5%	2	Digikey
66	P1.0KECT-ND	R39, R63	RES 1.0K OHM 1/4W 5% 1206 SMD	2	Digikey
67	P3.3KZCT-ND	R40, R64	RES 3.3K OHM 1/10W .1% 0805 SMD	2	Digikey
68	P22KACT-ND	R41, R55, R57, R65, R67, R73	RES 22K OHM 1/8W 5% 0805 SMD	6	Digikey
69	P0.0ACT-ND	R42, R66	RES 0.0 OHM 1/8W 5% 0805 SMD	2	Digikey
70	PT2.2KXCT-ND	R43, R68	RES 2.2K OHM 1W 5% 2512 SMD	2	Digikey
71	PT10XCT-ND	R45, R70	RES 10 OHM 1W 5% 2512 SMD	2	Digikey
72	311-470ARCT-ND	R46, R71	RES 470 OHM 1/8W 5% 0805 SMD	2	Digikey
73	P4.7ACT-ND	R48, R54, R72, R78	RESISTOR 4.7 OHM 1/8W 5% 0805	4	Digikey
74	3361P-102GCT-ND	R49, R74	TRIMPOT 1K OHM 6MM SQ SMD	2	Digikey
75	P100ECT-ND	R50, R75, R80, R90, R94	RES 100 OHM 1/4W 5% 1206 SMD	5	Digikey
76	P1.0KACT-ND	R51, R52, R76, R77, R104, R106, R121, R138	RES 1.0K OHM 1/8W 5% 0805 SMD	8	Digikey
77	P200KACT-ND	R58, R59	RES 200K OHM 1/8W 5% 0805 SMD	2	Digikey
78	P33KACT-ND	R81	RES 33K OHM 1/8W 5% 0805 SMD	1	Digikey
79	P47KACT-ND	R83, R86, R93, R95, R96, R105, R111, R123, R129, R139, R140	RES 47K OHM 1/8W 5% 0805 SMD	11	Digikey
80	P68KACT-ND	R85, R97	RES 68K OHM 1/8W 5% 0805 SMD	2	Digikey
81	P4.7KACT-ND	R89	RES 4.7K OHM 1/8W 5% 0805 SMD	1	Digikey
82	P100ACT-ND	R98, R114, R131	RES 100 OHM 1/8W 5% 0805 SMD	3	Digikey
83	3362H-502LF-ND	R100	POT 5.0K OHM 1/4" SQ CERM SL ST	1	Digikey
84	P330ACT-ND	R102	RES 330 OHM 1/8W 5% 0805 SMD	1	Digikey
85	P82KACT-ND	R103	RES 82K OHM 1/8W 5% 0805 SMD	1	Digikey
86	P5.76KFCT-ND	R110, R113, R120, R124, R126, R127	RES 5.76K OHM 1/4W 1% 1206 SMD	6	Digikey
87	P10ECT-ND	R115	RES 10 OHM 1/4W 5% 1206 SMD	1	Digikey
88	P0.0ECT-ND	R122, R128	RES ZERO OHM 1/4W 5% 1206 SMD	2	Digikey
89	P3G7103-ND	R130	POT 10K OHM 9MM VERT MET BUSHING	1	Digikey
90	RMCF1/100RCT-ND	R141, R148, R151	RES 0.0 OHM 1/8W 0805 SMD	3	Digikey
91	P47.5KCCT-ND	R144, R145, R146	RES 47.5K OHM 1/8W 1% 0805 SMD	3	Digikey
92	PT10XCT-ND	R147, R149, R150	RES 10 OHM 1W 5% 2512 SMD	3	Digikey
93	open	R152	0ohm for 1kw	1	Digikey
94	P0.0ACT-ND	R153	RES 1.0K OHM 1/8W 5% 0805 SMD	1	Digikey
95	311-1.0KARCT-ND	R154, R155	RES 1.0K OHM 1/8W 5% 0805 SMD	2	Digikey
96	open	R156, R157	Bypass vol ctrl	2	
97	EG1944-ND	S1, S2	SWITCH SLIDE DP3T .2A L=6MM	2	Digikey
98	P8010S-ND	S3	6MM LIGHT TOUCH SW H=5	1	Digikey
99	LM5574MT-ND	U2, U3, U4	IC REG BUCK 75V 0.5A 16-TSSOP	3	Digikey
100	IRF7380	U5, U9	80V DUAL N MOSFET SO8	2	IR

101	AD825ARZ-ND	U6, U11	IC AMP JFET HS GEN-PURP 8-SOIC	2	Digikey
102	XN0121500LCT-ND	U7, U10	TRANS ARRAY NPN/NPN W/RES MINI5P	2	Digikey
103	296-1089-1-ND	U8, U12	IC SINGLE INVERTER GATE SOT23-5	2	Digikey
104	296-11643-1-ND	U13	DUAL 4-BIT BINARY COUNTERS	1	Digikey
105	300-8001-1-ND	U14	OSCILLATOR 1.5440 MHZ SMT	1	Digikey
106	296-1194-1-ND	U_1	IC HEX SCHMITT-TRIG INV 14-SOIC	1	Digikey
107	3310IR02	U_2	Stand-alone Controller	1	Tachyonix
108	598-1599-ND	U_3	Amplifiers - Audio Stereo Digital Volume Control	1	Digikey/Mouser
109	BZT52C15-7DICT-ND	Z1	DIODE ZENER 15V 500MW SOD-123	1	Digikey
110	MMSZ5263BT1OSCT-ND	Z2, Z3	DIODE ZENER 500MW 56V SOD123	2	Digikey
111	BZT52C5V1-7DICT-ND	Z4	DIODE ZENER 5.1V 500MW SOD-123	1	Digikey
112	BZT52C15-FDICT-ND	Z5, Z6	DIODE ZENER 500MW 15V SOD123	2	Digikey
113	BZT52C18-FDICT-ND	Z7	DIODE ZENER 500MW 18V SOD123	1	Digikey
114	BZT52C36-7DICT-ND	Z8	DIODE ZENER 36V 500MW SOD-123	1	Digikey
115	MMSZ5268BT1GOSCT-ND	Z9	DIODE ZENER 82V 500MW SOD-123	1	Digikey
116	BZT52C5V6-FDICT-ND	Z10, Z12	DIODE ZENER 5.6V 500MW SOD123	2	Digikey

Table 2 IRAUDAMP6 Daughter board's Materials

No	P/N	Designator	Description	Quantity	Vendor
1	445-2276-1-ND	C1, C2, C3, C4	CAP CER 47000PF 100V X7R 10%0805	4	Digikey
2	PCC470CGCT-ND	C5, C6	CAP 47PF 50V CERM CHIP 0805 SMD	2	Digikey
3	587-1329-1-ND	C9, C10, C13, C14	CAP CER 2.2UF 25V X7R 1206	4	Digikey
4	399-3706-1-ND	C11, C12	CAPACITOR TANT 10UF 16V 10% SMD	2	Digikey
5	445-1607-1-ND	C15, C16	CAP CER 22UF 25V X7R 20% 1812	2	Digikey
6	445-2296-1-ND	C17, C18	CAP CER .22UF 250V X7R 10% 1210	2	Digikey
7	445-2300-1-ND	C19, C20, C21, C22, C23, C24, C25, C26	CAP CER .10UF 630V X7R 10% 1812	8	Digikey
8	B130LAW-FDICT-ND	D2, D3	DIODE SCHOTTKY 1A 30V SOD123	2	Digikey
9	1N4148WTPMSCT-ND	D4, D5	DIODE SWITCH 100V 150MA SOD123	2	Digikey
10	ES1D-FDICT-ND	D6, D7	DIODE ULTRA FAST 1A 200V SMA	2	Digikey
11	BAV21W-FDICT-ND	D8, D9	DIODE SWITCH 200V 250MW SOD123	2	Digikey
12	2011-03-ND	J1, J2	CONN HEADER .100 DUAL STR 6POS	2	Digikey
13	2011-04-ND	J3	CONN HEADER .100 DUAL STR 8POS	1	Digikey
14	MMBT5551-7DICT-ND	Q1, Q4	TRANS 160V 350MW NPN SMD SOT-23	2	Digikey
15	MMBT5401DICT-ND	Q2, Q3	TRANS 150V 350MW PNP SMD SOT-23	2	Digikey
16	IRF6785M	Q5, Q6, Q7, Q8	DirectFET M-Case	4	IR

17	P100KACT-ND	R1, R3, R5, R7, R9, R11	RES 100K OHM 1/8W 5% 0805 SMD	6	Digikey
18	P10KACT-ND	R2, R8, R30, R31	RES 10K OHM 1/8W 5% 0805 SMD	4	Digikey
19	P1.0KACT-ND	R4, R6	RES 1.0K OHM 1/8W 5% 0805 SMD	2	Digikey
20	RHM9.1KARCT-ND	R12, R13	RES 9.1K OHM 1/8W 5% 0805 SMD	2	Digikey
21	P100ACT-ND	R14, R15	RES 100 OHM 1/8W 5% 0805 SMD	2	Digikey
22	RHM18KERCT-ND	R16, R17	RES 18K OHM 1/4W 5% 1206 SMD	2	Digikey
23	RHM1.2KARCT-ND	R18, R20	RES 1.2K OHM 1/8W 5% 0805 SMD	2	Digikey
24	P8.2KACT-ND	R19, R21	RES 8.2K OHM 1/8W 5% 0805 SMD	2	Digikey
25	P3.3KACT-ND	R22, R23	RES 3.3K OHM 1/8W 5% 0805 SMD	2	Digikey
26	P4.7ACT-ND	R24, R25	RESISTOR 4.7 OHM 1/8W 5% 0805	2	Digikey
27	P10ACT-ND	R26, R27, R36, R37, R38, R39	RES 10 OHM 1/8W 5% 0805 SMD	6	Digikey
28	P33KACT-ND	R28, R29	RES 33K OHM 1/8W 5% 0805 SMD	2	Digikey
29	RHM2.2KARCT-ND	R32, R33	RES 2.2K OHM 1/8W 5% 0805 SMD	2	Digikey
30	RHM7.5KARCT-ND	R34, R35	RES 7.5K OHM 1/8W 5% 0805 SMD	2	Digikey
31	P1.0PCT-ND	R40, R41	RES 1.0 OHM 1/4W 5% 1206 SMD	2	Digikey
32	P0.0ACT-ND	R42, R43	RES 0.0 OHM 1/8W 5% 0805 SMD	2	Digikey
33	594-2381-675-20907	Rp1, Rp2	Thermistors PTC Temp Prot. 100 C	2	Mouser
34	IRS20957S	U1, U2	IC GATE DRIVER	2	IR

Table 3 IRAUDAMP6 Mechanical Bill of Materials

No	P/N	Description	Quantity	Vendor
1	BER229-ND	THERMAL PAD 8"X16" .080" GP1500		Digikey
2	DCC5837U-18B	Heat Sink 57.9 x 36.8 x 17.8	1	Alpha Novatech Inc.
3	S001YZ1H	PIP 3.175*8.5[TH]	4	Alpha Novatech Inc.
4	S001YJ1D	Spring	4	Alpha Novatech Inc.

IRAUDAMP6 PCB Specifications

PCB:

1. Two Layers SMT PCB with through holes
2. 1/16 thickness
3. 2/0 OZ Cu
4. FR4 material
5. 10 mil lines and spaces
6. Solder Mask to be Green enamel EMP110 DBG (CARAPACE) or Enthone Endplate DSR-3241or equivalent.
7. Silk Screen to be white epoxy non conductive per IPC–RB 276 Standard.
8. All exposed copper must finished with TIN-LEAD Sn 60 or 63 for 100u inches thick.
9. Tolerance of PCB size shall be 0.010 –0.000 inches
10. Tolerance of all Holes is -.000 + 0.003”
11. PCB acceptance criteria as defined for class II PCB’S standards.

Gerber Files Apertures Description:

All Gerber files stored in the attached CD-ROM were generated from Protel Altium Designer Altium Designer 6. Each file name extension means the following:

1. .gtl Top copper, top side
2. .gbl Bottom copper, bottom side
3. .gto Top silk screen
4. .gbo Bottom silk screen
5. .gts Top Solder Mask
6. .gbs Bottom Solder Mask
7. .gko Keep Out,
8. .gm1 Mechanical1
9. .gd1 Drill Drawing
10. .gg1 Drill locations
11. .txt CNC data
12. .apr Apertures data

Additional files for assembly that may not be related with Gerber files:

13. .pcb PCB file
14. .bom Bill of materials
15. .cpl Components locations
16. .sch Schematic
17. .csv Pick and Place Components
18. .net Net List
19. .bak Back up files
20. .lib PCB libraries

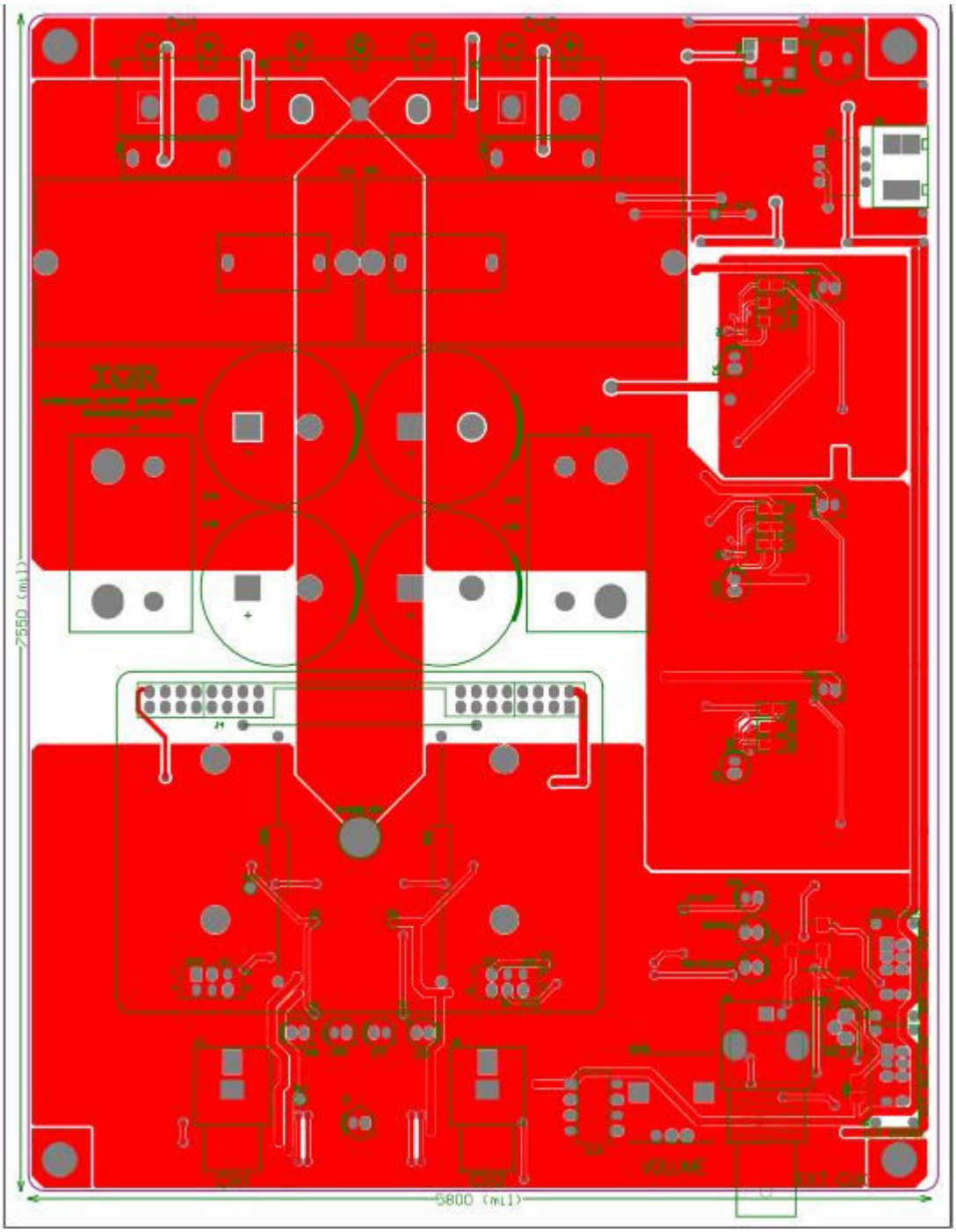


Fig 25 IRAUDAMP6 Mother board PCB Top Overlay (Top View)

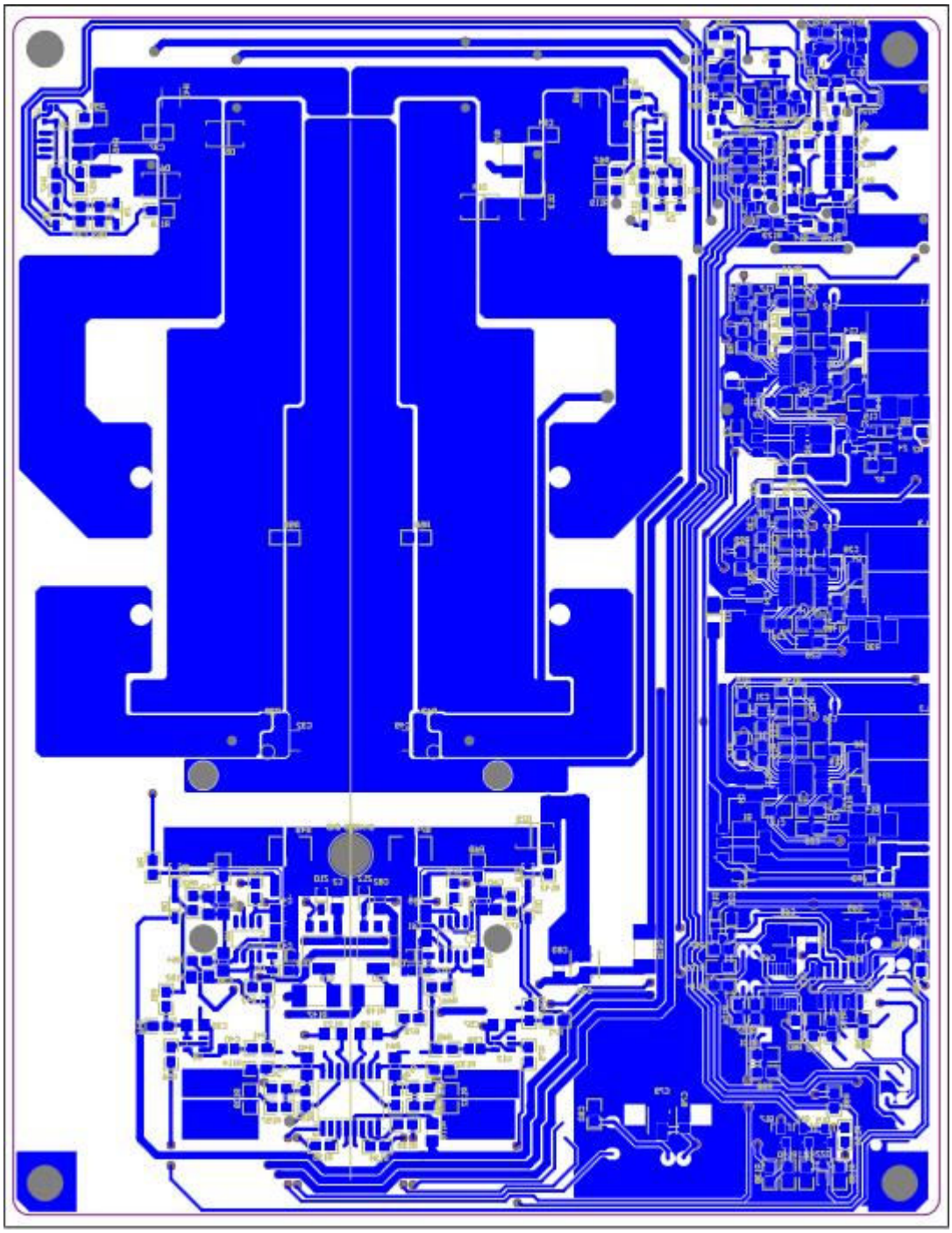


Fig 26 IRAUDAMP6 Mother board PCB Bottom Layer (Top View)

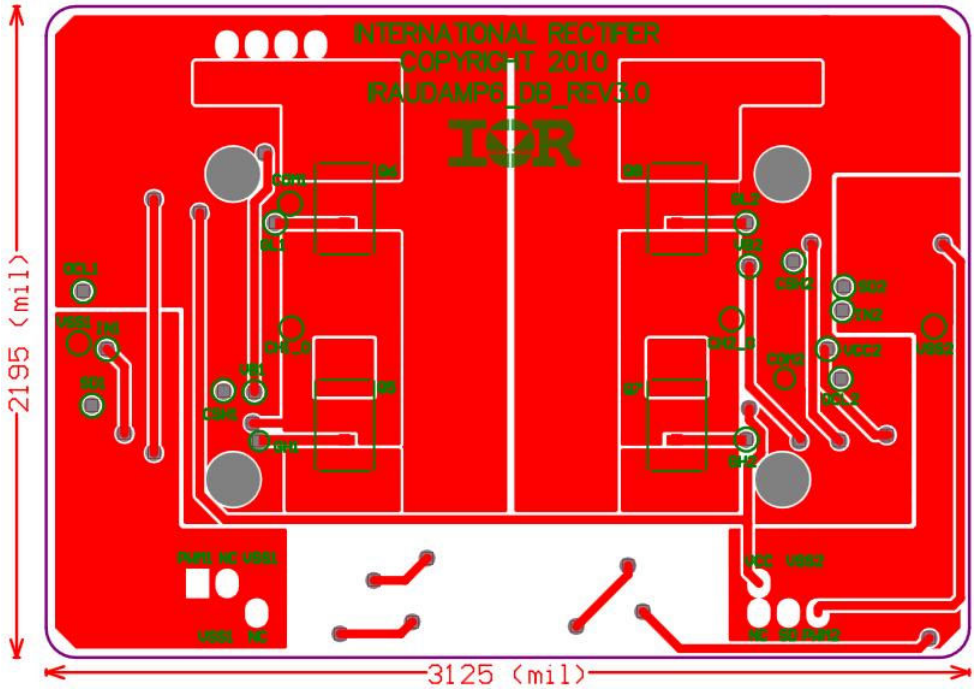


Fig 27 IRAUDAMP6 Daughter board PCB Top Overlay (Top View)

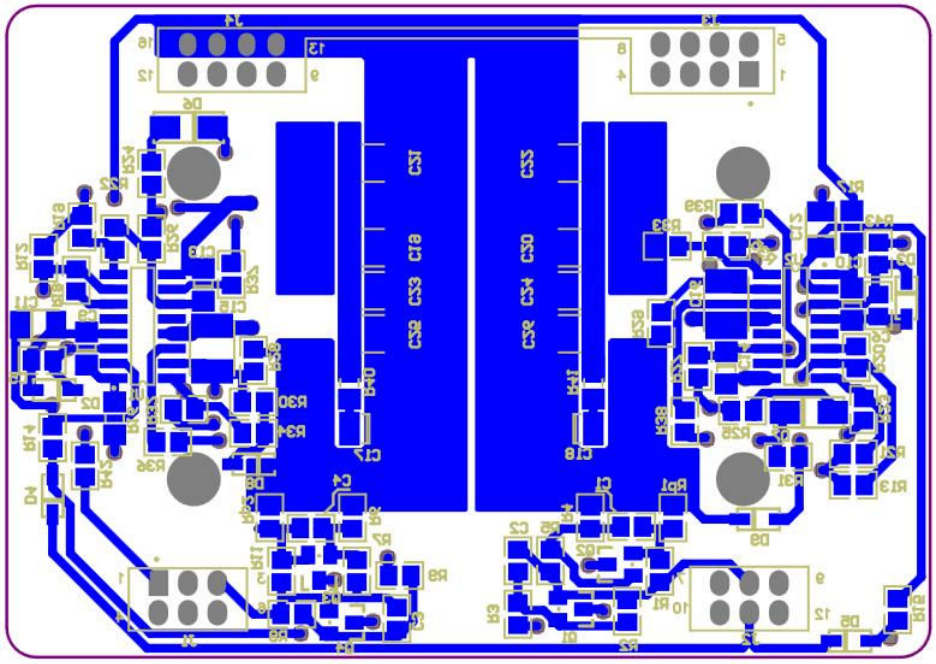


Fig 28 IRAUDAMP6 Daughter board PCB Bottom Layer (Top View)

Revision changes descriptions

Revision	Changes description	Date
Rev 1.0	Released	May, 30 2010

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