–28 V, –200 mA, Low Noise, Linear Regulator

Data Sheet

ADP7182

FEATURES

- Low noise: 18 µV rms
- Power supply rejection ratio (PSRR): 66 dB at 10 kHz at V_{OUT} = –3 V
- Positive or negative enable logic
- Stable with small 2.2 µF ceramic output capacitor
- Input voltage range: –2.7 V to –28 V
- Maximum output current: –200 mA
- Low dropout voltage: –185 mV at –200 mA load
- Initial accuracy: ±1%
- Accuracy over line, load, and temperature
  - +2% maximum/–3% minimum
- Low quiescent current, I_{GND} = –650 µA with –200 mA load
- Low shutdown current: –2 µA
- Adjustable output from –1.22 V to $-V_{IN} + V_{DO}$
- Current-limit and thermal overload protection
- 6- and 8-lead LFCSP and 5-lead TSOT
- Supported by ADIsimPower tool

APPLICATIONS

- Regulation to noise sensitive applications
  - Analog-to-digital converter (ADC) and digital-to-analog converter (DAC) circuits, precision amplifiers
- Communications and infrastructure
- Medical and healthcare
- Industrial and instrumentation

TYPICAL APPLICATION CIRCUITS

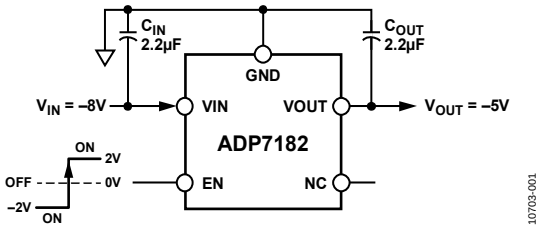

Figure 1. ADP7182 with Fixed Output Voltage, V_{OUT} = –5 V

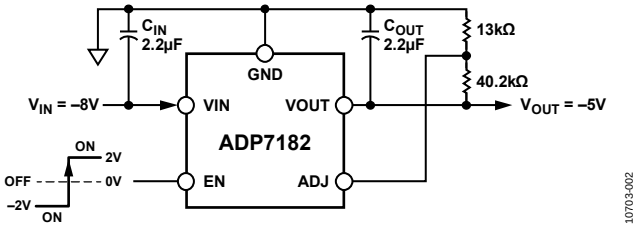

Figure 2. ADP7182 with Adjustable Output Voltage, V_{OUT} = –5 V

GENERAL DESCRIPTION

The ADP7182 is a CMOS, low dropout (LDO) linear regulator that operates from –2.7 V to –28 V and provides up to –200 mA of output current. This high input voltage LDO is ideal for regulation of high performance analog and mixed signal circuits operating from –27 V down to –1.2 V rails. Using an advanced proprietary architecture, it provides high power supply rejection and low noise, and achieves excellent line and load transient response with a small 2.2 µF ceramic output capacitor.

The ADP7182 is available in fixed output voltage and an adjustable version that allows the output voltage to range from –1.22 V to $-V_{IN} + V_{DO}$ via an external feedback divider.

The following fixed output voltages are available from stock: –5 V (3 mm × 3 mm LFCSP), –1.8 V, –2.5 V, –3 V, –5 V (TSOT), –1.2 V, –1.5 V, –2.5 V, –5 V (2 mm × 2 mm LFCSP). Additional voltages are available by special order.

The ADP7182 regulator output noise is 18 µV rms independent of the output voltage. The enable logic is capable of interfacing with positive or negative logic levels for maximum flexibility.

The ADP7182 is available in 5-lead TSOT, 6- and 8-lead LFCSP packages for a small, low profile footprint.

Rev. J
Document Feedback

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ADP7182* PRODUCT PAGE QUICK LINKS

Last Content Update: 03/28/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADP7182 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1329: Noise Reduction Network for Adjustable Low Dropout Regulators
- AN-1359: Low Noise, Dual-Supply Solution Using the ADP5070 for the Precision AD5761R Bipolar DAC in Single-Supply Systems

Data Sheet

- ADP7182: –28 V, –200 mA, Low Noise, Linear Regulator Data Sheet

User Guides

- UG-412: Evaluating the ADP7182 Low Noise, Linear Regulator

TOOLS AND SIMULATIONS

- ADI Linear Regulator Design Tool and Parametric Search
- ADIsimPower™ Voltage Regulator Design Tool

REFERENCE DESIGNS

- CN0280
- CN0292

REFERENCE MATERIALS

Press

- Integrated Analog Front-end Simplifies Sensor Interfaces

DESIGN RESOURCES

- ADP7182 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADP7182 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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4/2013—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = (V_{OUT} − 0.5 V) or −2.7 V (whichever is more negative), EN = V_{IN}, I_{OUT} = −10 mA, C_{IN} = C_{OUT} = 2.2 µF, T_J = −40°C to +125°C for minimum/maximum specifications, T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}		−2.7		−28	V
OPERATING SUPPLY CURRENT	I_{GND}	I_{OUT} = 0 µA		−33	−53	µA
		I_{OUT} = −10 mA		−100	−150	µA
		I_{OUT} = −200 mA		−650	−850	µA
SHUTDOWN CURRENT	I_{GND-SD}	EN = GND		−2		µA
		EN = GND, V_{IN} = −2.7 V to −28 V			−8	µA
OUTPUT VOLTAGE ACCURACY						
Fixed Output Voltage Accuracy	V_{OUT}	I_{OUT} = −10 mA, T_A = 25°C	−1		+1	%
		−1 mA < I_{OUT} < −200 mA, V_{IN} = (V_{OUT} − 0.5 V) to −28 V	−3		+2	%
Adjustable Output Voltage Accuracy	V_{ADJ}	I_{OUT} = −10 mA	−1.208	−1.22	−1.232	V
		−1 mA < I_{OUT} < −200 mA, V_{IN} = (V_{OUT} − 0.5 V) to −28 V	−1.184		−1.244	V
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} − 0.5 V) to −28 V	−0.01		+0.01	%/V
LOAD REGULATION[1]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = −1 mA to −200 mA		0.001	0.006	%/mA
ADJ INPUT BIAS CURRENT	ADJ_{I-BIAS}	−1 mA < I_{OUT} < −200 mA, V_{IN} = (V_{OUT} − 0.5 V) to −28 V		10		nA
DROPOUT VOLTAGE[2]	V_{DO}	I_{OUT} = −10 mA		−25	−70	mV
		I_{OUT} = −50 mA		−46	−90	mV
		I_{OUT} = −200 mA		−185	−360	mV
START-UP TIME[3]	$t_{START-UP}$	V_{OUT} = −5 V		550		µs
		V_{OUT} = −2.8 V		375		µs
CURRENT-LIMIT THRESHOLD[4]	I_{LIMIT}		−230	−350	−500	mA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
EN THRESHOLD						
Positive Rise	$V_{EN-POS-RISE}$	V_{OUT} = off to on (positive)			1.2	V
Negative Rise	$V_{EN-NEG-RISE}$	V_{OUT} = off to on (negative)	−2.0			V
Positive Fall	$V_{EN-POS-FALL}$	V_{OUT} = on to off (positive)	0.3			V
Negative Fall	$V_{EN-NEG-FALL}$	V_{OUT} = on to off (negative)			−0.55	V
INPUT VOLTAGE LOCKOUT						
Start Threshold	V_{START}		−2.695	−2.49		V
Shutdown Threshold	$V_{SHUTDOWN}$			−2.34	−2.1	V
Hysteresis				150		mV
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, V_{OUT} = −1.5 V, V_{OUT} = −3 V, and V_{OUT} = −5 V		18		µV rms
		10 Hz to 100 kHz, V_{OUT} = −5 V, adjustable mode, C_{NR} = open, R_{NR} = open, R_{FB1} = 147 kΩ, R_{FB2} = 13 kΩ		150		µV rms
		10 Hz to 100 kHz, V_{OUT} = −5 V, adjustable mode, C_{NR} = 100 nF, R_{NR} = 13 kΩ, R_{FB1} = 147 kΩ, R_{FB2} = 13 kΩ		33		µV rms

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY REJECTION RATIO	PSRR	1 MHz, V_{IN} = −4.3 V, V_{OUT} = −3 V		45		dB
		1 MHz, V_{IN} = −6 V, V_{OUT} = −5 V		32		dB
		100 kHz, V_{IN} = −4.3 V, V_{OUT} = −3 V		45		dB
		100 kHz, V_{IN} = −6 V, V_{OUT} = −5 V		45		dB
		10 kHz, V_{IN} = −4.3 V, V_{OUT} = −3 V		66		dB
		10 kHz, V_{IN} = −6 V, V_{OUT} = −5 V		66		dB
		1 MHz, V_{IN} = −16 V, V_{OUT} = −15 V, adjustable mode, C_{NR} = 100 nF, R_{NR} = 13 kΩ, R_{FB1} = 13 kΩ, R_{FB2} = 147 kΩ		45		dB
		100 kHz, V_{IN} = −16 V, V_{OUT} = −15 V, adjustable mode, C_{NR} = 100 nF, R_{NR} = 13 kΩ, R_{FB1} = 13 kΩ, R_{FB2} = 147 kΩ		45		dB
		10 kHz, V_{IN} = −16 V, V_{OUT} = −15 V, adjustable mode, C_{NR} = 100 nF, R_{NR} = 13 kΩ, R_{FB1} = 13 kΩ, R_{FB2} = 147 kΩ		66		dB

[1] Based on an endpoint calculation using −1 mA and −200 mA loads. See Figure 10 for the typical load regulation performance for loads less than 1 mA.
[2] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages below −3 V.
[3] Start-up time is defined as the time between the rising edge of EN to VOUT being at 90% of the nominal value.
[4] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a −5 V output voltage is defined as the current that causes the output voltage to drop to 90% of −5 V, or −4.5 V.

INPUT AND OUTPUT CAPACITANCE, RECOMMENDED SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT AND OUTPUT CAPACITANCE						
Minimum Capacitance[1]	C_{MIN}	T_A = −40°C to +125°C	1.5	2.2		µF
Capacitor Effective Series Resistance (ESR)	R_{ESR}	T_A = −40°C to +125°C	0.001		0.2	Ω

[1] The minimum input and output capacitance must be greater than 1.5 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN to GND	+0.3 V to −30 V
VOUT to GND	0.3 V to VIN
EN to GND	5 V to VIN
EN to VIN	+30 V to −0.3 V
ADJ to GND	+0.3 V to VOUT
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Operating Ambient Temperature Range	−40°C to +85°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP7182 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that junction temperature (T_J) is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated.

In applications with moderate power dissipation and low printed circuit board (PCB) thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The T_J of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}).

Maximum T_J is calculated from the T_A and P_D using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout.

In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} can vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 in. × 3 in. circuit board. See JESD51-7 and JESD51-9 for detailed information on the board construction. For additional information, see the AN-617 Application Note, *MicroCSP™ Wafer Level Chip Scale Package*.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature is calculated from the board temperature (TB) and power dissipation using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

See JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA}, θ_{JC}, and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Ψ_{JB}	Unit
8-Lead LFCSP	50.2	31.7	18.2	°C/W
6-Lead LFCSP	68.9	42.29	44.1	°C/W
5-Lead TSOT	170	Not applicable	43	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

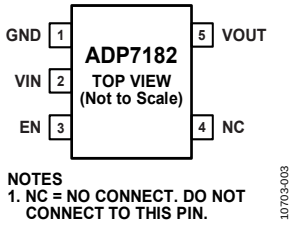


Figure 3. 5-Lead TSOT Pin Configuration, Fixed Output Voltage

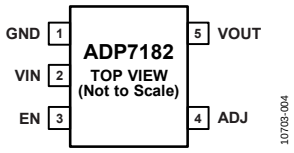
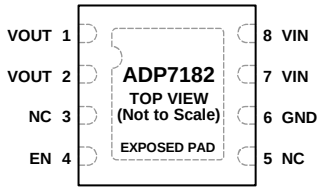


Figure 4. 5-Lead TSOT Pin Configuration, Adjustable Output Voltage

Table 5. 5-Lead TSOT Pin Function Descriptions

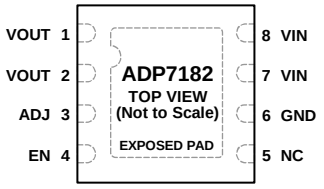
TSOT Pin No.			
Fixed Output Voltage	**Adjustable Output Voltage**	**Mnemonic**	**Description**
1	1	GND	Ground.
2	2	VIN	Regulator Input Supply. Bypass VIN to GND with a 2.2 µF or greater capacitor.
3	3	EN	Drive EN 2 V above or below ground to enable the regulator, or drive EN to ground to turn off the regulator. For automatic startup, connect EN to VIN.
4	Not applicable	NC	No Connect. Do not connect to this pin.
Not applicable	4	ADJ	Adjustable Input. An external resistor divider sets the output voltage.
5	5	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 2.2 µF or greater capacitor.



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED PAD ON THE BOTTOM OF THE LFCSP PACKAGE ENHANCES THERMAL PERFORMANCE AND IS ELECTRICALLY CONNECTED TO VIN INSIDE THE PACKAGE. THE EXPOSED PAD MUST BE CONNECTED TO THE VIN PLANE ON THE BOARD FOR PROPER OPERATION. BECAUSE THIS IS A NEGATIVE VOLTAGE REGULATOR, VIN IS THE MOST NEGATIVE POTENTIAL IN THE CIRCUIT.

10703-005

Figure 5. 8-Lead LFCSP Pin Configuration, Fixed Output Voltage



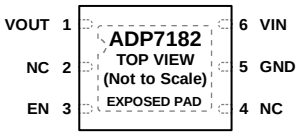
NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED PAD ON THE BOTTOM OF THE LFCSP PACKAGE ENHANCES THERMAL PERFORMANCE AND IS ELECTRICALLY CONNECTED TO VIN INSIDE THE PACKAGE. THE EXPOSED PAD MUST BE CONNECTED TO THE VIN PLANE ON THE BOARD FOR PROPER OPERATION. BECAUSE THIS IS A NEGATIVE VOLTAGE REGULATOR, VIN IS THE MOST NEGATIVE POTENTIAL IN THE CIRCUIT.

10703-006

Figure 6. 8-Lead LFCSP Pin Configuration, Adjustable Output Voltage

Table 6. 8-Lead LFCSP Pin Function Descriptions

LFCSP Pin No.			
Fixed Output Voltage	**Adjustable Output Voltage**	**Mnemonic**	**Description**
1, 2	1, 2	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 2.2 µF or greater capacitor.
Not applicable	3	ADJ	Adjustable Input. An external resistor divider sets the output voltage.
3	Not applicable	NC	No Connect. Do not connect to this pin.
4	4	EN	Drive EN 2 V above or below ground to enable the regulator, or drive EN to ground to turn off the regulator. For automatic startup, connect EN to VIN.
5	5	NC	No Connect. Do not connect to this pin.
6	6	GND	Ground.
7, 8	7, 8	VIN	Regulator Input Supply. Bypass VIN to GND with a 2.2 µF or greater capacitor.
9	9	EPAD	Exposed pad. The exposed pad on the bottom of the LFCSP package enhances thermal performance and is electrically connected to VIN inside the package. The exposed pad must be connected to the VIN plane on the board for proper operation. Because this is a negative voltage regulator, VIN is the most negative potential in the circuit.



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED PAD ON THE BOTTOM OF THE LFCSP PACKAGE ENHANCES THERMAL PERFORMANCE AND IS ELECTRICALLY CONNECTED TO VIN INSIDE THE PACKAGE. THE EXPOSED PAD MUST BE CONNECTED TO THE VIN PLANE ON THE BOARD FOR PROPER OPERATION. BECAUSE THIS IS A NEGATIVE VOLTAGE REGULATOR, VIN IS THE MOST NEGATIVE POTENTIAL IN THE CIRCUIT.

10703-107

Figure 7. 6-Lead LFCSP Pin Configuration, Fixed Output Voltage

NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED PAD ON THE BOTTOM OF THE LFCSP PACKAGE ENHANCES THERMAL PERFORMANCE AND IS ELECTRICALLY CONNECTED TO VIN INSIDE THE PACKAGE. THE EXPOSED PAD MUST BE CONNECTED TO THE VIN PLANE ON THE BOARD FOR PROPER OPERATION. BECAUSE THIS IS A NEGATIVE VOLTAGE REGULATOR, VIN IS THE MOST NEGATIVE POTENTIAL IN THE CIRCUIT.

10703-106

Figure 8. 6-Lead LFCSP Pin Configuration, Adjustable Output Voltage

Table 7. 6-Lead LFCSP Pin Function Descriptions

LFCSP Pin No.			
Fixed Output Voltage	**Adjustable Output Voltage**	**Mnemonic**	**Description**
1	1	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 2.2 µF or greater capacitor.
Not applicable	2	ADJ	Adjustable Input. An external resistor divider sets the output voltage.
3	3	EN	Drive EN 2 V above or below ground to enable the regulator, or drive EN to ground to turn off the regulator. For automatic startup, connect EN to VIN.
2, 4	4	NC	No Connect. Do not connect to this pin.
5	5	GND	Ground.
6	6	VIN	Regulator Input Supply. Bypass VIN to GND with a 2.2 µF or greater capacitor.
7	7	EPAD	Exposed pad. The exposed pad on the bottom of the LFCSP package enhances thermal performance and is electrically connected to VIN inside the package. The exposed pad must be connected to the VIN plane on the board for proper operation. Because this is a negative voltage regulator, VIN is the most negative potential in the circuit.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = −3.5 V, V_{OUT} = −3 V, I_{OUT} = −10 mA, C_{IN} = C_{OUT} = 2.2 µF, T_A = 25°C, unless otherwise noted.

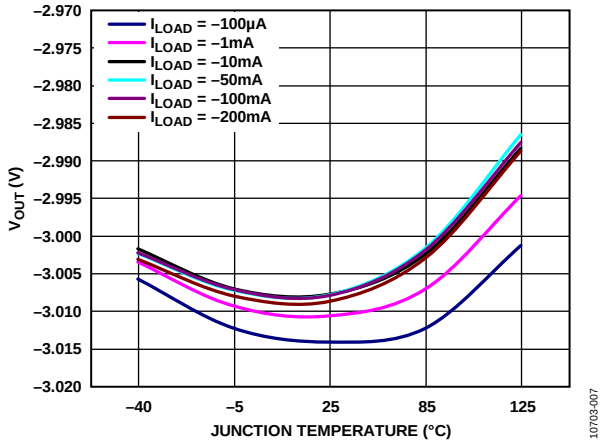


Figure 9. Output Voltage (V_{OUT}) vs. Junction Temperature (T_J)

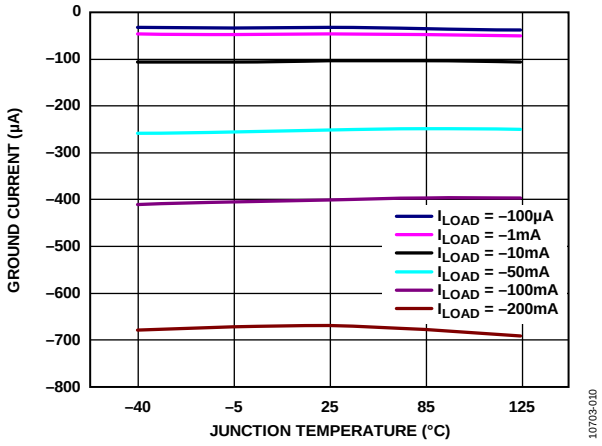


Figure 12. Ground Current vs. Junction Temperature (T_J)

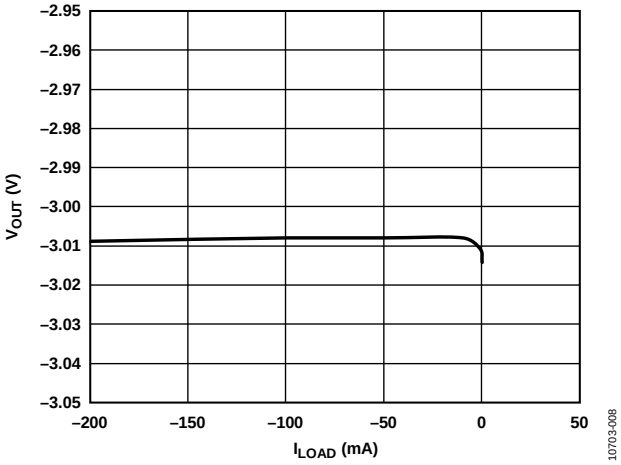


Figure 10. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD})

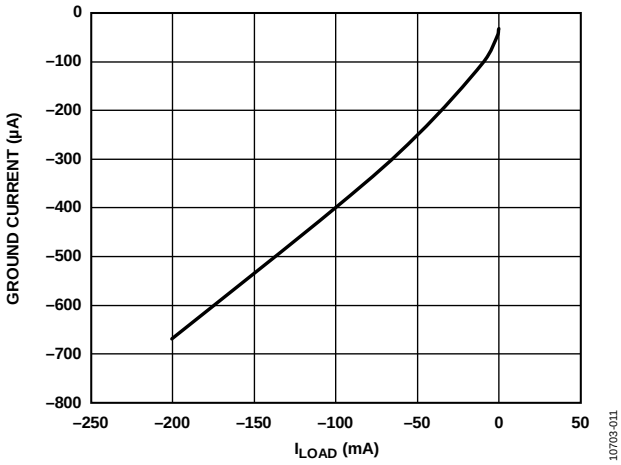


Figure 13. Ground Current vs. Load Current (I_{LOAD})

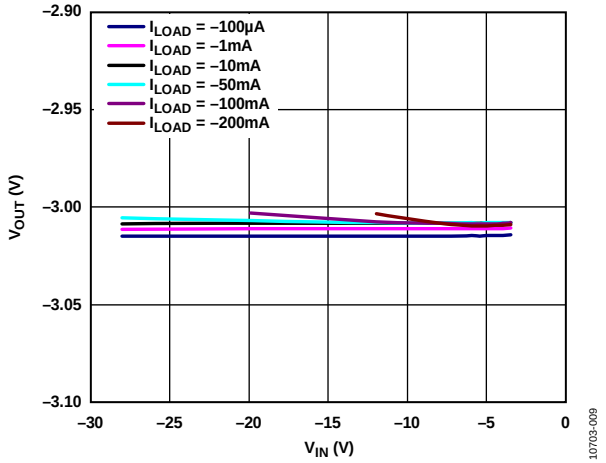


Figure 11. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN})

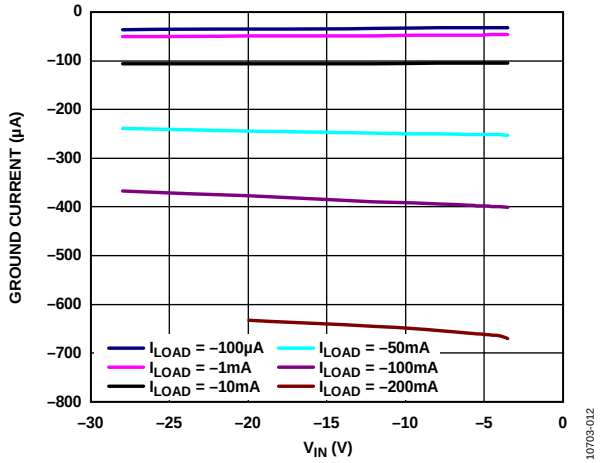


Figure 14. Ground Current vs. Input Voltage (V_{IN})

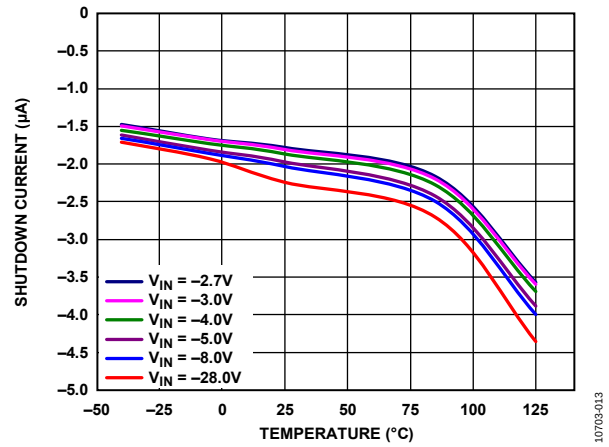


Figure 15. Shutdown Current vs. Temperature at Various Input Voltages

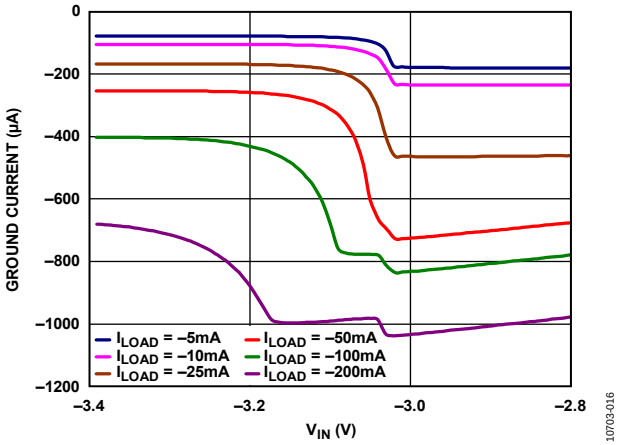


Figure 18. Ground Current vs. Input Voltage (V_{IN}) in Dropout

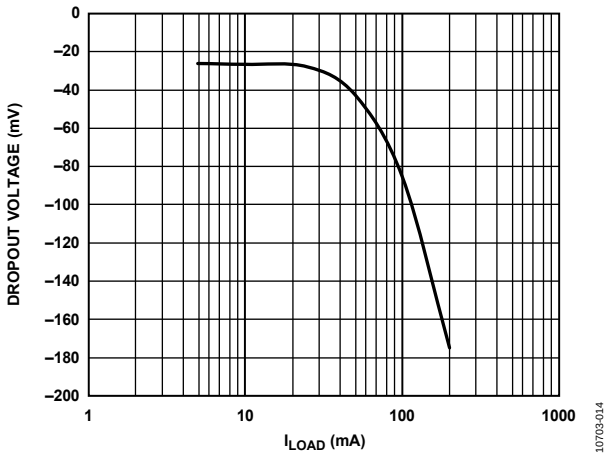


Figure 16. Dropout Voltage vs. Load Current (I_{LOAD})

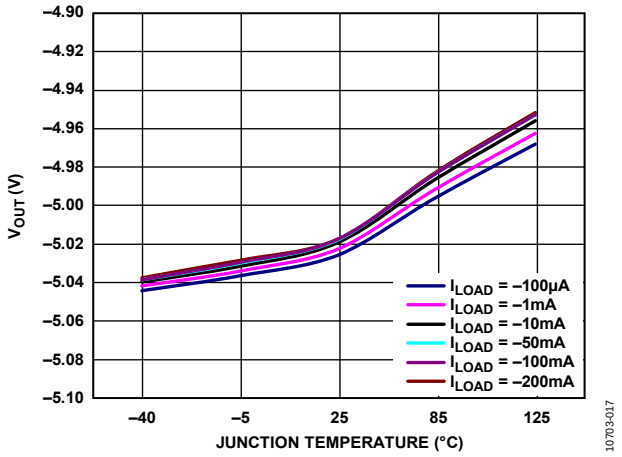


Figure 19. Output Voltage (V_{OUT}) vs. Junction Temperature (T_J), V_{OUT} = –5 V

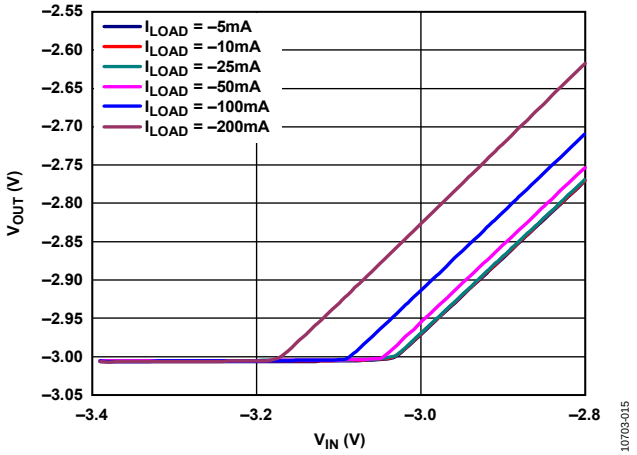


Figure 17. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) in Dropout

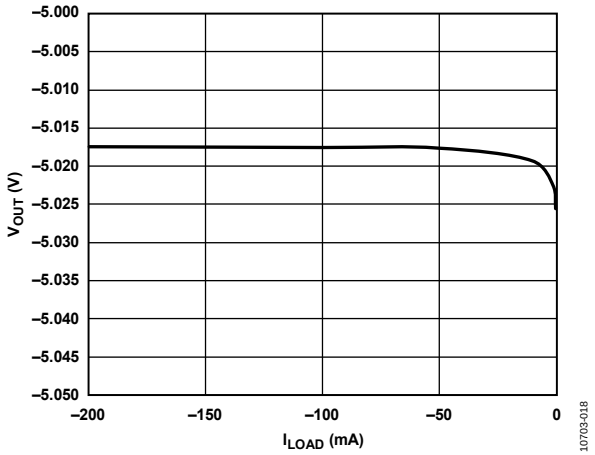


Figure 20. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), V_{OUT} = –5 V

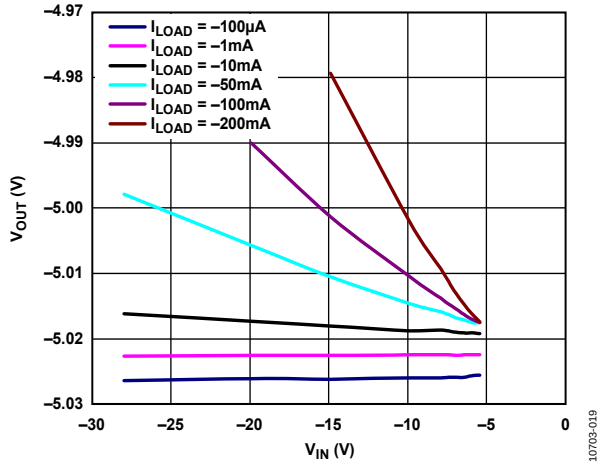


Figure 21. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), V_{OUT} = –5 V

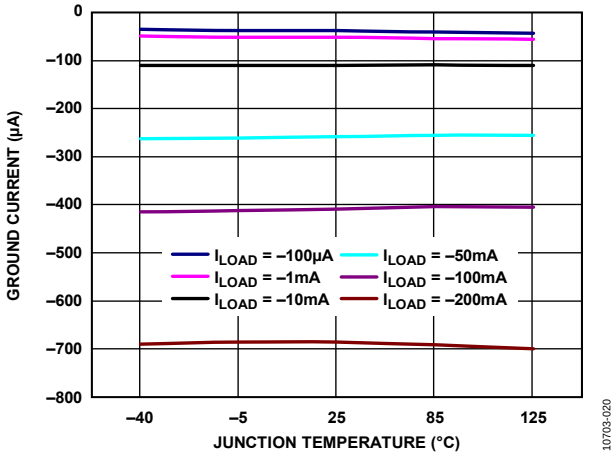


Figure 22. Ground Current vs. Junction Temperature (T_J), V_{OUT} = –5 V

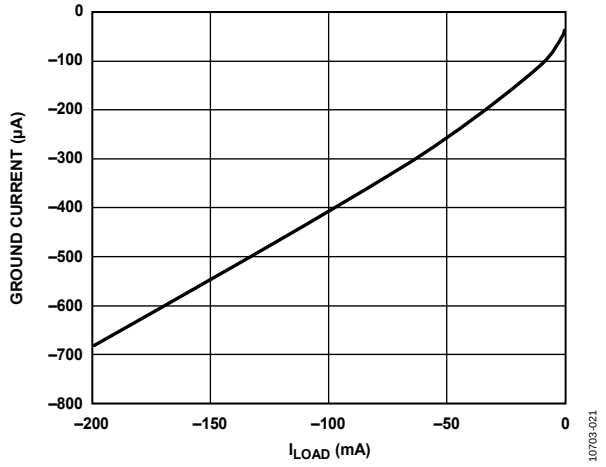


Figure 23. Ground Current vs. Load Current (I_{LOAD}), V_{OUT} = –5 V

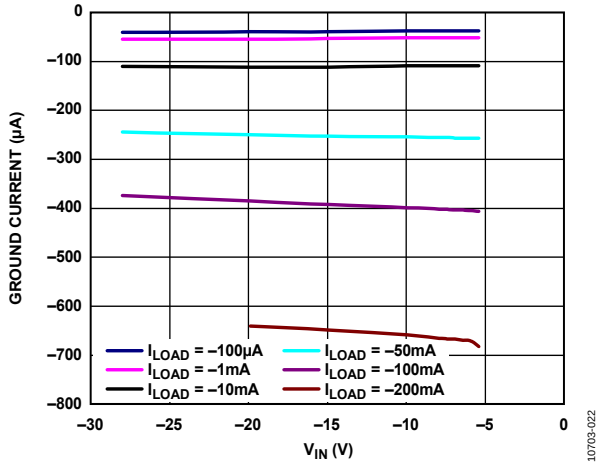


Figure 24. Ground Current vs. Input Voltage (V_{IN}), V_{OUT} = –5 V

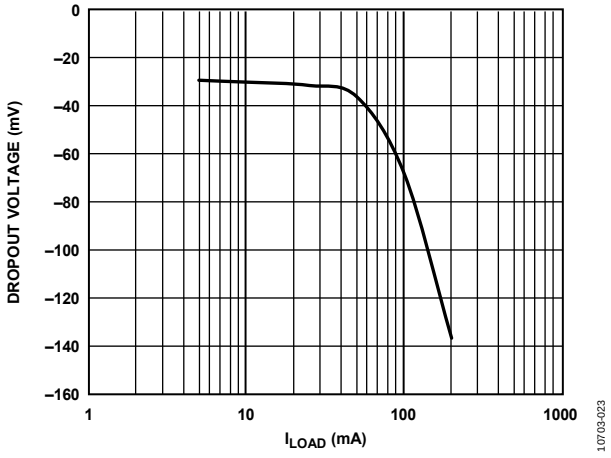


Figure 25. Dropout Voltage vs. Load Current (I_{LOAD}), V_{OUT} = –5 V

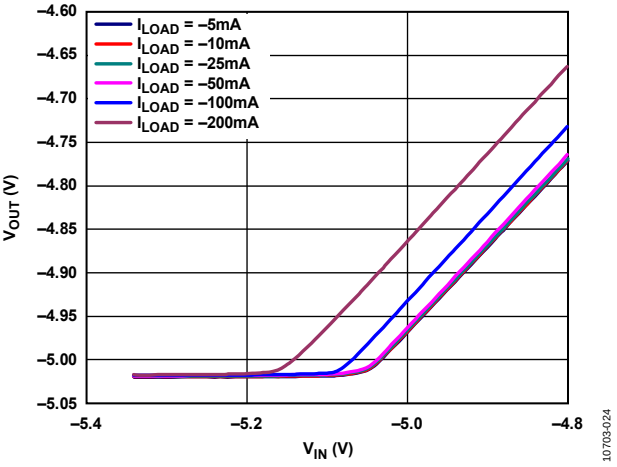


Figure 26. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) in Dropout, V_{OUT} = –5 V

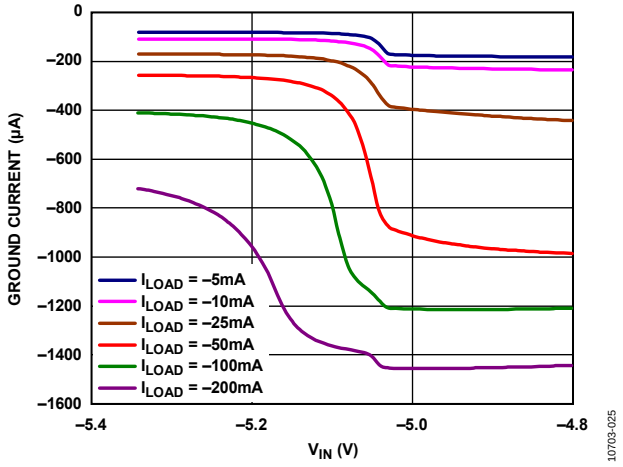


Figure 27. Ground Current vs. Input Voltage (V_{IN}) in Dropout, V_{OUT} = −5 V

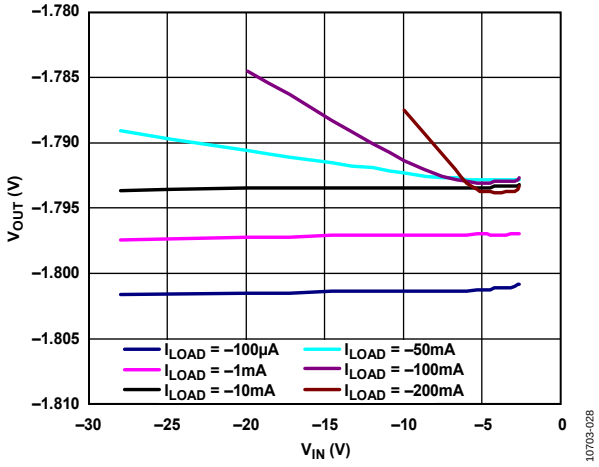


Figure 30. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), V_{OUT} = −1.8 V

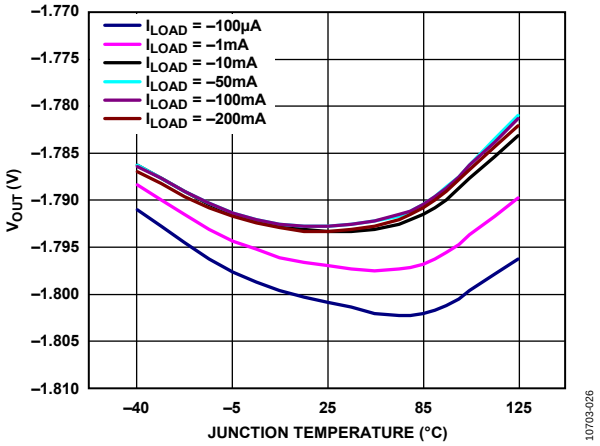


Figure 28. Output Voltage (V_{OUT}) vs. Junction Temperature (T_J), V_{OUT} = −1.8 V

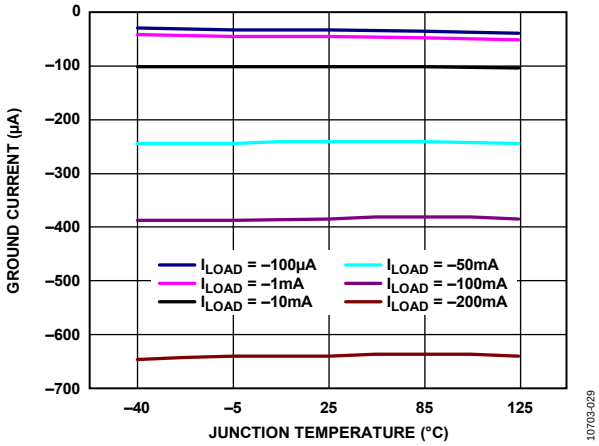


Figure 31. Ground Current vs. Junction Temperature (T_J), V_{OUT} = −1.8 V

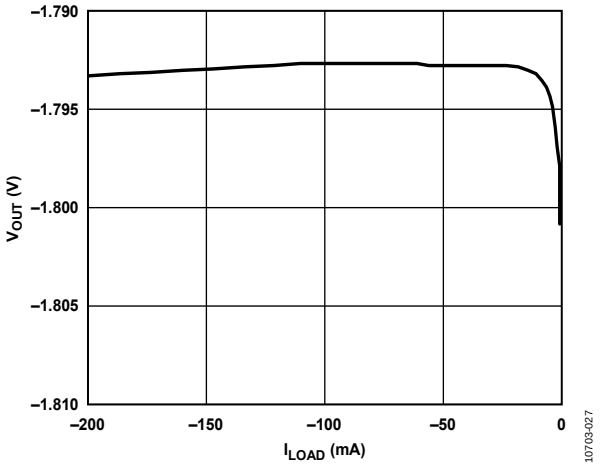


Figure 29. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), V_{OUT} = −1.8 V

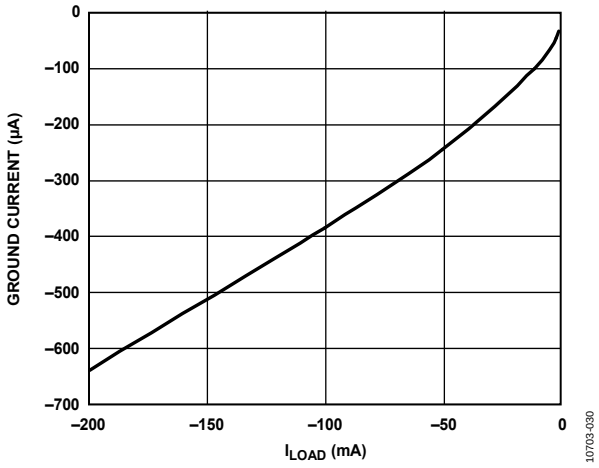


Figure 32. Ground Current vs. Load Current (I_{LOAD}), V_{OUT} = −1.8 V

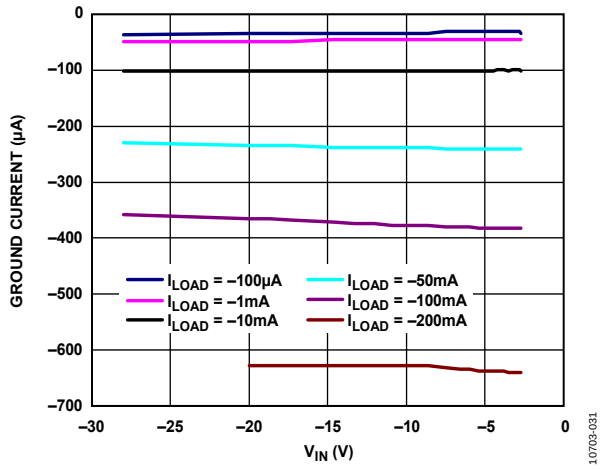


Figure 33. Ground Current vs. Input Voltage (V_{IN}), V_{OUT} = −1.8 V

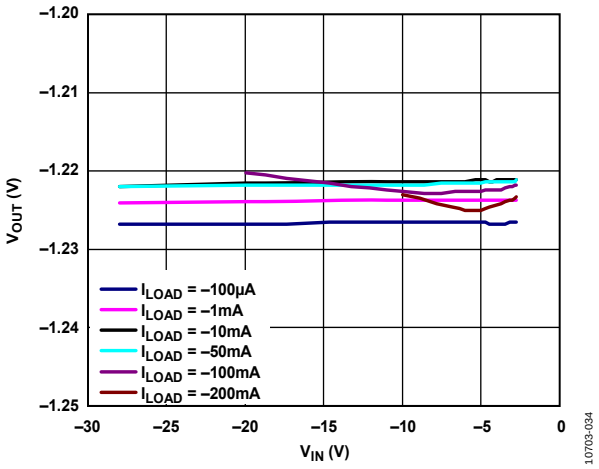


Figure 36. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), V_{OUT} = −1.22 V

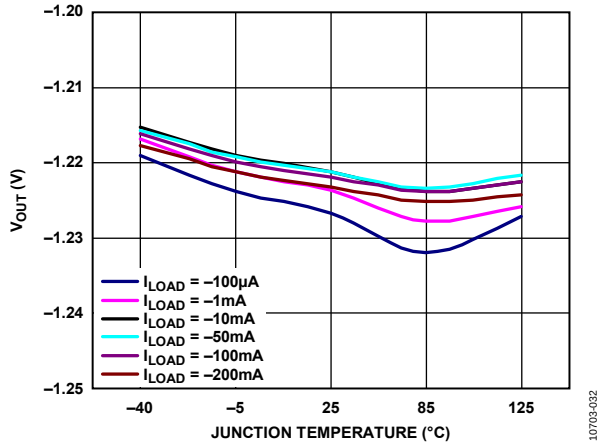


Figure 34. Output Voltage (V_{OUT}) vs. Junction Temperature (T_J), V_{OUT} = −1.22 V

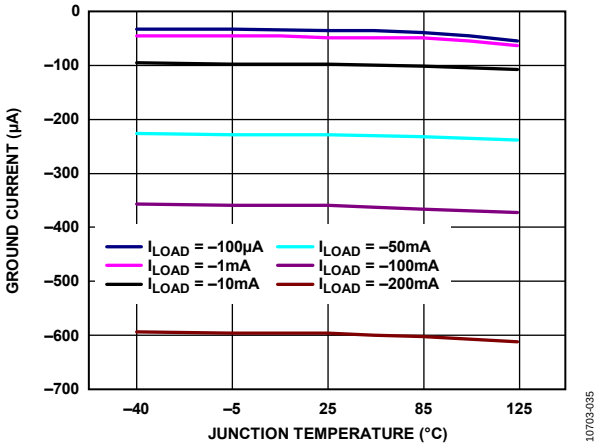


Figure 37. Ground Current vs. Junction Temperature (T_J), V_{OUT} = −1.22 V

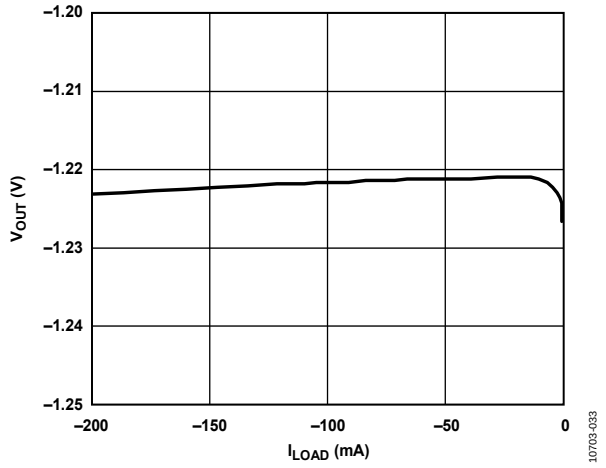


Figure 35. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), V_{OUT} = −1.22 V

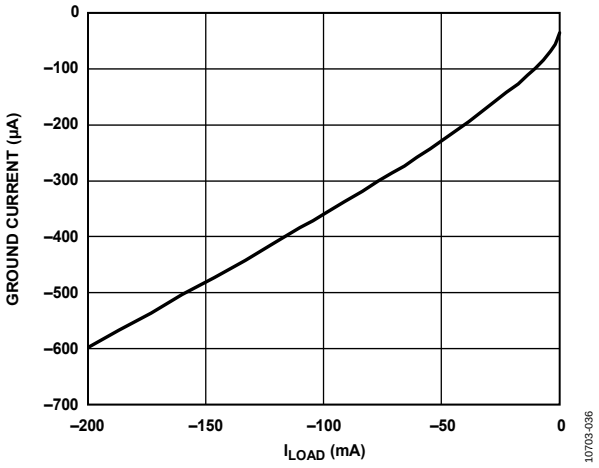


Figure 38. Ground Current vs. Load Current (I_{LOAD}), V_{OUT} = −1.22 V

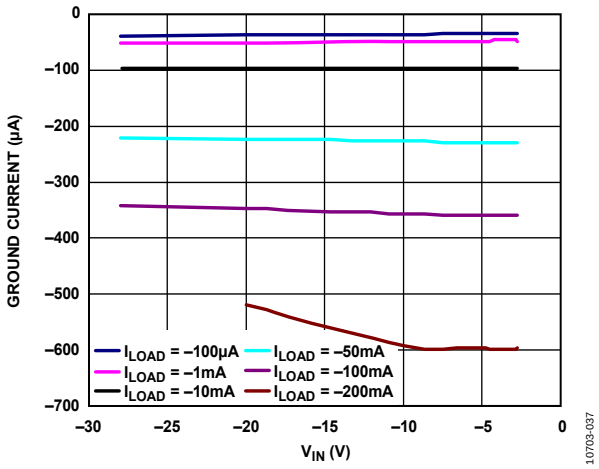


Figure 39. Ground Current vs. Input Voltage (V_{IN}), V_{OUT} = −1.22 V

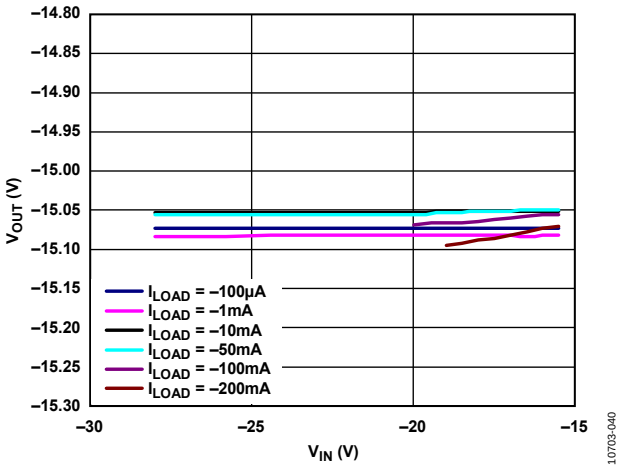


Figure 42. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), Adjustable Output Voltage, V_{OUT} = −15 V

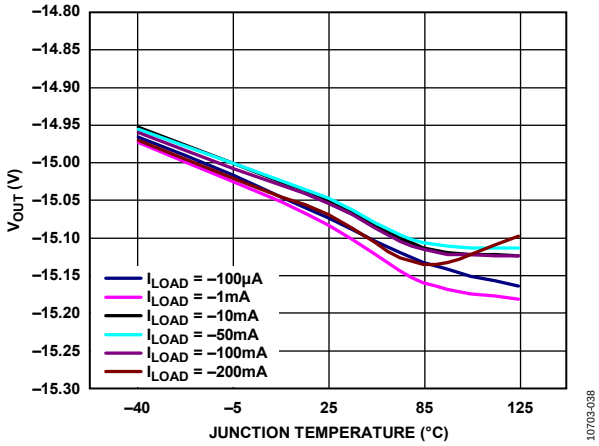


Figure 40. Output Voltage (V_{OUT}) vs. Junction Temperature (T_J), Adjustable Output Voltage, V_{OUT} = −15 V

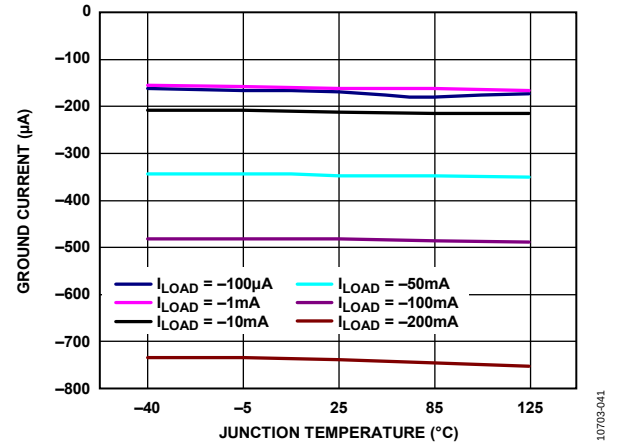


Figure 43. Ground Current vs. Junction Temperature (T_J), Adjustable Output Voltage, V_{OUT} = −15 V

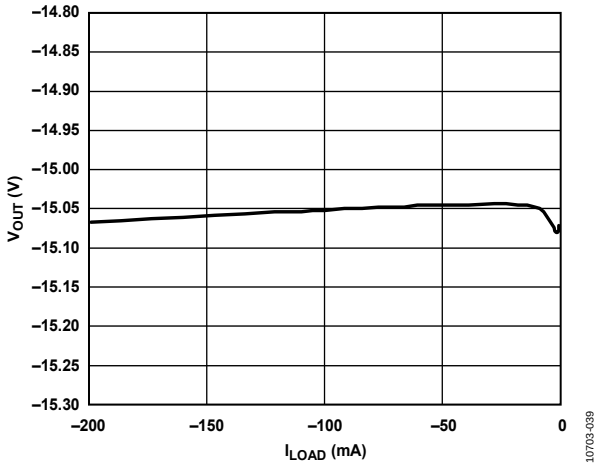


Figure 41. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), Adjustable Output Voltage, V_{OUT} = −15 V

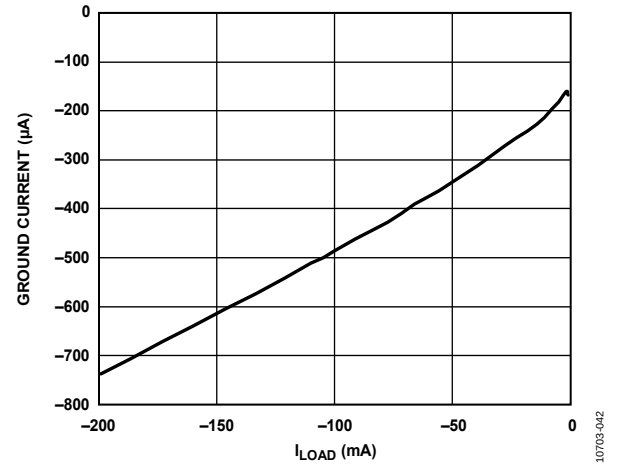


Figure 44. Ground Current vs. Load Current (I_{LOAD}), Adjustable Output Voltage, V_{OUT} = −15 V

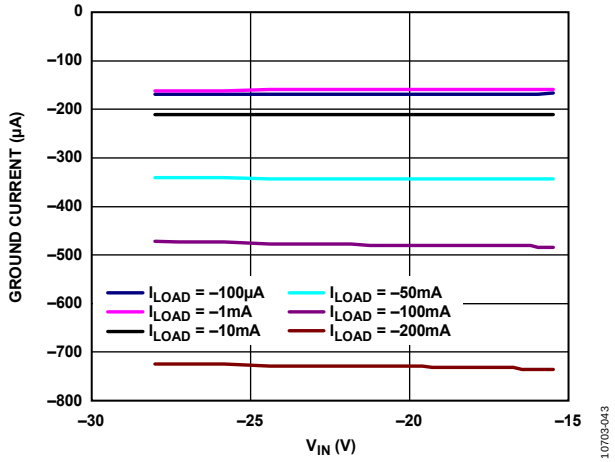


Figure 45. Ground Current vs. Input Voltage (V_{IN}), Adjustable Output Voltage, V_{OUT} = −15 V

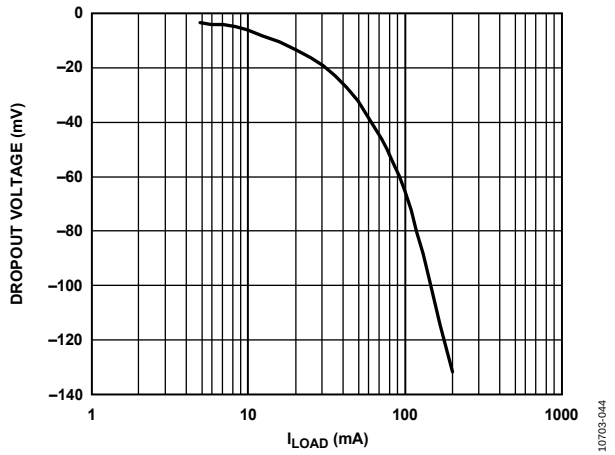


Figure 46. Dropout Voltage vs. Load Current (I_{LOAD}), Adjustable Output Voltage, V_{OUT} = −15 V

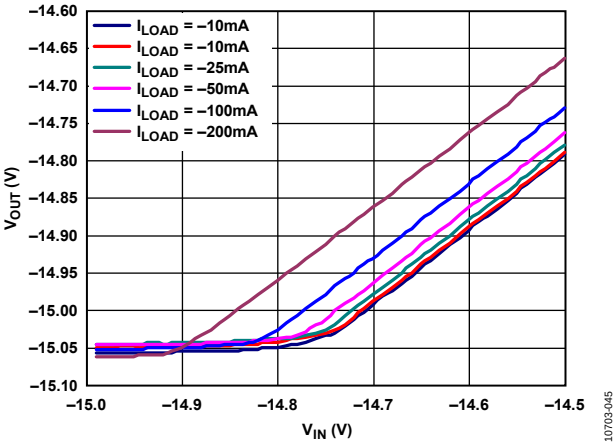


Figure 47. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) in Dropout, Adjustable Output Voltage, V_{OUT} = −15 V

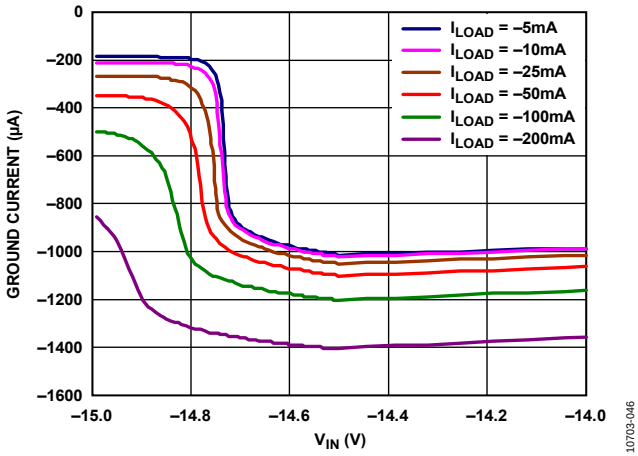


Figure 48. Ground Current vs. Input Voltage (V_{IN}) in Dropout, V_{OUT} = −15 V

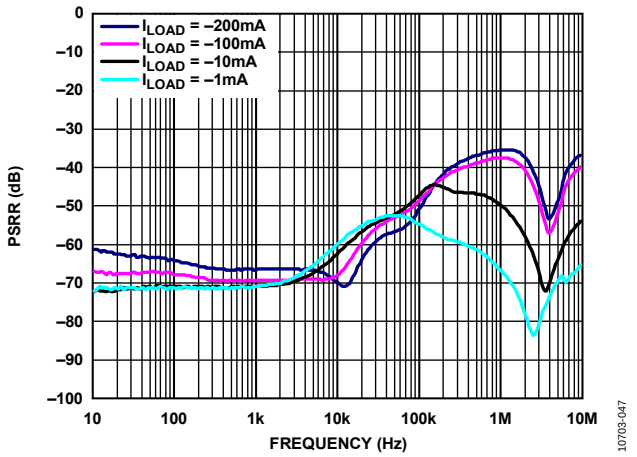


Figure 49. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{OUT} = −1.22 V vs. Different Load Currents (I_{LOAD}), V_{IN} = −2.7 V

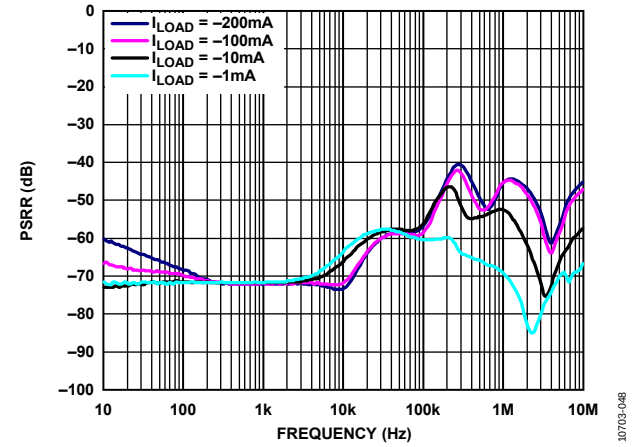


Figure 50. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{OUT} = −1.22 V vs. Different Load Currents (I_{LOAD}), V_{IN} = −5.7 V

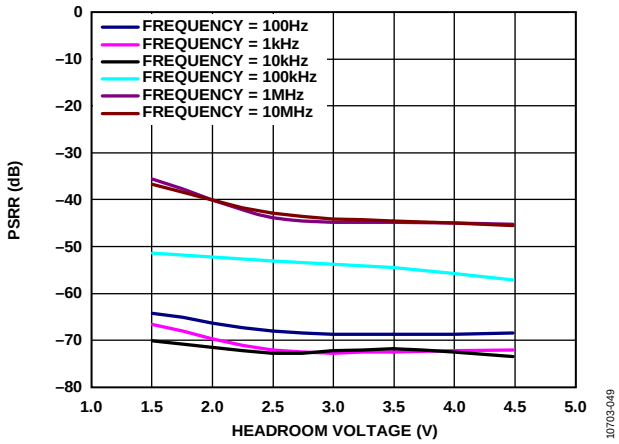


Figure 51. Power Supply Rejection Ratio (PSRR) vs. Headroom Voltage, V_{OUT} = −1.22 V, Load Current (I_{LOAD}) = −200 mA

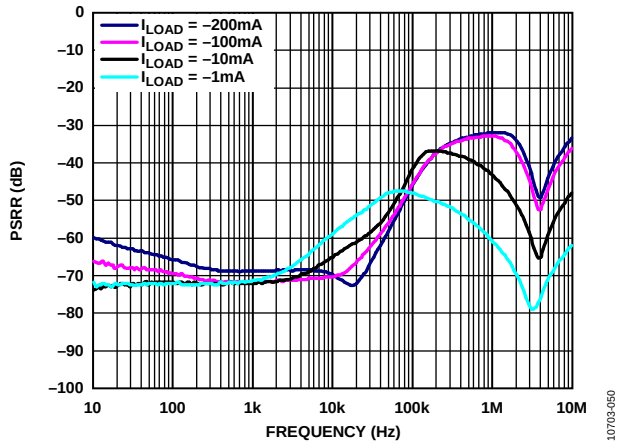


Figure 52. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{OUT} = −1.8 V vs. Different Load Currents (I_{LOAD}), V_{IN} = −2.8 V

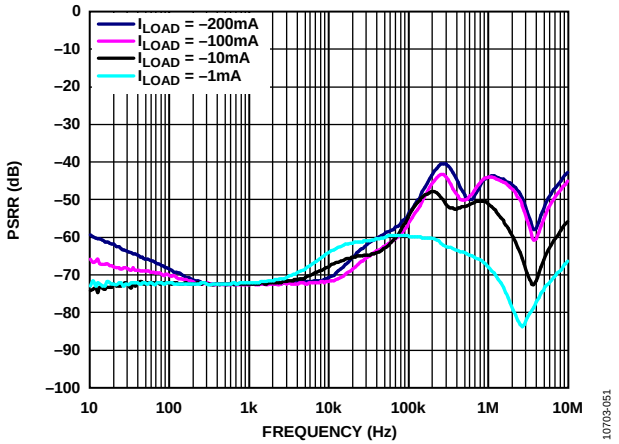


Figure 53. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{OUT} = −1.8 V vs. Different Load Currents (I_{LOAD}), V_{IN} = −5.5 V

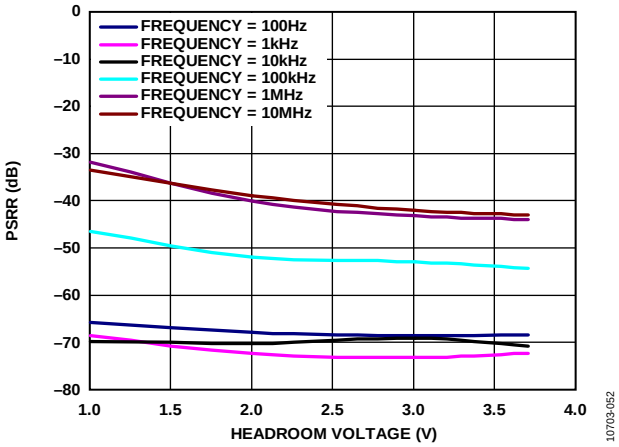


Figure 54. Power Supply Rejection Ratio (PSRR) vs. Headroom Voltage, V_{OUT} = −1.8 V, Load Current (I_{LOAD}) = −200 mA

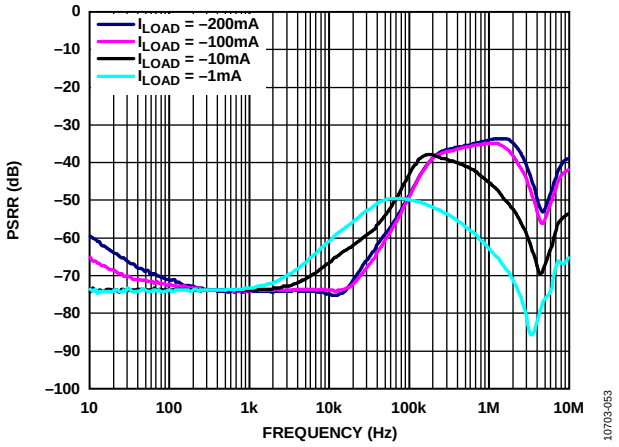


Figure 55. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{OUT} = −3 V vs. Different Load Currents (I_{LOAD}), V_{IN} = −4.0 V

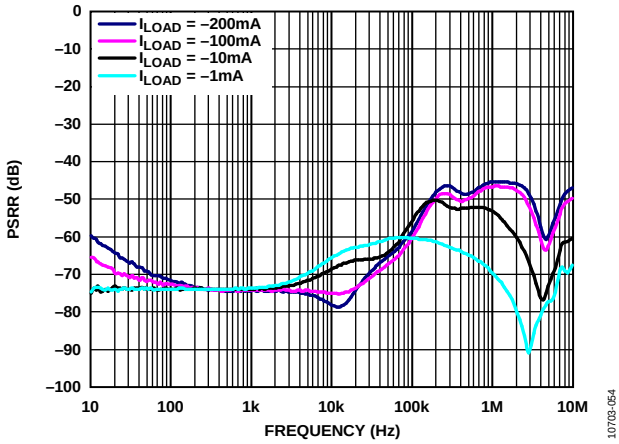


Figure 56. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{OUT} = −3 V vs. Different Load Currents (I_{LOAD}), V_{IN} = −5.5 V

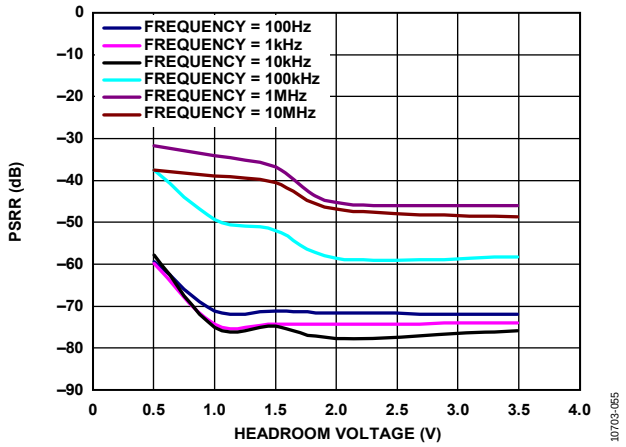


Figure 57. Power Supply Rejection Ratio (PSRR) vs. Headroom Voltage, V_{OUT} = −3 V, Load Current (I_{LOAD}) = −200 mA

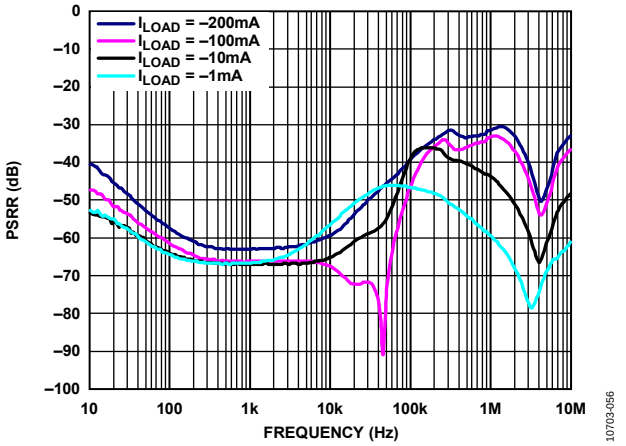


Figure 58. Power Supply Rejection Ratio (PSRR) vs. Frequency, Adjustable Output Voltage, V_{OUT} = −15 V vs. Different Load Currents (I_{LOAD}), V_{IN} = −15.5 V with Noise Reduction Network

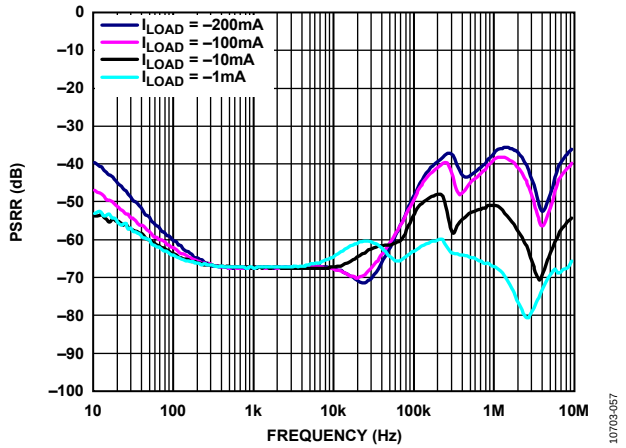


Figure 59. Power Supply Rejection Ratio (PSRR) vs. Frequency, Adjustable Output Voltage, V_{OUT} = −15 V vs. Different Load Currents (I_{LOAD}), V_{IN} = −16.5 V with Noise Reduction Network

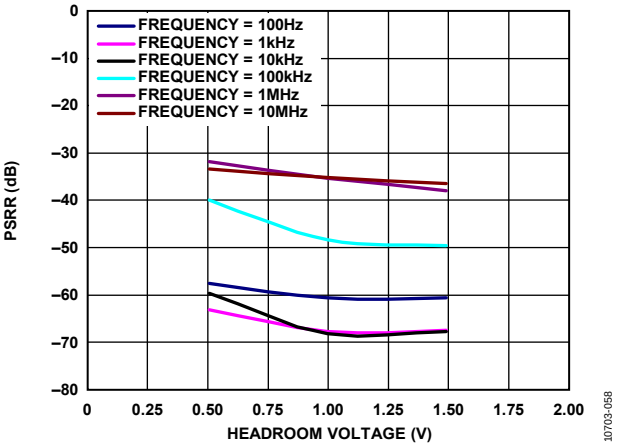


Figure 60. Power Supply Rejection Ratio (PSRR) vs. Headroom Voltage, Adjustable Output Voltage, V_{OUT} = −15 V with Noise Reduction Network, Load Current (I_{LOAD}) = −200 mA

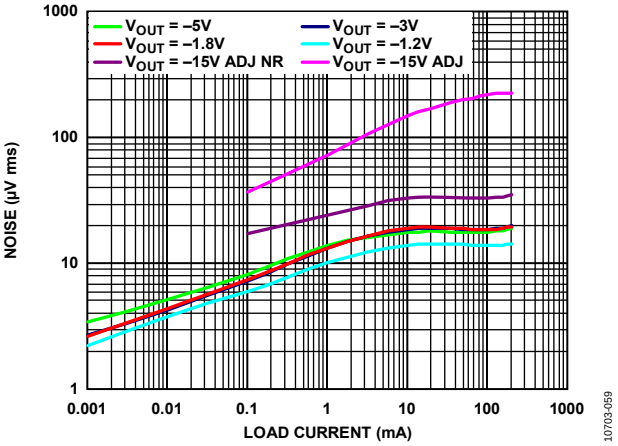


Figure 61. RMS Noise vs. Load Current (I_{LOAD}), Various Output Voltages

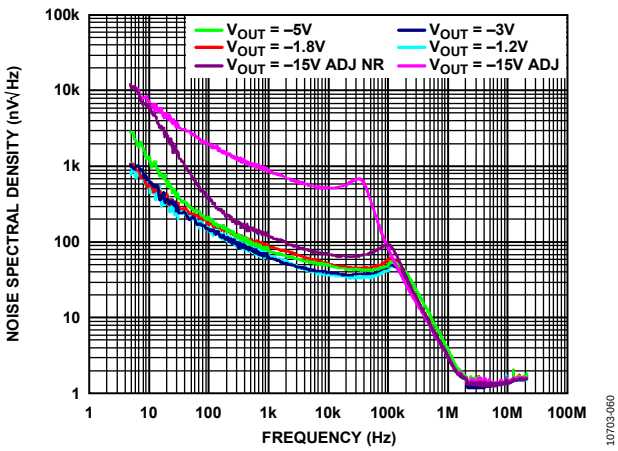


Figure 62. Noise Spectral Density, Various Output Voltages

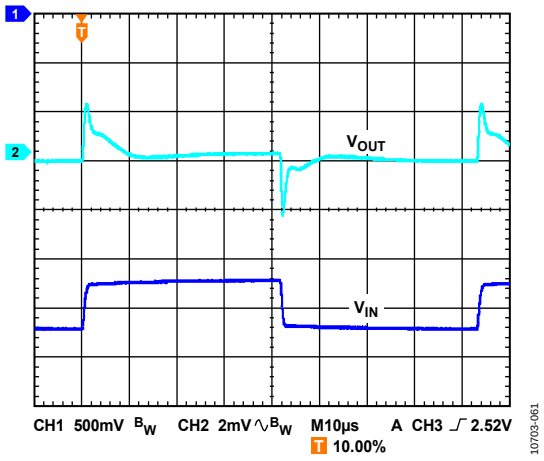


Figure 63. Line Transient Response, 500 mV Step, V_{OUT} = −1.22 V, I_{LOAD} = −200 mA

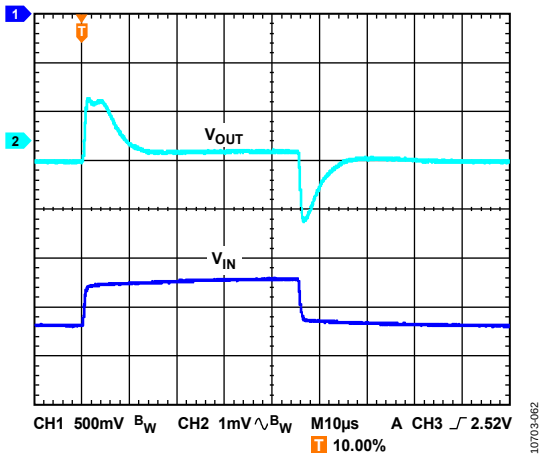


Figure 64. Line Transient Response, 500 mV Step, V_{OUT} = −1.22 V, I_{LOAD} = −10 mA

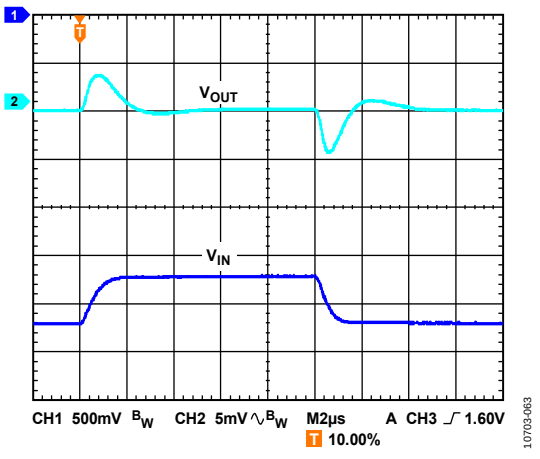


Figure 65. Line Transient Response, 500 mV Step, V_{OUT} = −1.8 V, I_{LOAD} = −200 mA

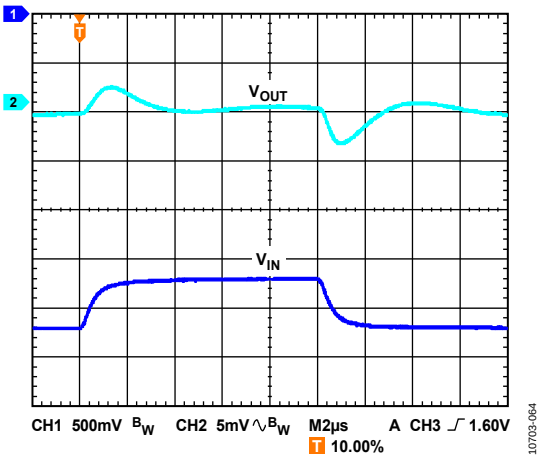


Figure 66. Line Transient Response, 500 mV Step, V_{OUT} = −1.8 V, I_{LOAD} = −10 mA

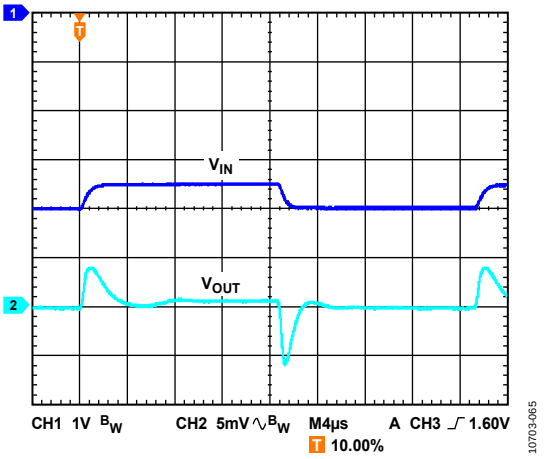


Figure 67. Line Transient Response, 500 mV Step, V_{OUT} = −3 V, I_{LOAD} = −200 mA

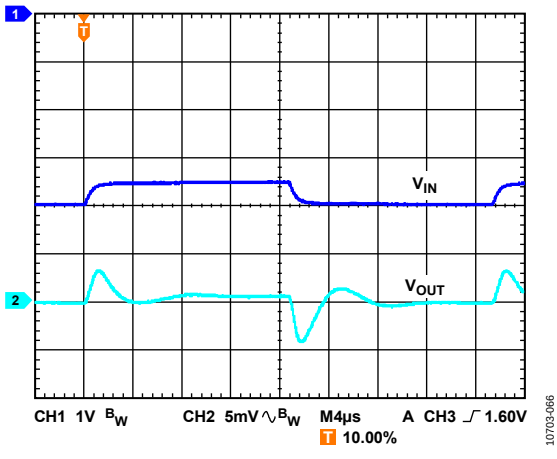


Figure 68. Line Transient Response, 500 mV Step, V_{OUT} = −3 V, I_{LOAD} = −10 mA

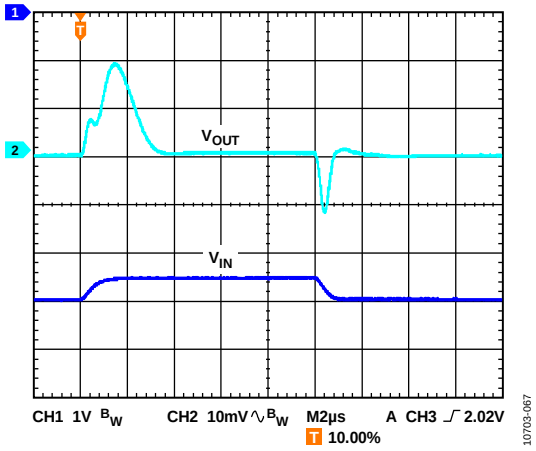


Figure 69. Line Transient Response, 500 mV Step, V_{OUT} = −5 V, I_{LOAD} = −200 mA

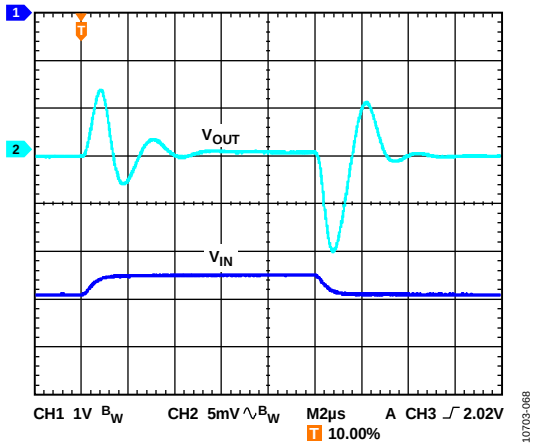


Figure 70. Line Transient Response, 500 mV Step, V_{OUT} = −5 V, I_{LOAD} = −10 mA

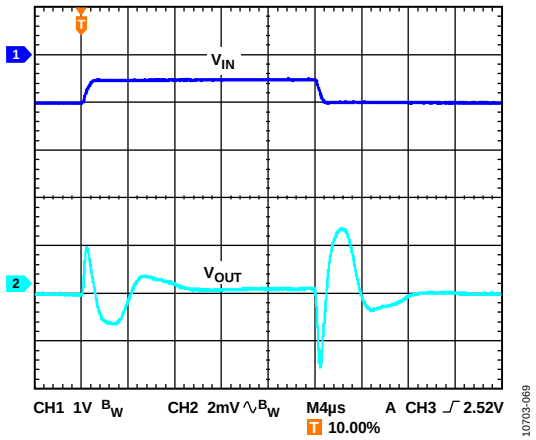


Figure 71. Line Transient Response, 500 mV Step, V_{OUT} = −15 V, Noise Reduction Network, I_{LOAD} = −200 mA

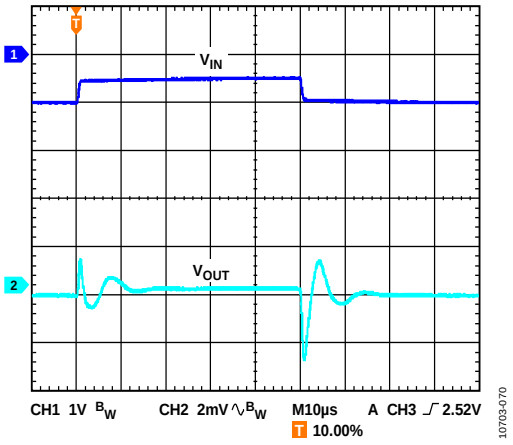


Figure 72. Line Transient Response, 500 mV Step, V_{OUT} = −15 V, Noise Reduction Network, I_{LOAD} = −10 mA

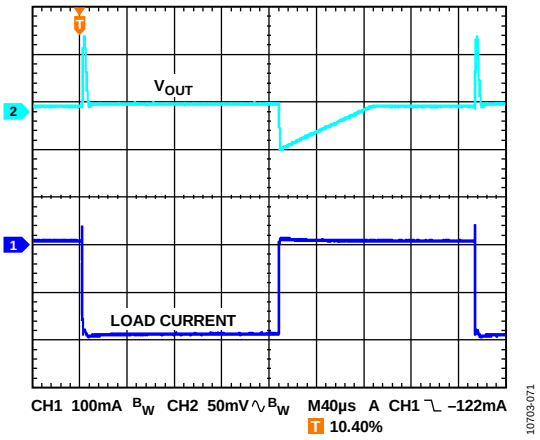


Figure 73. Load Transient Response, V_{OUT} = −1.22 V, I_{LOAD} = −1 mA to −200 mA, Load Step = 1 A/µs

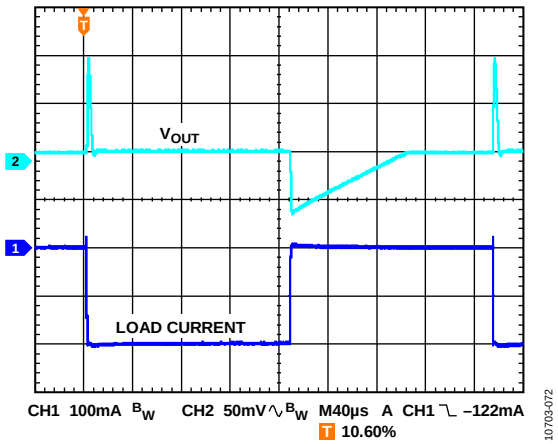


Figure 74. Load Transient Response, V_{OUT} = −3 V, I_{LOAD} = −1 mA to −200 mA, Load Step = 1 A/µs

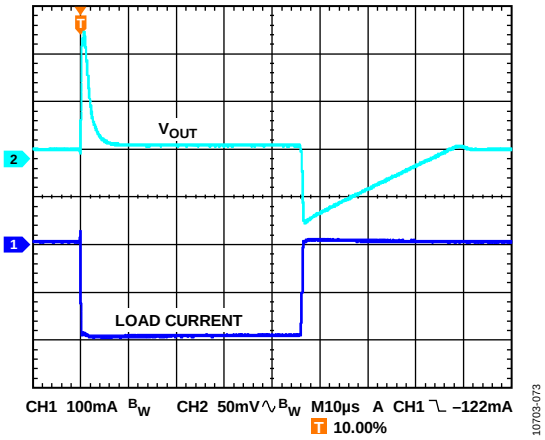


Figure 75. Load Transient Response, V_{OUT} = −5 V, I_{LOAD} = −1 mA to −200 mA, Load Step = 1 A/µs

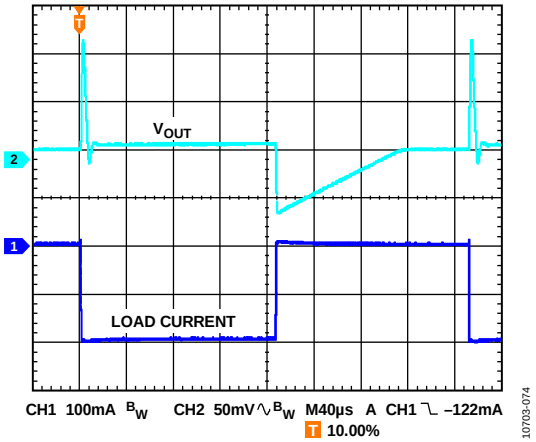


Figure 76. Load Transient Response, V_{OUT} = −15 V, I_{LOAD} = −1 mA to −200 mA, Load Step = 1 A/µs, Noise Reduction Network

THEORY OF OPERATION

The ADP7182 is a low quiescent current, LDO linear regulator that operates from −2.7 V to −28 V and can provide up to −200 mA of output current. Drawing a low −650 µA of quiescent current (typical) at full load makes the ADP7182 ideal for battery-powered portable equipment. Maximum shutdown current consumption is −8 µA at room temperature.

Optimized for use with small 2.2 µF ceramic capacitors, the ADP7182 provides excellent transient performance.

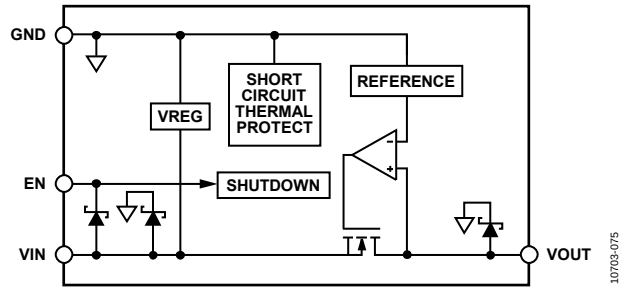


Figure 77. Fixed Output Voltage Internal Block Diagram

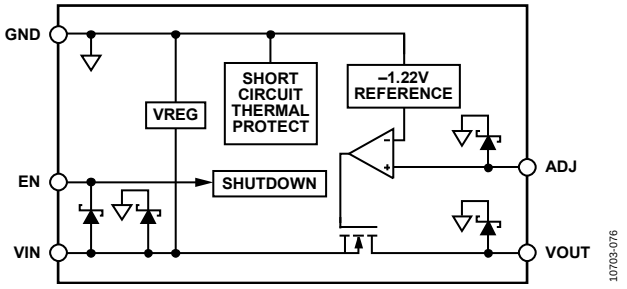


Figure 78. Adjustable Output Voltage Internal Block Diagram

Internally, the ADP7182 consists of a reference, an error amplifier, a feedback voltage divider, and an NMOS pass transistor. Output current is delivered via the NMOS pass transistor, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is more positive than the reference voltage, the gate of the NMOS transistor is pulled toward GND, allowing more current to pass and increasing the output voltage. If the feedback voltage is more negative than the reference voltage, the gate of the NMOS transistor is pulled toward $-V_{IN}$, allowing less current to pass and decreasing the output voltage.

The ESD protection devices are shown in the block diagram as Zener diodes (see Figure 77 and Figure 78).

ADJUSTABLE MODE OPERATION

The ADP7182 is available in a fixed output voltage and an adjustable mode version with an output voltage that can be set to between −1.22 V and −27 V by an external voltage divider. The output voltage can be set according to

$$-V_{OUT} = -1.22\ \text{V}\ (1 + R_{FB1}/R_{FB2})$$

R_{FB2} must be less than 120 kΩ to minimize the output voltage errors due to the leakage current of the ADJ pin. The error voltage caused by the ADJ pin leakage current is the parallel combination of R_{FB1} and R_{FB2} times the ADJ pin leakage current.

For example, when $R_{FB1} = R_{FB2} = 120$ kΩ, the output voltage is −2.44 V and the error due to the typical ADJ pin leakage current (10 nA) is 60 kΩ times 10 nA, or 6 mV. This example results in an output voltage error of 0.245%.

The addition of a small capacitor (~100 pF) in parallel with R_{FB1} can improve the stability of the ADP7182. Larger values of capacitance also reduce the noise and improve PSRR (see the Noise Reduction of the Adjustable section).

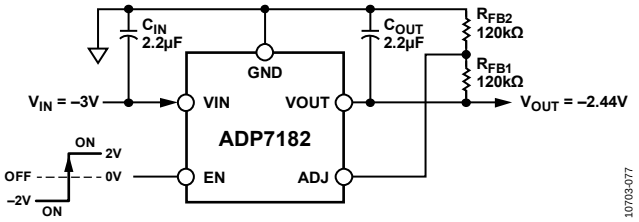


Figure 79. Setting Adjustable Output Voltage

APPLICATIONS INFORMATION

ADIsimPower DESIGN TOOL

The ADP7182 is supported by the ADIsimPower™ design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and devices count taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about, and to obtain ADIsimPower design tools, visit www.analog.com/ADIsimPower.

CAPACITOR SELECTION

Output Capacitor

The ADP7182 is designed for operation with small space-saving ceramic capacitors; however, it functions with most commonly used capacitors as long as care is taken with regard to the ESR value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 2.2 µF capacitance with an ESR of 0.2 Ω or less is recommended to ensure the stability of the ADP7182. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP7182 to large changes in load current. Figure 80 shows the transient responses for an output capacitance value of 2.2 µF.

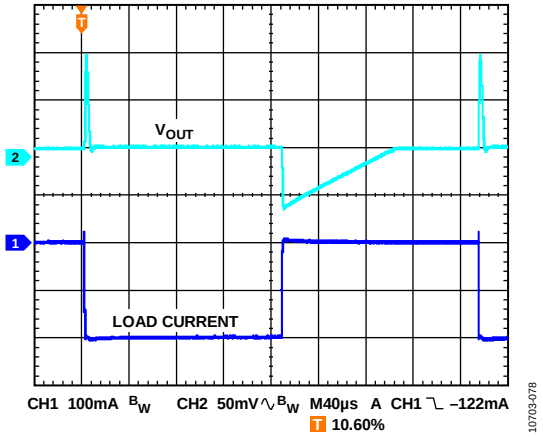


Figure 80. Output Transient Response, C_{OUT} = 2.2 µF

Input Bypass Capacitor

Connecting a 2.2 µF capacitor from VIN to GND reduces the circuit sensitivity to PCB layout, especially when long input traces or high source impedance are encountered. When more than 2.2 µF of output capacitance is required, increase the input capacitance to match it.

Input and Output Capacitor Properties

As long as they meet the minimum capacitance and maximum ESR requirements, any good quality ceramic capacitors can be used with the ADP7182. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage.

Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 25 V or 50 V are recommended. Due to their poor temperature and dc bias characteristics, Y5V and Z5U dielectrics are not recommended.

Figure 81 depicts the capacitance vs. voltage bias characteristics of an 0805, 2.2 µF, 25 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is ~ ±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

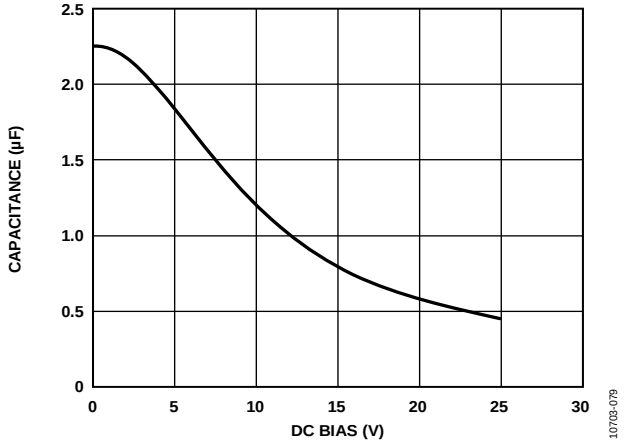


Figure 81. Capacitance vs. DC Bias Characteristics

Use Equation 1 to determine the worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

where:
C_{BIAS} is the effective capacitance at the operating voltage, which is −3 V for this example.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is 10%, and the C_{BIAS} is 2.08 µF at a 3 V bias, as shown in Figure 81.

Substituting these values in Equation 1 yields

$$C_{EFF} = 2.08\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 1.59\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage of −3 V.

To guarantee the performance of the ADP7182, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

ENABLE PIN OPERATION

The ADP7182 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. When EN is at ±2 V with respect to GND, VOUT turns on, and when EN is at 0 V, VOUT turns off. For automatic startup, EN can be connected to VIN. When the device is disabled, a ~220 kΩ resistor connects to the VOUT pin, which pulls the VOUT pin up to GND.

The ADP7182 provides a dual polarity enable pin (EN) that turns on the LDO when $|V_{EN}| \geq 2$ V. The enable voltage can be positive or negative with respect to ground.

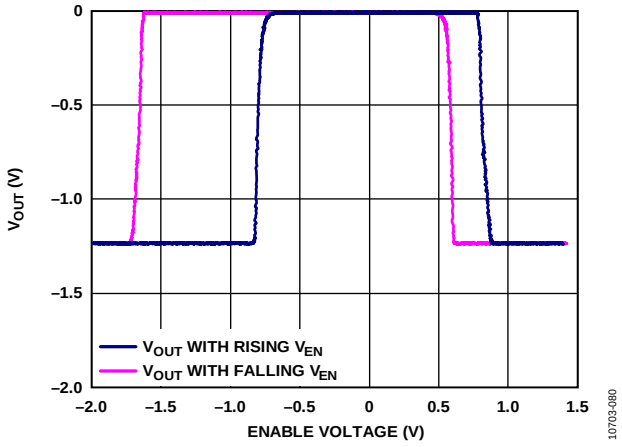


Figure 82. Typical EN Pin Operation

Figure 82 shows the typical hysteresis of the EN pin. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

Figure 83 shows typical EN thresholds when the input voltage varies from −2.7 V to −28 V.

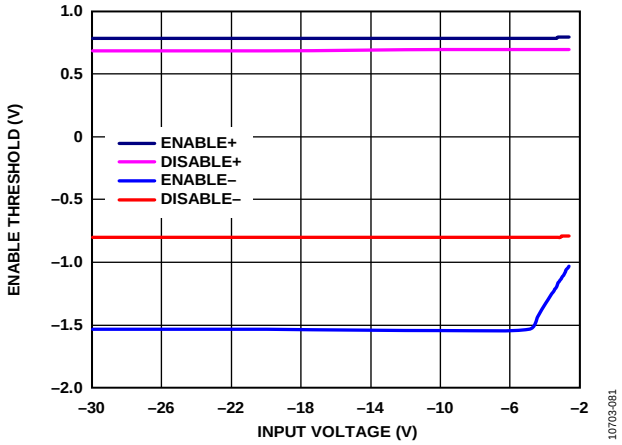


Figure 83. Typical EN Pin Thresholds vs. Input Voltage

Figure 84 and Figure 85 show the start-up behavior for a −5 V output with positive and negative going enable signals.

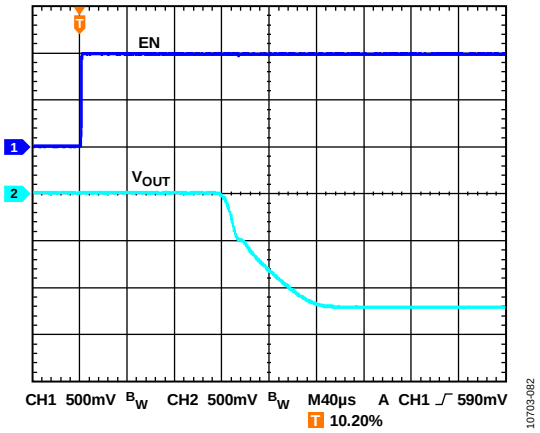


Figure 84. Typical Start-Up Behavior, Positive Going Enable

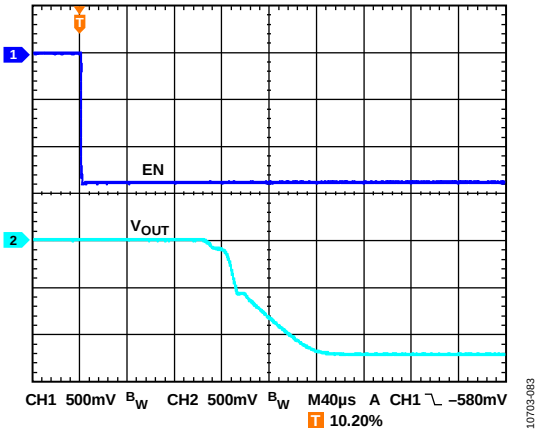


Figure 85. Typical Start-Up Behavior, Negative Going Enable

SOFT START

The ADP7182 uses an internal soft start to limit the inrush current when the output is enabled. The start-up time for the −5 V option is approximately 450 µs from the time the EN active threshold is crossed to when the output reaches 90% of the final value. As shown in Figure 86, the start-up time is dependent on the output voltage setting.

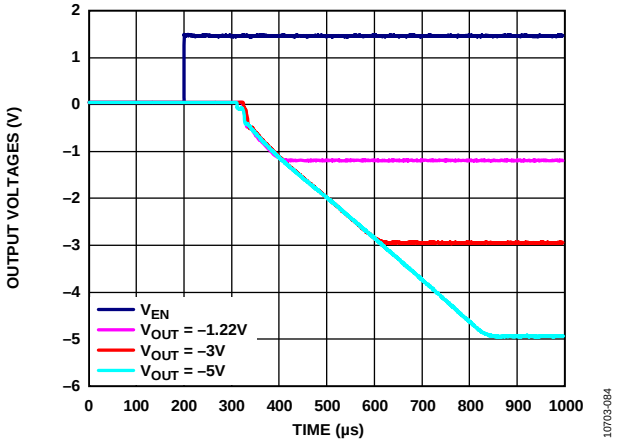


Figure 86. Typical Start-Up Behavior, Different Output Voltages

NOISE REDUCTION OF THE ADJUSTABLE ADP7182

The ultralow output noise of the fixed output ADP7182 is achieved by keeping the LDO error amplifier in unity gain and setting the reference voltage equal to the output voltage. This architecture does not work for an adjustable output voltage LDO. The adjustable output ADP7182 uses the more conventional architecture where the reference voltage is fixed and the error amplifier gain is a function of the output voltage. The disadvantage of the conventional LDO architecture is that the output voltage noise is proportional to the output voltage.

The adjustable LDO circuit can be modified slightly to reduce the output voltage noise to levels close to that of the fixed output of the ADP7182. The circuit shown in Figure 87 adds two additional components to the output voltage setting resistor divider. C_{NR} and R_{NR} are added in parallel with R_{FB1} to reduce the ac gain of the error amplifier. R_{NR} is chosen to be nearly equal to R_{FB2}; this limits the ac gain of the error amplifier to approximately 6 dB. The actual gain is the parallel combination of R_{NR} and R_{FB1} divided by R_{FB2}. This resistance ensures that the error amplifier always operates at greater than unity gain.

C_{NR} is chosen by setting the reactance of C_{NR} equal to $R_{FB1} - R_{NR}$ at a frequency between 10 Hz and 100 Hz. This capacitance sets the frequency where the ac gain of the error amplifier is 3 dB down from the dc gain.

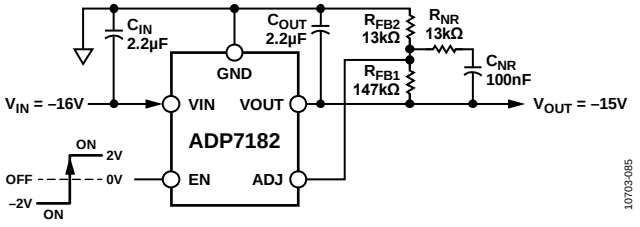


Figure 87. Noise Reduction Modification to Adjustable LDO

The noise of the LDO is approximately the noise of the fixed output LDO (typically 18 µV rms) times R_{FB2}, divided by the parallel combination of R_{NR} and R_{FB1}. Based on the component values shown in Figure 87, the ADP7182 has the following characteristics:

- DC gain of 12.3 (21.8 dB)
- 3 dB roll-off frequency of 10.8 Hz
- High frequency ac gain of 1.92 (5.67 dB)
- Noise reduction factor of 6.41 (16.13 dB)
- Measured rms noise of the adjustable LDO at −200 mA without noise reduction of 220 µV rms
- Measured rms noise of the adjustable LDO at −200 mA with noise reduction circuit of 35 µV rms
- Calculated rms noise of the adjustable LDO with noise reduction (assuming 18 µV rms for fixed voltage option) of 34.5 µV rms

The noise of the LDO is approximately the noise of the fixed output LDO (typically 18 µV rms) times the high frequency ac gain.

The following equation shows the calculation with the values shown in Figure 87.

$$18\,\mu V \times \left(1 + \left(\frac{1}{1/13\,k\Omega + 1/147\,k\Omega}\right)/13\,k\Omega\right) \quad (2)$$

Figure 88 shows the difference in noise spectral density for the adjustable ADP7182 set to −15 V with and without the noise reduction network. In the 100 Hz to 30 kHz frequency range, the reduction in noise is significant.

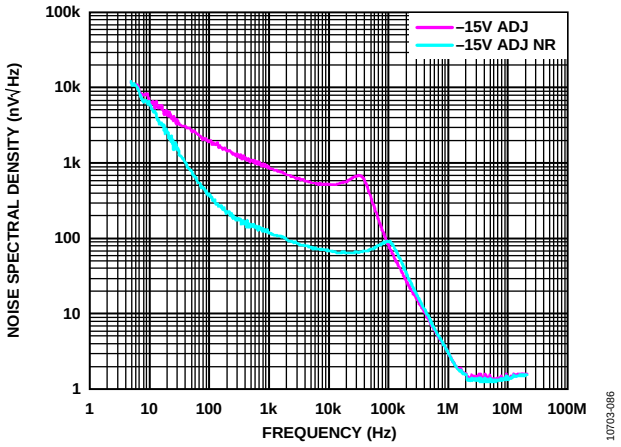


Figure 88. −15 V Adjustable ADP7182 with and without the Noise Reduction Network (CNR and RNR)

CURRENT-LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP7182 is protected against damage due to excessive power dissipation by current-limit and thermal overload protection circuits. The ADP7182 is designed to limit current when the output load reaches −350 mA (typical). When the output load exceeds −350 mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation) when the junction temperature starts to rise above 150°C, the output is turned off, reducing the output current to 0 mA. When the junction temperature falls below 135°C, the output is turned on again, and the output current is restored to the nominal value.

Consider the case where a hard short from VOUT to ground occurs. At first, the ADP7182 limits current so that only −350 mA is conducted into the short. If self-heating of the junction is great enough to cause the temperature to rise above 150°C, thermal shutdown is activated, turning off the output and reducing the output current to 0 mA. As the junction temperature cools and falls below 135°C, the output turns on and conducts −350 mA into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between −350 mA and 0 mA that continues as long as the short remains at the output.

Current-limit and thermal overload protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so that the junction temperatures do not exceed 125°C.

THERMAL CONSIDERATIONS

In most applications, the ADP7182 does not dissipate much heat due to the high efficiency. However, in applications with high ambient temperature, and high supply voltage to output voltage differential, the heat dissipated in the package is large enough that it can cause the junction temperature of the die to exceed the maximum junction temperature of 125°C.

When the junction temperature exceeds 150°C, the converter enters thermal shutdown. It recovers only after the junction temperature has decreased below 135°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application is important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 3.

To guarantee reliable operation, the junction temperature of the ADP7182 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user must be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} number is dependent on the package assembly compounds that are used, and the amount of copper that solders the package VIN pins to the PCB.

Table 8 and Table 9 show typical θ_{JA} values of the 6- and 8-lead and 5-lead TSOT packages for various PCB copper sizes. Table 10 shows the typical ΨJB values of the 6- and 8-lead and and 5-lead TSOT.

Table 8. Typical θ_{JA} Values of the LFCSP

	θ_{JA} (°C/W)	
Copper Size (mm²)	**8-Lead LFCSP**	**6-Lead LFCSP**
25[1]	175	177.8
100	135.6	138.2
500	77.3	79.8
1000	65.2	67.8
6400	51	53.5

[1] Device soldered to minimum size pin traces.

Table 9. Typical θ_{JA} Values of the 5-Lead TSOT

Copper Size (mm²)	θ_{JA} (°C/W)
0[1]	170
50	152
100	146
300	134
500	131

[1] Device soldered to minimum size pin traces.

Table 10. Typical Ψ_{JB} Values

Model	Ψ_{JB} (°C/W)
6-lead LFCSP	44.1
8-lead LFCSP	18.2
5-lead TSOT	43

The junction temperature of the ADP7182 can be calculated by

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (3)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (4)$$

where:
V_{IN} and V_{OUT} are the input and output voltages, respectively.
I_{LOAD} is the load current.
I_{GND} is the ground current.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (5)$$

As shown in Equation 5, for a given ambient temperature, input-to-output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure that the junction temperature does not rise above 125°C. Figure 89 to Figure 97 show junction temperature calculations for different ambient temperatures, power dissipation, and areas of PCB copper.

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP7182. Adding thermal planes under the package also improves thermal performance. However, as listed in Table 8 and Table 9, a point of diminishing returns is reached eventually, beyond which an increase in the copper area does not yield significant reduction in the junction-to-ambient thermal resistance.

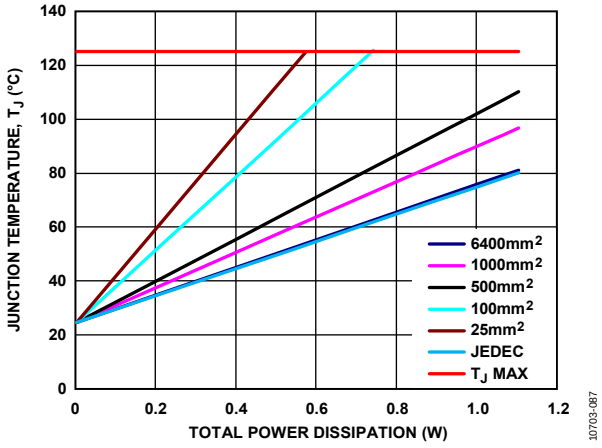


Figure 89. Junction Temperature vs. Total Power Dissipation for the 8-Lead LFCSP, T_A = 25°C

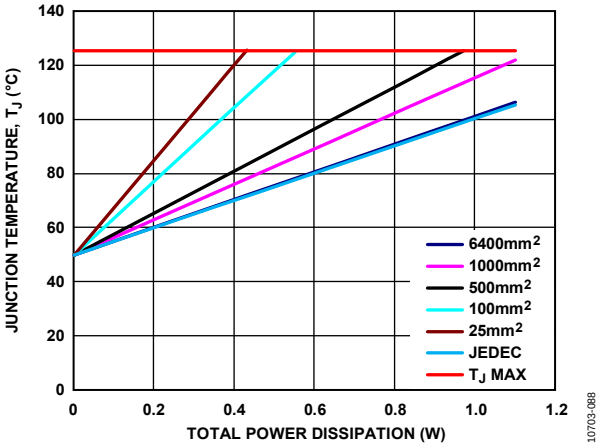


Figure 90. Junction Temperature vs. Total Power Dissipation for the 8-Lead LFCSP, T_A = 50°C

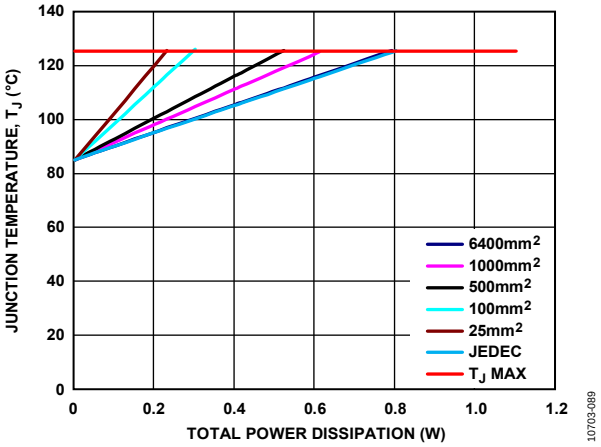


Figure 91. Junction Temperature vs. Total Power Dissipation for the 8-Lead LFCSP, T_A = 85°C

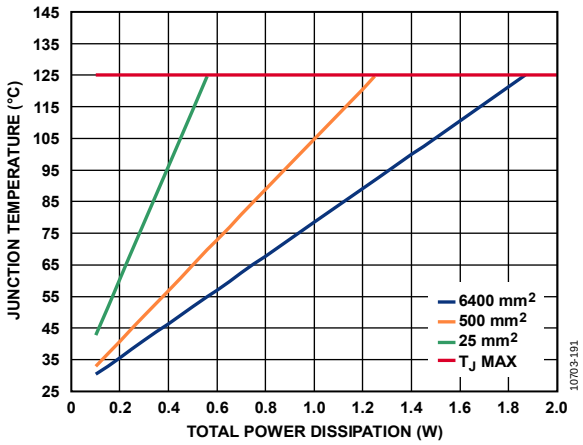


Figure 92. Junction Temperature vs. Total Power Dissipation for the 6-Lead LFCSP, T_A = 25°C

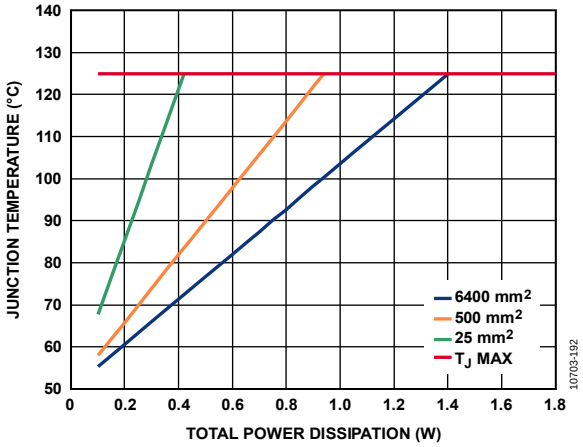


Figure 93. Junction Temperature vs. Total Power Dissipation for the 6-Lead LFCSP, T_A = 50°C

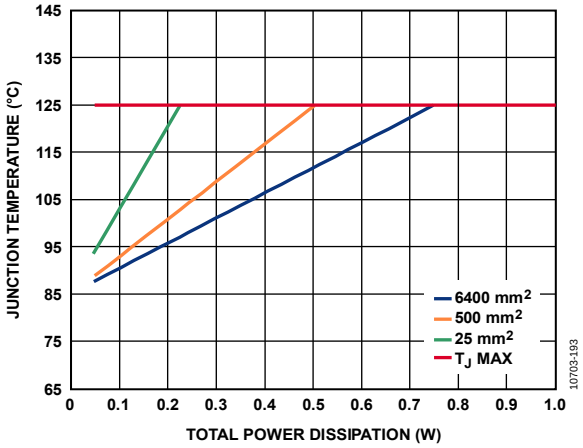


Figure 94. Junction Temperature vs. Total Power Dissipation for the 6-Lead LFCSP, T_A = 85°C

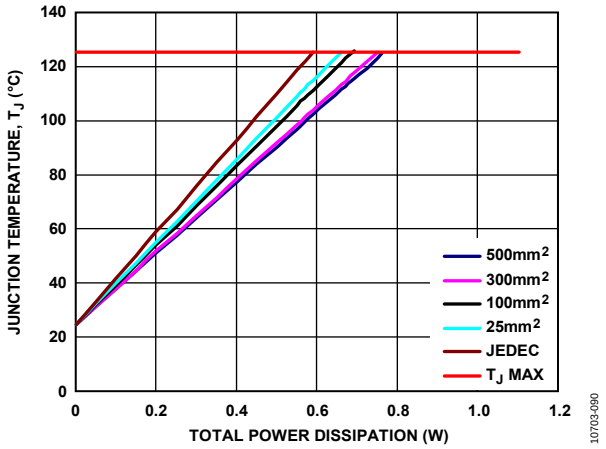


Figure 95. Junction Temperature vs. Total Power Dissipation for the 5-Lead TSOT, T_A = 25°C

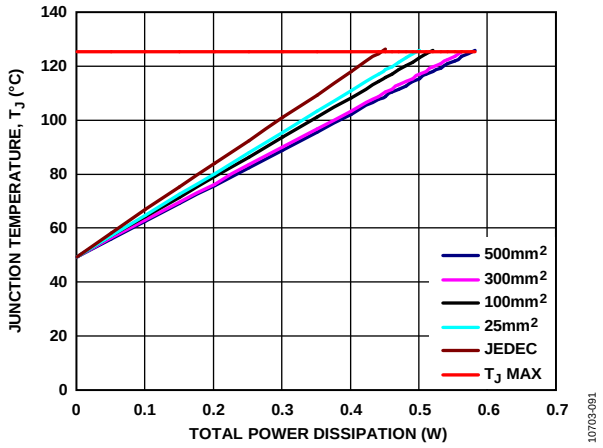


Figure 96. Junction Temperature vs. Total Power Dissipation for the 5-Lead TSOT, T_A = 50°C

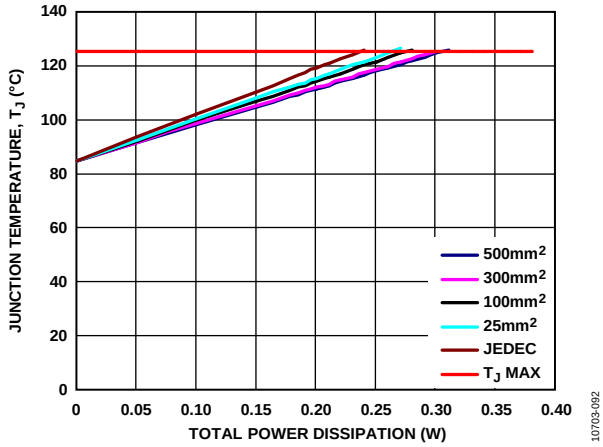


Figure 97. Junction Temperature vs. Total Power Dissipation for the 5-Lead TSOT, T_A = 85°C

Thermal Characterization Parameter, Ψ_{JB}

When the board temperature is known, use the thermal characterization parameter, Ψ_{JB}, to estimate the junction temperature rise (see Figure 98 and Figure 100). Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (6)$$

The typical value of Ψ_{JB} is 18.2°C/W for the 8-lead LFCSP package, 44.1°C/W for the 6-lead LFCSP package and 43°C/W for the 5-lead TSOT package.

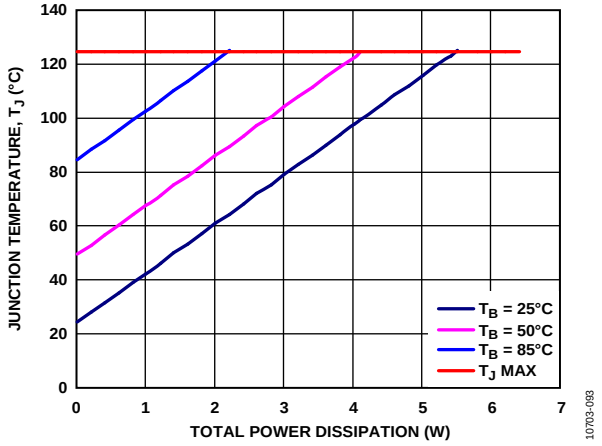


Figure 98. Junction Temperature vs. Total Power Dissipation for the 8-Lead LFCSP, T_A = 85°C

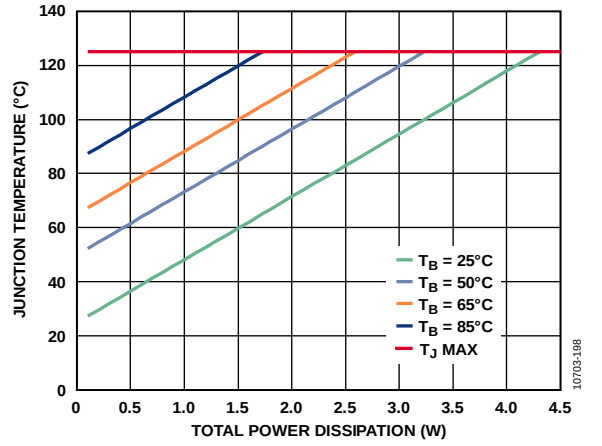


Figure 99. Junction Temperature vs. Total Power Dissipation for the 6-Lead LFCSP, T_A = 85°C

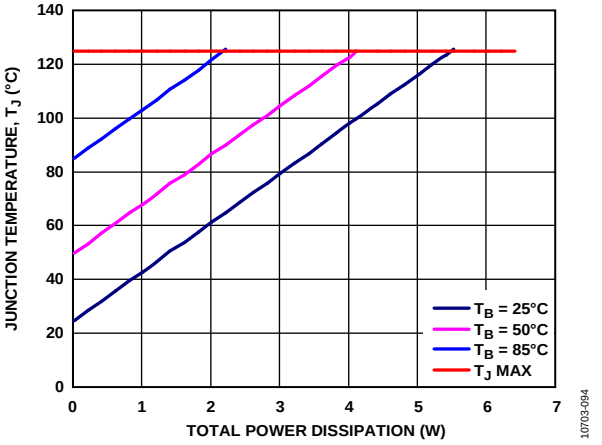


Figure 100. Junction Temperature vs. Total Power Dissipation for the 5-Lead TSOT, T_A = 85°C

PCB LAYOUT CONSIDERATIONS

Place the input capacitor as close as possible to the VIN and GND pins. Place the output capacitor as close as possible to the VOUT and GND pins. Use of 1206 or 0805 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

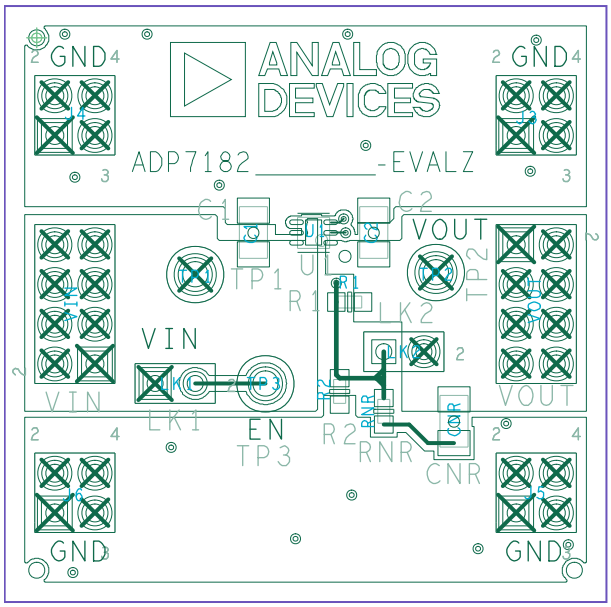


Figure 101. Example of the 6-Lead LFCSP PCB Layout

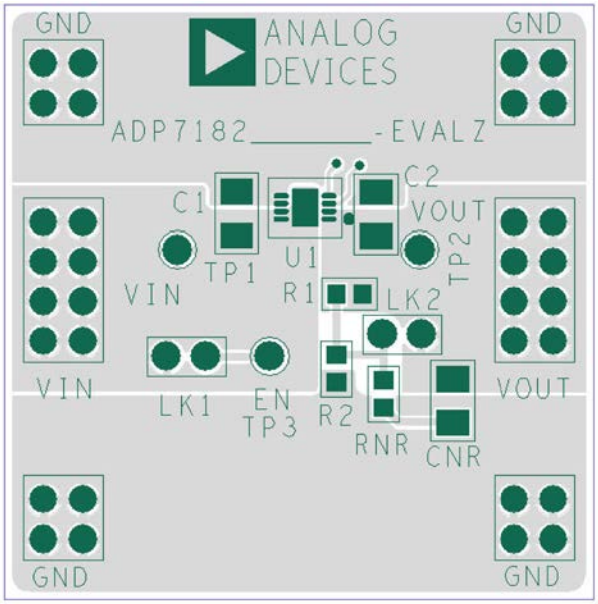


Figure 102. Example of the 8-Lead LFCSP PCB Layout

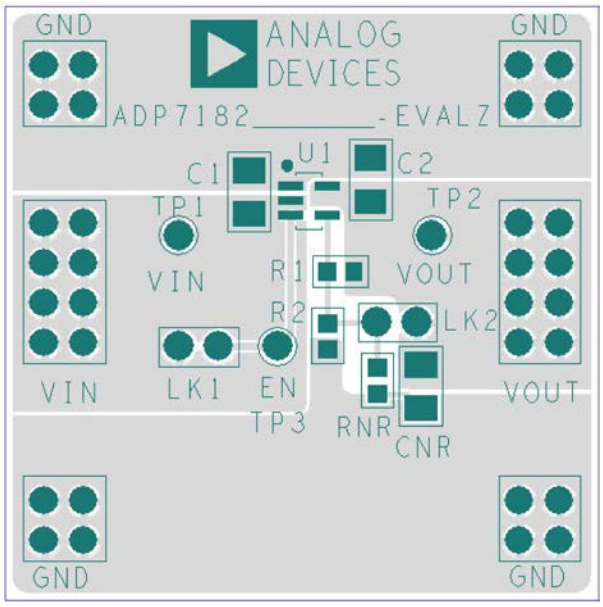


Figure 103. Example of the 5-Lead TSOT PCB Layout

Table 11. Recommended LDOs for Very Low Noise Operation

Device Number	V_{IN} Range (V)	V_{OUT} Fixed (V)	V_{OUT} Adjust (V)	I_{OUT} (mA)	I_Q at I_{OUT} (µA)	I_{GND-SD} Max (µA)	Soft Start	P_{GOOD}	Noise (Fixed) 10 Hz to 100 kHz (µV rms)	PSRR 100 kHz (dB)	PSRR 1 MHz (dB)	Package
ADP7102	3.3 to 20	1.5 to 9	1.22 to 19	300	750	75	No	Yes	15	60	40	3 mm × 3 mm 8-lead LFCSP, 8-lead SOIC
ADP7104	3.3 to 20	1.5 to 9	1.22 to 19	500	900	75	No	Yes	15	60	40	3 mm × 3 mm 8-lead LFCSP, 8-lead SOIC
ADP7105	3.3 to 20	1.8, 3.3, 5	1.22 to 19	500	900	75	Yes	Yes	15	60	40	3 mm × 3 mm 8-lead LFCSP, 8-lead SOIC
ADP7118	2.7 to 20	1.2 to 5	1.2 to 19	200	160	10	Yes	No	11	68	50	2 mm × 2 mm 6-lead LFCSP, 8-lead SOIC, 5-lead TSOT
ADP7142	2.7 to 40	1.2 to 5	1.2 to 39	200	160	10	Yes	No	11	68	50	2 mm × 2 mm 6-lead LFCSP, 8-lead SOIC, 5-lead TSOT
ADP7182	−2.7 to −28	−1.8 to −5	−1.22 to −27	−200	−650	−8	No	No	18	45	45	2 mm × 2 mm 6-lead LFCSP, 3 mm × 3 mm 8-lead LFCSP, 5-lead TSOT

OUTLINE DIMENSIONS

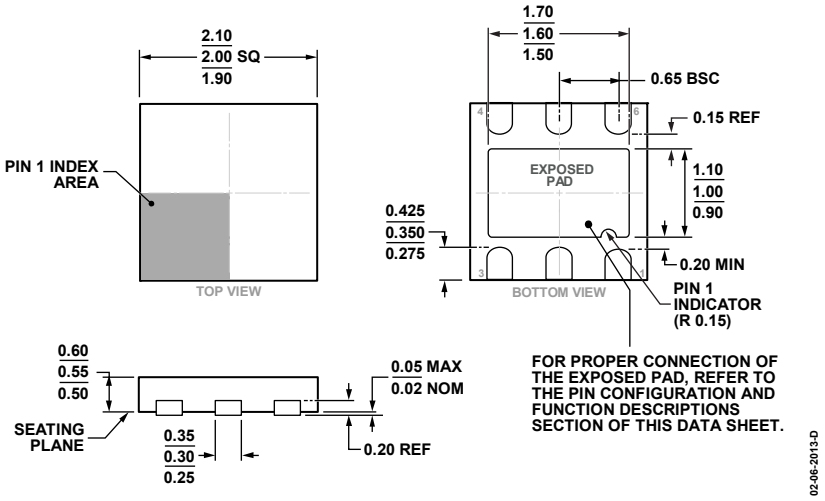
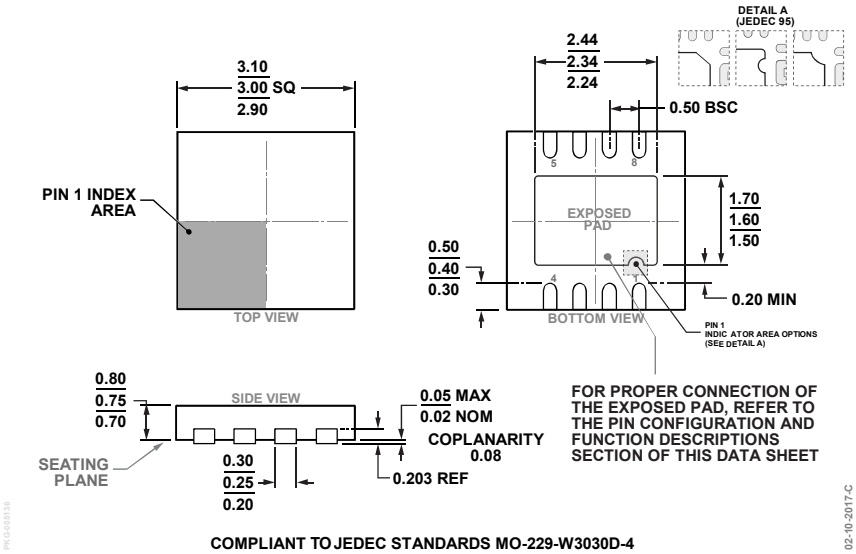


Figure 104. 6-Lead Lead Frame Chip Scale Package [LFCSP]
2.00 mm × 2.00 mm Body and 0.55 Package Height
(CP-6-3)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-229-W3030D-4

Figure 105. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 Package Height
(CP-8-11)
Dimensions shown in millimeters

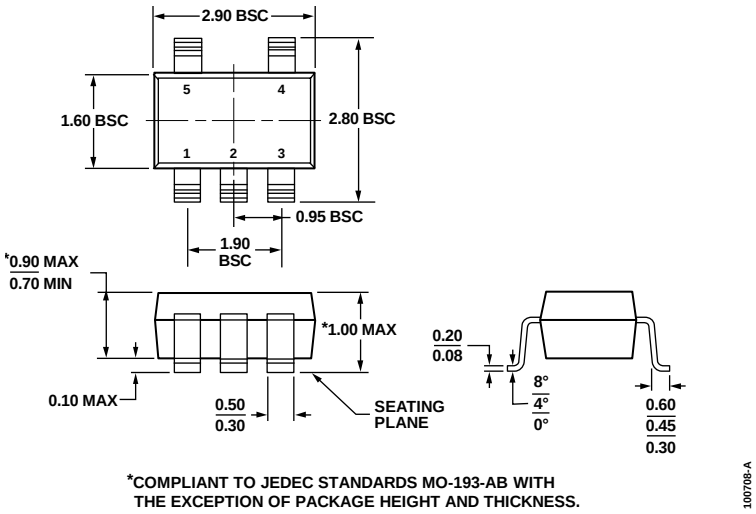


Figure 106. 5-Lead Thin Small Outline Transistor Package [TSOT]
(UJ-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage (V)[2]	Package Description	Package Option	Branding
ADP7182ACPZ-R7	−40°C to +125°C	Adjustable	8-Lead LFCSP	CP-8-11	LN6
ADP7182ACPZ-5.0-R7	−40°C to +125°C	−5	8-Lead LFCSP	CP-8-11	LN9
ADP7182AUJZ-R7	−40°C to +125°C	Adjustable	5-Lead TSOT	UJ-5	LN6
ADP7182AUJZ-1.8-R7	−40°C to +125°C	−1.8	5-Lead TSOT	UJ-5	LN1
ADP7182AUJZ-2.5-R7	−40°C to +125°C	−2.5	5-Lead TSOT	UJ-5	LN7
ADP7182AUJZ-3.0-R7	−40°C to +125°C	−3	5-Lead TSOT	UJ-5	LN2
ADP7182AUJZ-5.0-R7	−40°C to +125°C	−5	5-Lead TSOT	UJ-5	LN9
ADP7182ACPZN-R7	−40°C to +125°C	Adjustable	6-Lead LFCSP	CP-6-3	LN6
ADP7182ACPZN-5.0R7	−40°C to +125°C	−5	6-Lead LFCSP	CP-6-3	LN9
ADP7182ACPZN-2.5R7	−40°C to +125°C	−2.5	6-Lead LFCSP	CP-6-3	LN7
ADP7182ACPZN-1.5R7	−40°C to +125°C	−1.5	6-Lead LFCSP	CP-6-3	LQK
ADP7182ACPZN-1.2R7	−40°C to +125°C	−1.2	6-Lead LFCSP	CP-6-3	LRE
ADP7182UJ-EVALZ			Evaluation Board, TSOT		
ADP7182CP-EVALZ			Evaluation Board, LFCSP		

[1] Z = RoHS Compliant Part.
[2] For additional voltage options, contact a local Analog Devices, Inc., sales or distribution representative.